

Design of a Programmable Upsampler of Broadband Data for High Speed Operation

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Abstract— This paper presents the design of a high-speed programmable upsampler for the upsampling of a broadband signal. Several filter architectures and types of logic are compared. A Cascaded Integrator Comb (CIC) filter has been selected to achieve a power efficient upsampler with a operating speed of 3 GHz with an estimated 250mW power consumption while at the same time keeping the amount of generated noise low to avoid interference with the analog part of the IC.

I. INTRODUCTION

Nowadays the data rate of communication standards, such as digital television broadcast and internet-through-cable, becomes larger and larger. This increase of data rate has to be transmitted over the available bandwidth as efficiently as possible. This places ever more stringent demands for the components involved for the generation and reception of these signals.

An example of such a standard is DOCSIS (Data Over Cable Service Interface Specification) [1]. This standard is developed to broadcast large amounts of information in a metropolitan area. The DOCSIS standard specifies a frequency range of 88 - 860 MHz for the downstream path. This bandwidth is split into many carriers, each 6 - 8 MHz wide, depending on the geographical location.

In most existing systems each individual carrier is converted with a DAC and then upconverted with an analog mixer to the desired frequency. This requires for N parallel channels N DACs and N mixers, see Fig. 1(a), with all the additional analog filters. A potentially more advantageous system is described in this paper, which combines a large group of carriers, possibly all, and uses one DAC to convert the digital signal into an analog signal, see Fig. 1(b). All the mixing and modulation is done in the digital domain. Thanks to new developments in high speed DACs that may offer these possibilities [2], [3], [4]. The main advantage

of this approach is the reduced complexity of the analog system. Analog mixers require tuning to calibrate them to the desired frequency, which is not required in the digital system. Moreover, problems like aging and temperature drift will not affect the performance of the digital system. Another advantage is the reduced size of the system. In the traditional approach, see Fig. 1, the size of the modulation system is rather large due to the large amount of required analog components. On the other hand, the digital modulator can be integrated into a single IC with only one analog filter at the output, for which no calibration is required.

The application which is used as an example in this paper is the DOCSIS standard, although upsamplers are common building blocks and are used in many other systems. The complexity of the upsampler is almost completely determined by the filtering which is required. This is especially true when the upsample factor becomes large [5].

The main challenges in the new approach are A. the power consumption, B. the interference to the analog DAC through the power supply and substrate, C. the design complexity. These challenges will be discussed in the remaining sections. Here, a number of potential types of upsamplers is discussed. In section II, the requirements of the upsample system are given. In section III, types of filters which could be used in the system are described. Section IV describes the type of logic which is used for the high speed operation of the filter, and section V shows the upsample filter implemented in CMOS 90nm process.

II. FILTER REQUIREMENTS

In the proposed system, see Fig. 1(b), the individual carriers have to be combined into a single signal before the actual D/A conversion is performed. This requires that the data of each carrier is upsampled from the data rate (5.36 MSymbols/s) to the system output frequency. If the complete bandwidth of the

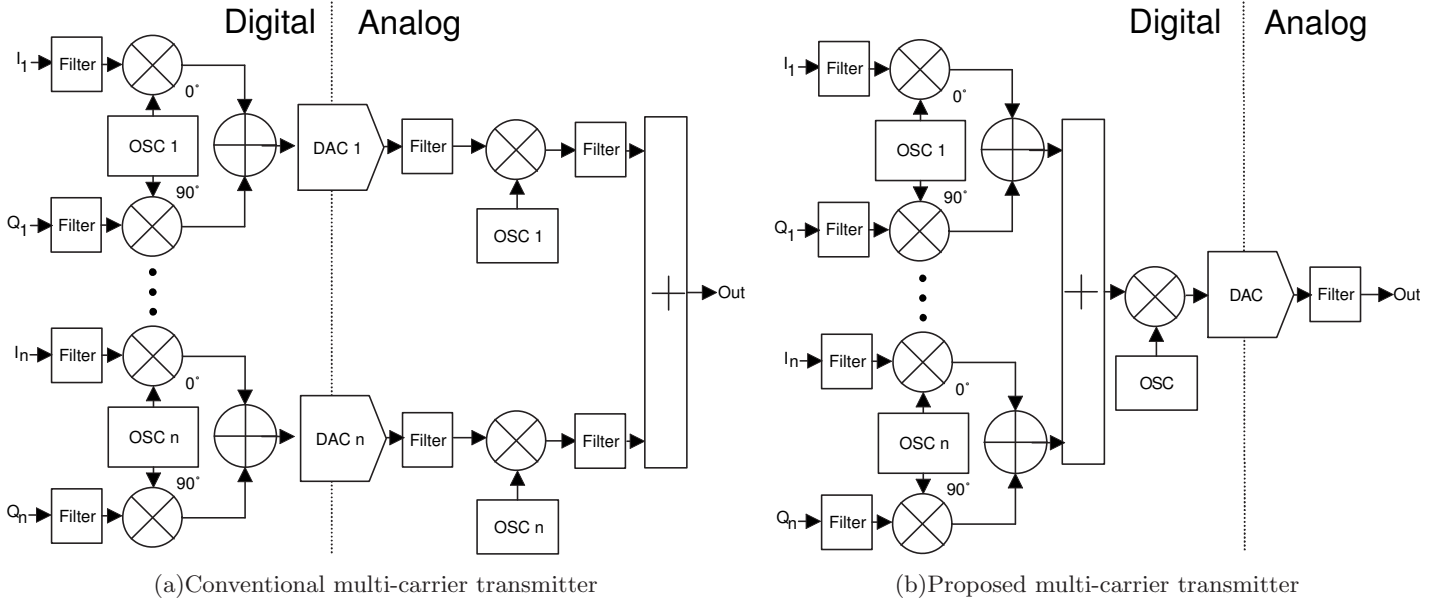


Fig. 1. The multi-carrier QAM modulator and upconversion chain.

channel is to be covered by a single DAC, the clock frequency of the DAC should be larger than 2 GHz. To simplify the analog filters and the digital inverse sinc correction filter a clock frequency of 3 GHz is a better choice. The total upsample rate for the signal becomes therefore equal to about 300.

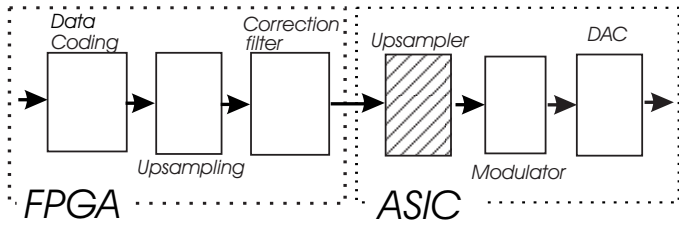


Fig. 2. The overview of the implementation of the upsampling

The upsampling could be done in a single step, but that would result in a non optimal system [5]. A better approach is to upsample in multiple steps. The overview of the implementation of the upsampling is shown in Fig. 2. This paper will focus at the shaded part. The data has to be delivered at the same rate as the DAC is clocked. The number of bits required for this DAC is about 10 bits. At these frequencies data transmission through the PCB becomes extremely difficult. Therefore, the last part of the upsampling is done just in front of the DAC on the same chip. The data can then be delivered towards the chip at a lower data rate, which simplifies the design of the PCB. The coding, error correction and modulation, as re-

quired by the DOCSIS standard, are implemented in an FPGA. The upsampler discussed in this paper is designed in 90nm CMOS process with a supply voltage of 1.2 V. Several aspects are used to evaluate the different possible implementations. They are:

Speed: The output sampling rate should be equal to 3 GHz. This results in stringent demands for the logic used.

Power: An efficient design should be used to minimize the power consumption.

Programmable sample rate: For this design a programmable sample rate will be implemented. Thus additional requirements for the architecture of the upsampler apply.

Electro Magnetic Interference (EMI): On the same chip analog components, such as a DAC, are integrated. Therefore it is required that the amount of noise generated by the digital logic should be minimized. The performance of these analog signals are easily corrupted by the interference coming from the digital blocks as noise via the supply and substrate. In the DACs that are presented in [2], [3], [4], a lot of attention is given to the design of the digital decoder used to convert the binary input to the thermometer coding used inside the DAC. These decoders are relative small digital blocks and are designed for operation frequencies of only several hundreds of MHz. The amount of digital logic that is required in our design is more extensive and operates at a higher frequency. Therefore, attention should be given to keep the EMI as low as possible.

In Fig. 3, the principle schematic of an upsampler is shown. In the first block the data is interpolated with $R - 1$ zeros then the signal is filtered. The filter

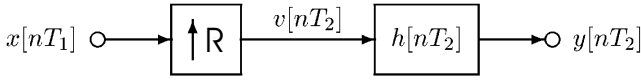


Fig. 3. Upsampling and filtering

requirements are:

Stopband attenuation: The filter should attenuate the signal outside the passband band enough as is defined by the application, see Fig. 4. For the DOC-SIS standard the attenuation should be larger than the value required as set in the standard for the total transmitter path.

Operation speed: Because of the high speed requirements pipelining is required. With pipelining the amount of operations done within one clock cycle can be reduced, at the cost of more overhead due to the additional registers that are used. Some filters require a feedback from the output to the input within one clock cycle. In that case pipelining can not be used to increase the operation speed of the filter, because a too large latency is introduced by using pipelining.

Passband ripple, phase response: When the bandwidth of the signal is large the phase response and passband ripple of the filter become important. This should be taken into account during the design of the filter.

Complexity: The complexity should be made as low as possible, because the complexity affects the power consumption and required area of the upsampler.

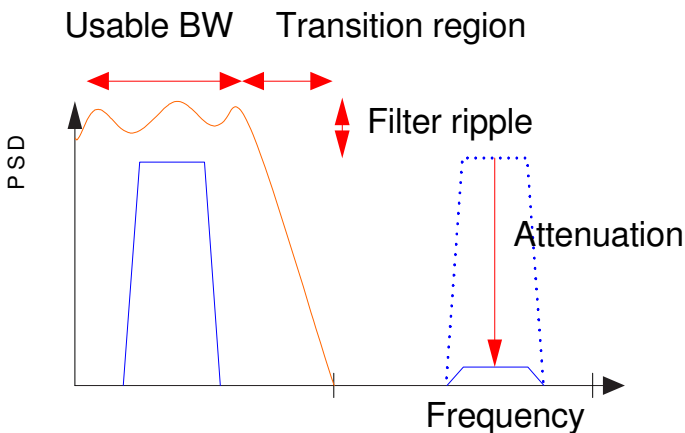


Fig. 4. Upsampling filter specifications

III. FILTER ARCHITECTURES

In this section we will look at suitable filter architectures. Several filter architectures, see Fig. 5, exist such as FIR, IIR and CIC filters [6].

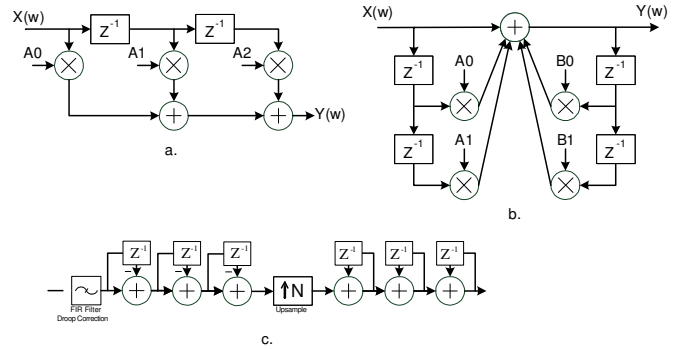


Fig. 5. Filter structures a. FIR filter, b. IIR filter, c. CIC filter.

FIR filter: This common filter is flexible, because it has many parameters that can be adjusted to accommodate the required filter transfer characteristics. The FIR filter can have a linear phase response and the passband ripple can be designed to be low. In addition, it is possible to design for large attenuation for out of band components and a small transition region, at the cost of increased complexity. Because the filter has no internal feedback, pipelining can be used. This allows for high speed operation. A disadvantage of the FIR filter is its complexity due to the large number of multipliers needed and since multipliers are complex building blocks. The multipliers can be used at the lower sampling rate of the upsampler, which results in reduced operating speed [5]. Another method to reduce complexity is the multiplication by factors of two or combinations of factors of two. A widely used method for replacing a multiplier with shift registers and adders is based upon the canonic-signed-digit (CSD) expression of the multiplicand [7], [8].

IIR filter: IIR filters have the advantage that they are small compared to a FIR filter with a similar transfer characteristic. The IIR filter structure is based on feedback, which limits the use of pipelining in the multipliers and adders. Therefore, the operation speed is reduced. Although transformations have been proposed in order to pipeline IIR filters [9], these highly pipelined IIR filters are usually not more computational efficient than their FIR counterparts. In addition, their phase characteristic is nonlinear, which introduces distortion to broadband signals, such as the signals used in this application.

Cascaded Integrator Comb (CIC) filters: This filter structure [10] uses no multipliers, but only adders and delays. The complexity is therefore low, compared to a FIR filter. It has a linear phase response, therefore the group delay is constant. The filter upsample ratio used is independent of the structure of the filter. Only the gain of the filter depends on the upsample rate. Therefore, the output should contain a shift register that selects the correct bits from the output word. The number of stages (N) and the delay in the comb stages (M) determines the ability to attenuate the signal outside the band of interest. The shape of the filter is given by the order (N), the delay in the comb stages (M) and the upsample ratio (R). In Fig. 6, the frequency response is drawn for a filter with an upsample ratio of $R = 15$, $M = 1$ and $N = 5$. Increasing the order N will increase the passband droop. A possible solution to compensate for this passband droop is to use precorrection. This can be done by

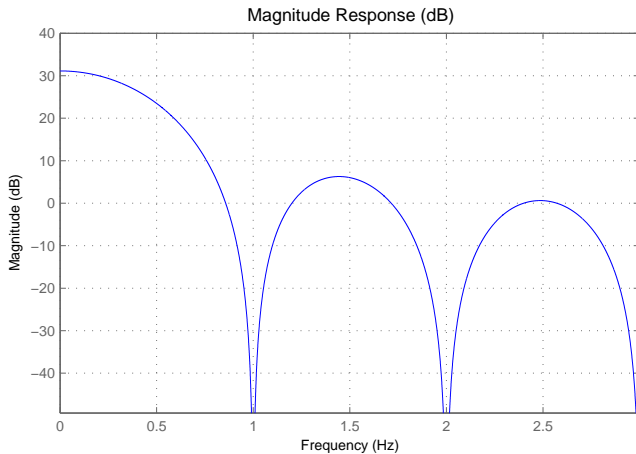


Fig. 6. CIC filter response for $N = 2$, $M = 1$ and $R = 6$

placing a FIR filter before the CIC filter to compensate the frequency response, see Fig. 7. This FIR filter could be placed at the lower sample rate side of the CIC filter. This increases the usable bandwidth for the CIC filter. Because of the low complexity this type of filter has been chosen.

IV. LOGIC

In this section we will compare a number of logic styles, see Fig. 8, which can be used to implement this filter. A few criteria will be set. The first is the mentioned operating speed. The second is the amount of noise it generates.

CMOS: A common type of logic is CMOS logic. However, due to the requirements with respect to the

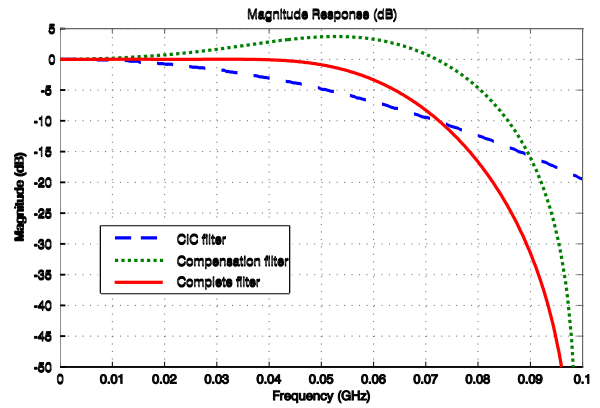


Fig. 7. CIC filter passband response with compensation filter

operating frequency and EMI, CMOS logic is not used in this design [11].

Domino logic: is often used in high speed applications [11]. Domino logic has the advantage that it uses only NMOS transistors at the input, which reduces the input capacitance and transistor count, compared to CMOS logic. However, this type of logic has also several disadvantages. One of the disadvantages is the sensitivity to noise on the inputs. In addition, domino logic has a high switching activity compared to, for example, CMOS logic. The output nodes of the gates are precharged every clock cycle, which results in a large dynamic power and, hence, more EMI.

CML (Current Mode Logic): CML like domino logic has the advantage that at the input only NMOS transistors are used, which reduces the input capacitance and increases the operating speed compared to CMOS logic [11]. CML has a reduced signal swing at the output. This increases the speed, because the capacitance of the wires and input has to be charged/discharged less. Furthermore, the reduced signal swing reduces the coupling between adjacent signals and because of the constant current of the current source in the gate, the switching noise and supply fluctuations are reduced. In addition, the XOR function, which is used in full adders, can be implemented efficiently, compared to CMOS and domino logic. In addition, CML itself is also more noise immune because of the differential nature. The power supply current is constant and independent of the operating frequency or switching activity. CML has also disadvantages; one is that it needs more wires. Therefore CML is preferred for high frequency applications, where the constant supply current is advantageous.

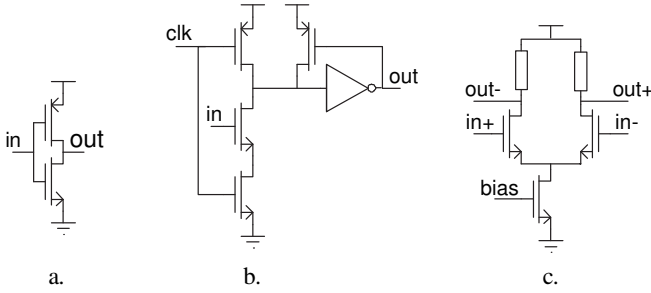


Fig. 8. Types of logic, a. CMOS, b. Domino Logic, c. CML

V. RESULTS

The block schematic of the upsampler that was implemented is shown in Fig. 2. We use CML for the logic, because of its speed and the reduced amount of noise it generates. The circuit was designed and the layout has been implemented. The technology used for the implementation of the circuit is the 90nm CMOS process. To achieve the required attenuation in the stopband to according fulfill the DOCSIS standard requires five stages. The comb section block, see Fig. 9, has an input width of 10 bits and an output width of 14 bits to accommodate for the bit growth of the CIC filter [10]. The total number of comb cells is equal to 65. The comb cells are optimized to operate at a frequency of 200 MHz. The next block in Fig. 9, is the upsampler. This block interpolates $R - 1$ zeros for an upsample rate of R . In addition, this block divides the clock from the high sample rate to the low sample rate. The upsampler is followed by the integrator section. The integrator section and upsampler are designed and optimized to operate at the high output frequency of the upsampler, which is 3 GHz. Like the comb section also the integrator section has bit growth at every stage. The output width of the integrator section is equal to a total of 26 bits. The gain compensator selects only 10 bits depending on the upsample rate that is used. A total number of 100 integrator cells, see Fig. 9, are needed. The integrator section is fully pipelined. For these high frequencies pipelining becomes essential. However, the disadvantage is that the overhead becomes larger. In addition, the latency of the upsampler is increased. Therefore, it is best to minimize the pipelining where ever possible. The resulting total equivalent number of gates for the integrator section is 2040, the tail current of this equivalent gate is on average $40\mu A$. To test for supply bounce problems a simple RLC network is used, with 4 Ohm and 4nH, which are realistic values.

Simulations demonstrates that there is only a small voltage ripple of tents of mV when it operates at full speed which excludes decoupling capacitance, which is considered small compared to the hundreds of mV reported for CMOS [12]. This demonstrates the efficiency of the CML. As a result of the chosen CML logic less decoupling capacitance is required, which reduces the required area. A critical part of the design of the upsampler is the clock network. The clocking of the filter requires careful design in order to clock all the integrator cells at the correct moment. The estimated power consumption of the upsampler is equal to 250mW, which includes the clocking and local interconnect of the upsampler.

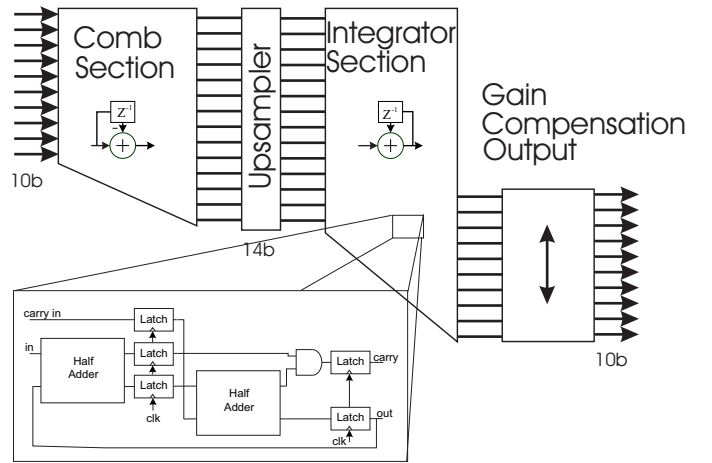


Fig. 9. Schematic of the CIC upsampler

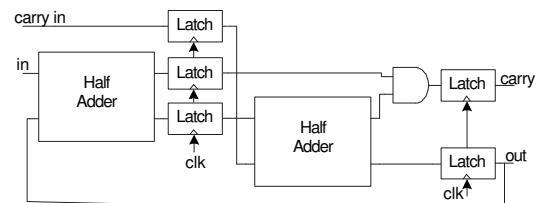


Fig. 10. Schematic of the CIC integrator cell

VI. CONCLUSION

In this paper several filter architectures were compared for the implementation of a high speed upsampler. In addition, a number of logic styles and filter architectures are compared. The major challenges that the designer will face in the implementation of an upsampler are highlighted. Analysis showed that for the design of a programmable high speed upsampler the combination of a CIC filter with correction filter implemented in CML is preferable. The use of CML increases the operation speed and reduces the amount

of EMI generated, which is beneficial for the analog circuitry that is implemented on the same IC. The design, which is optimized for 3 GHz in combination with a low power consumption and reduced interference, is simulated and built in CMOS 90nm.

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