

A 3x Subharmonic 60-GHz Oscillator

Wei Liat Chan and John R. Long

Abstract— An injection-locked I/Q oscillator is designed in this paper. The oscillator locks onto the third harmonic of the injected 20 GHz signal. With only LC lines setting the delay within the oscillator, high I/Q accuracy is expected. The 60-GHz free-running oscillator, with phase noise of -114 dBc/Hz at 1-MHz offset, consumes 9.6 mW (excluding buffers) from a 1.2-V supply. The locking range for an input with 200 mW swing is from 56.4 – 63.6 GHz.

Index Terms— Subharmonic oscillator, 60-GHz

I. INTRODUCTION

The availability of 7 GHz bandwidth around 60 GHz has generated much interest recently [1-3]. It is motivated by the possibility of realizing a wireless communication system with gigabit-per-second data transfer rate. Presently, III-V semiconductor technology has been used extensively to implement such circuits operating at high frequency, which can be prohibitively expensive. However, a low-cost silicon process, for example BiCMOS, also has potential in meeting the challenges at this frequency. The rapid scaling of silicon technology leads to the emergence of transistors with transit frequencies over 200 GHz, and improvements in the passive components. Moreover, BiCMOS process allows for high levels of integration, thus reducing the number of expensive off-chip components needed. At millimeter wavelength, on-chip antennas are also a possibility to achieve a fully integrated, low-cost transceiver design.

Fig. 1 shows a generic block diagram of a radio-frequency (RF) front-end. The local oscillator (LO) generates the carrier signal at either the same frequency as the incoming RF signal (as in a homodyne transceiver) or with a difference – defined by the intermediate-frequency (IF) – in a heterodyne architecture. In both cases, a 60-GHz signal source is required. At such high frequency, the oscillator requires substantial current for reasonable phase noise performance, and it is highly sensitive to parasitics. Controlling blocks of the LO must also operate at this frequency, which only increases the overall power consumption.

In this paper, the design of a 3x subharmonic 60-GHz in-phase and quadrature (I/Q) oscillator in a 0.13- μm SiGe BiCMOS process [4] is described. An injection-locked oscillator can provide a highly stable signal, and its phase noise is not critical as the output phase noise is largely determined by that of the injected signal source. With this

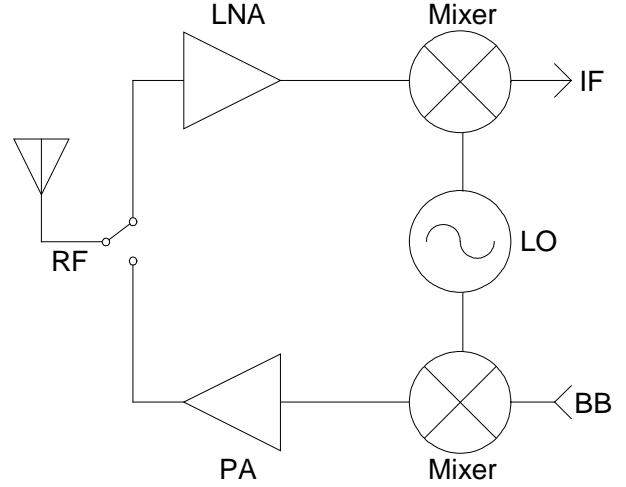


Fig. 1. Block diagram of a RF front-end.

oscillator, all controlling blocks only need to operate at a third of the intended frequency, i.e. 20 GHz, thereby conserving power, and simplifying their designs.

II. PRINCIPLE OF INJECTION LOCKING

The behavior of an injection-locked oscillator is described by Alder's equation [5]. The locking range of the oscillator is given by $\omega_0 \pm \Delta\omega$ such that

$$\Delta\omega = \frac{V_{INJ}}{V_0} \frac{\omega_0}{2Q} \quad (1)$$

where V_{INJ} and V_0 refer to the amplitude of the injected signal and free-running oscillation, respectively, ω_0 is the free-running frequency of the oscillator, and Q is the quality factor of the tank. When locked, the oscillator tracks the injected signal with a phase difference as the oscillator moves away from its free-running frequency. This continues until the phase difference increases to $\pm 90^\circ$, beyond which the oscillator loses lock. It then oscillates at its free-running frequency. Although the above theory is developed for fundamental locking of an oscillator, the same principle can also be applied to subharmonic locking.

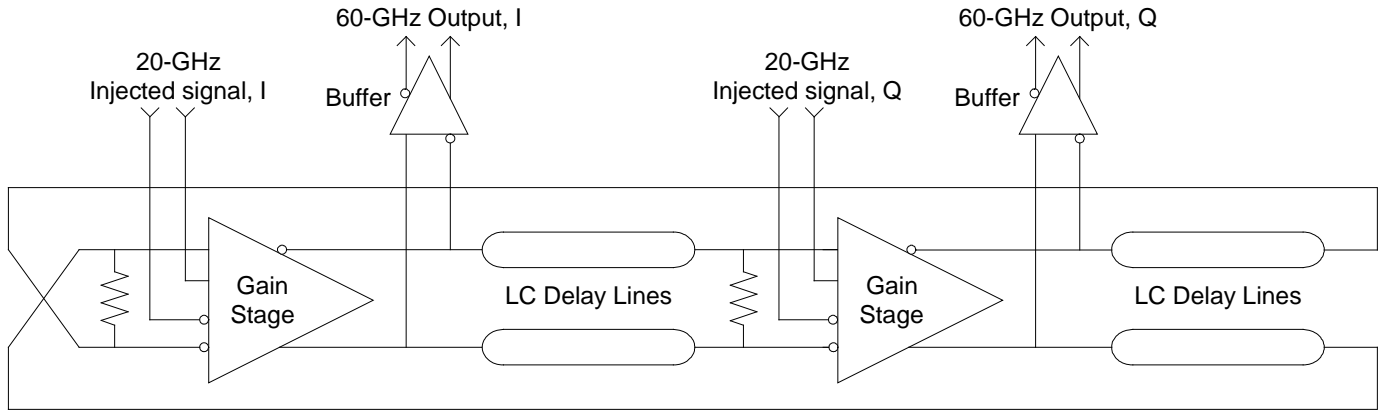


Fig. 2. Architecture of a 60-GHz I/Q oscillator.

Equation 1 shows that to obtain a wide locking range, V_{INJ} must be significantly greater than V_0 , and the Q of the tank has to be sufficiently small. Note that although the low Q of the oscillator results in poor phase noise, the oscillator – once locked – will have a phase noise given by approximately $20\log(n)$ smaller than that of the injected source (where n is the harmonic order to which the oscillator is subharmonically locked on) [6]. It is expected to be easier to design a signal generator at 20 GHz such that the phase noise of the locked oscillator at 60 GHz is lower than that of fundamental oscillator at 60 GHz. In addition, the overall power consumption of both the 20-GHz signal source and injection-locked oscillator may also be lower than that required by a single oscillator intended for 60 GHz.

III. 3X SUBHARMONIC I/Q OSCILLATOR ARCHITECTURE

The block diagram of the I/Q oscillator topology is given in Fig. 2 [7]. The LC delay lines provide 90° phase shift, while the cross-connected feedback paths contribute an additional 180° to sustain oscillation. At the end of each line is a termination resistor, which equals the characteristic impedance of the line. The two gain stages replenish the energy lost in the delay lines to maintain oscillation, and can be driven by an external signal generator for injection locking.

The gain stages are resonant tuned such that only the LC lines provide the delay. In this way, higher I/Q accuracy is expected, as the fabrication of LC delay lines (using the top metals of any process) can be better controlled than for transistors.

IV. LC DELAY LINES

Fig. 3 shows a simple LC delay line circuit model [8] which can be used for time domain simulations. M is the coupling factor of the two inductors; C is the capacitance between the

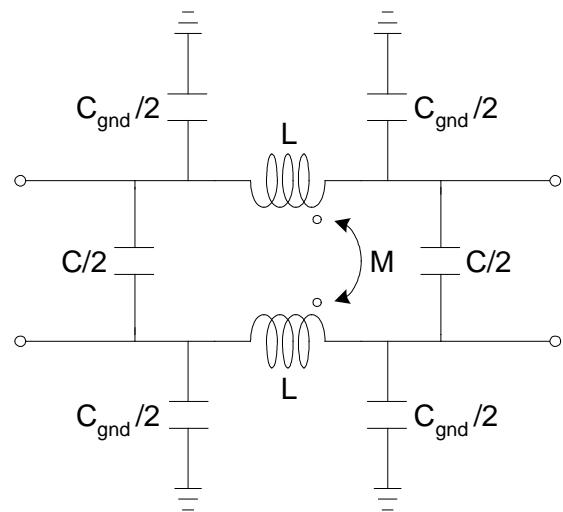


Fig. 3. Simple delay line model.

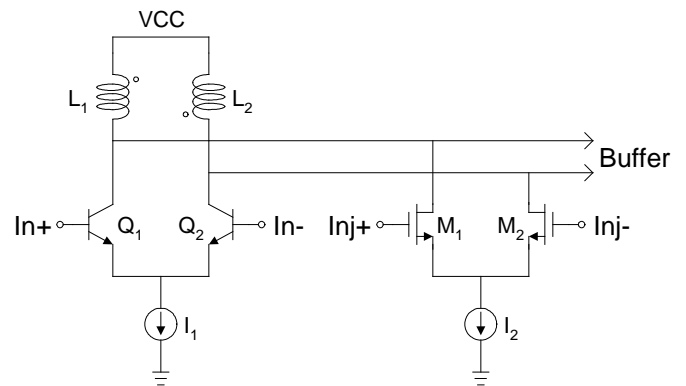


Fig. 4. Circuit implementation of a gain stage.

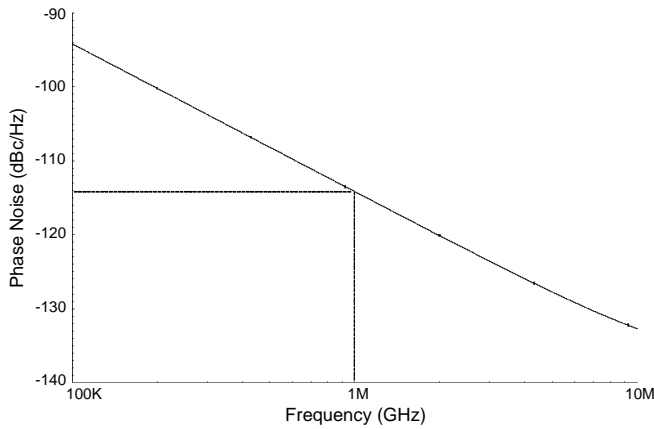


Fig. 5. Phase noise of free-running oscillator at 60 GHz.

two inductive lines, whereas C_{gnd} is the capacitance of the line to ground.

The required inductance is first estimated from the length of interconnect needed to implement 90° phase shift at 60 GHz, thereafter its capacitance can be easily calculated from the length of the line. These values are then used in the simulation of the oscillator. This process is reiterated until a better approximation of the inductance and capacitance is found. The LC delay line structure is then designed so as to keep the layout compact, and simulated with 3-D electromagnetic software. In this way, the number of runs required for the

highly time-consuming electromagnetic simulation is greatly reduced.

V. GAIN STAGE

At 60 GHz, the circuit implementation for the gain stage should be simple in order to reduce the parasitics. Fig. 4 shows the circuit schematic of the gain stage. A bipolar differential amplifier realizes the gain cell, whereas the injection stage is a CMOS differential pair. Each amplifier is biased with its own current source.

The input impedance of the LC delay lines loads the tank of the gain stage; therefore, a high gain amplifier is required to sustain the oscillation. A bipolar differential cell can provide high gain at low bias current. For the injection stage, a CMOS injection pair is, however, preferred to a bipolar realization. The CMOS differential pair has higher input impedance than the bipolar implementation, as the injection amplifier will be voltage driven by an external 20-GHz signal source. Through amplitude limiting (i.e. clipping) of the injected sinusoidal signal, which produces odd-order harmonics, the CMOS injection pair amplifies the third harmonic to lock the oscillator. Both the gain and injection amplifiers are carefully designed, and their bias currents properly chosen to maximize the locking range.

An output buffer (not shown in Fig. 4 for simplicity) – a bipolar differential stage with inductive loads – cascades each gain stage to drive subsequent circuits, e.g. mixers.

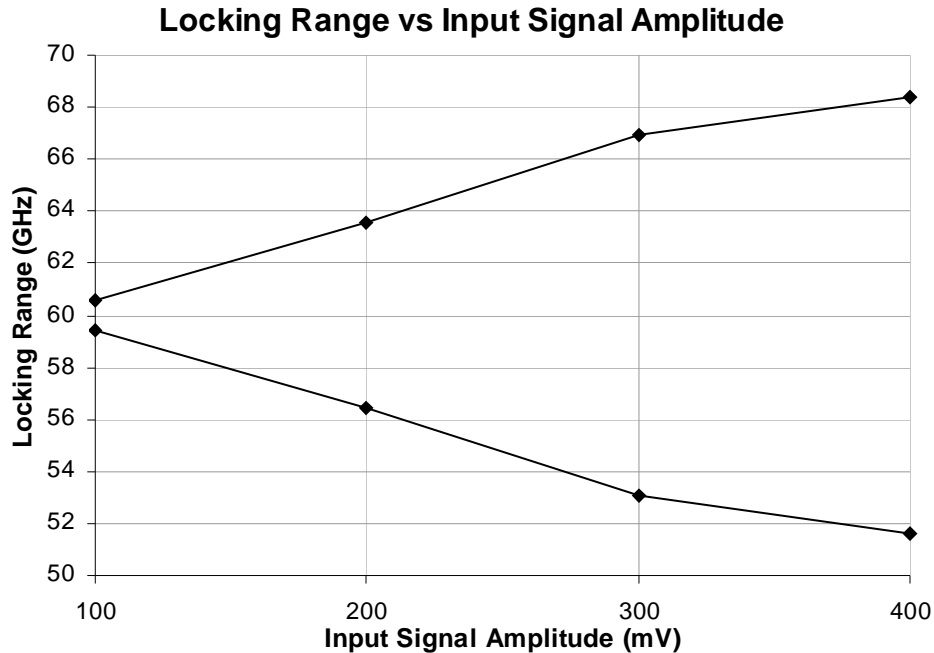


Fig. 6. Locking range of the oscillator against injected signal swing.

VI. SIMULATION RESULTS

The 3x subharmonic 60-GHz I/Q oscillator consumes 9.6 mW from a 1.2-V supply, with an additional 7.2 mW by the output buffers. The free-running frequency of the oscillator is 60 GHz, with phase noise of -114 dBc/Hz at 1-MHz offset from the carrier, as given in Fig. 5. Fig. 6 shows the locking range of the oscillator with injected signal amplitude. As expected, the locking range increases with injected signal amplitude, and the locked region is symmetrical about the free-running frequency, i.e. 60 GHz. It can also be seen that the efficiency of injection locking decreases with large input signal swing. Thus for optimal locking efficiency, a signal with less than 300 mV swing should be used.

Injected with a signal with amplitude of only 200 mV, a locking range of more than 7 GHz (56.4 – 63.6 GHz) is achieved, which is sufficient to cover the entire 7 GHz bandwidth allocated. The locking range decreases less than 10% when the simulation temperature is increased to 125° C. Note that it is comparatively easier to design a 20-GHz on-chip signal generator, which can provide 200 mV output swing from a 1.2-V supply.

With meticulous design and optimization, it is possible to obtain a wide locking range from a relatively small-injected swing, and yet, the phase noise of the free-running low power oscillator is not significantly worsened by the low Q of the tank due to the loading from the termination resistors.

VII. CONCLUSION

The design of a 3x subharmonic 60-GHz I/Q oscillator is presented. The gain stages are resonant tuned such that only the LC delay lines set the delay within the oscillator in order to achieve high I/Q accuracy. Including the output buffers, the oscillator consumes 16.8 mW from a 1.2-V supply, and has a free-running oscillation frequency of 60 GHz, with phase noise of -114 dBc/Hz at 1-MHz offset. The oscillator can be locked over 7 GHz with an injected signal swing of only 200 mV.

ACKNOWLEDGEMENT

This work was supported by Freeband WiComm.

REFERENCES

- [1] C. H. Doan, S. Emami et al., "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.
- [2] B. A. Floyd, S. K. Reynolds et al., "SiGe bipolar transceiver circuits operating at 60 GHz", *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.
- [3] B. Razavi, "A 60GHz direct-conversion CMOS receiver," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 400-401.
- [4] B. A. Orner, Q. Z. Liu et al., "A 0.13 μm BiCMOS technology featuring a 200/280 GHz (f_T/f_{max}) SiGe HBT," in *Proc. Bipolar/BiCMOS Circuits and Technology Mtg.*, Sept. 2003, pp. 203-206.
- [5] R Alder, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 61, pp. 1380-1385, Oct. 1973.
- [6] X. Zhang, X. Zhou et al., " A theoretical and experimental study of the noise behavior of subharmonically injection-locked oscillators," *IEEE Trans. Microwave Tech*, vol. 40, pp. 895-902, May 1992.
- [7] D. K. Ma and J. R. Long, "A subharmonically injected LC delay line oscillator for 17-GHz quadrature LO generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1434-1445, Sept. 2004.
- [8] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RFIC's," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 357-368, Mar. 1997.