

Uniformity of Chemical Vapor Deposited Boron-Silicide Layers on Silicon

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Abstract—High-quality Schottky diodes and ultra-shallow p⁺n junctions have been implemented with a novel chemical vapor deposition technique that forms a boron-silicide (B_xSi) layer on silicon. In this paper the uniformity of such a doping method has been electrically characterized in terms of bulk and perimeter currents. The results show that B mainly segregates at the contact edges during the first stage of deposition. For long exposure the uniformity of boron-silicide layers is improved respect both to the geometry dependence and position over the wafer.

Index Terms—Boron-silicide (B_xSi), chemical vapor deposition (CVD), delta-doped layer, surface passivation, ultra-shallow junction.

I. INTRODUCTION

FORMATION of extremely shallow and highly doped junctions is of crucial importance for future bipolar and MOS transistor technology. However, conventional ion implantation may not be able to overcome the trade-off between progressive reduction of junction depth and optimization of sheet resistance. In fact, the associated implantation damage is mainly responsible for transient-enhanced diffusion (TED) during the subsequent dopant activation by (rapid) thermal annealing. This is particularly severe for boron impurities and can lead to a significant broadening of the desired dopant profiles. Moreover, the induced defects in the silicon substrate could cause junction leakage current. As an alternative to the traditional B⁺ or BF₂⁺ implantations, a surface-reaction doping using B₂H₆ as gas source has been applied for implementing ultra-shallow junctions in the molecular layer doping (MLD) [1]-[2], and vapor-phase doping (VPD) [3]-[5]. Since these methods prevent damage in the substrate, TED is effectively avoided and low-leakage junctions are formed. However, they suffer either from poor control of the high-concentration boron adsorbed layers or process complexity.

In an earlier paper we presented a novel doping technique that uses a pure boron atmospheric/low-pressure chemical vapor deposition (AP/LPCVD) in a commercially available epitaxial reactor to form less than 2-nm-thick δ-doped boron-

silicide (B_xSi) layer on the silicon surface [6]. For deposition temperatures from 500 to 700 °C the B₂H₆ gas source will in first instance chemically react with the Si surface leading to B adsorption and B_xSi formation. This layer acts as a highly doped p-type region that can either ensure low-ohmic contact to lightly doped p-regions or provide an ideal p⁺n junction on n-regions. For long exposure B segregates at the surface to form a very slow growing amorphous layer of pure B (α-B) that has semi-metallic properties with a high resistivity of ~ 10⁶ Ω·cm. Moreover, in combination with thermal or excimer laser annealing (ELA), the as-deposited α-B/B_xSi layers can supply a TED-free source of B for thermal diffusion of junctions. During diffusion the α-B layer acts as a capping layer that prevents B desorption from the B_xSi layer, and also gives an abundant supply of boron that can be diffused into the Si substrate. Thus this method offers a high doping efficiency and a good control of the resulting junction depth.

In this work the electrical properties of the as-deposited α-B/B_xSi stack have been studied by fabricating and measuring diodes where the B-deposition is formed directly in contact windows for several B₂H₆ exposure times. Particularly, an electrical characterization of diodes with respect to the bulk and perimeter currents is performed in order to evaluate the pattern dependence of the uniformity of B-doped surface layers.

II. EXPERIMENT

A. Boron CVD deposition

The boron deposition is performed in an ASM Epsilon One AP/LPCVD epitaxial reactor on Si(100) wafers using B₂H₆ as the gas source diluted in H₂, for a range of deposition temperatures and pressures from 500 to 700 °C and from 36 to 760 Torr, respectively. The formation of the boron layers is slower the lower the temperature and the B₂H₆ partial pressure, and predominantly determined by the exposure time. The results presented here correspond to 1 s to 30 min depositions at 700 °C and B partial pressure of 3.56 × 10⁻³ Torr in a 760 Torr ambient.

The pure B only deposits on clean Si surfaces and can thus be placed selectively in contact windows to the silicon. For the experiments a native-oxide-free silicon surface is ensured by HF dipping before entering the CVD reactor and using an in-situ 30 min pre-bake step at 900 °C in H₂ atmosphere before

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deposition. Moreover, the integration of such B-layers in a device process is facilitated by the fact that the B-layer is very robust: it does not oxidize in air and is resistant to HF etching.

A surface morphology analysis of B_xSi layers has shown that nucleation is initiated for a small dose of B_2H_6 , and for increasing doses and temperatures grains form and merge into a rough film as a mixture of boron and silicon atoms [7]. In the present work, the process conditions lead to an ultra-shallow rough layer of only ~ 2 nm thick. In fact, the high flow rate of diborane induces a rapid B segregation that can prevent re-evaporation of adsorbed boron into the atmosphere and promote the reactivity of the chemisorbed species with the surface silicon atoms for the B_xSi formation. In addition, the relatively low process temperature (700 °C) ensures a negligible diffusion of B atoms into the substrate.

TABLE I
BORON SURFACE CONCENTRATIONS OF DELTA-DOPED LAYERS

Deposition time	α -B removal	Dose (cm^{-2})
1 s	-	3.84×10^{13}
5 s	-	4.22×10^{14}
20 s	-	2.47×10^{15}
1 min	-	9.82×10^{15}
10 min	-	1.55×10^{17}
10 min	x	9.16×10^{13}

The B surface doping densities of the processed δ -doped boron layers are summarized in Table I. When the deposition time increases, the total B concentration is seen to increase until the boron coverage exceeds 1 ML (ML = mono-layer), which will be comparable to the corresponding Si(100) surface atomic density of $6.78 \times 10^{14} cm^{-2}$. This results in the α -B layer formation. For many applications the high series resistance through this layer will limit the device performance at high current levels. The α -B layer can be removed by standard cleaning in HNO_3 (100%) followed by a HF (0.55%) dip to remove the resulting cleaning oxide. This process will, however, also remove a substantial part of the B_xSi layer as can be seen in Table I, which has also been measured to significantly increase the B_xSi sheet resistance. On the other hand, after a thermal annealing step the removal of the α -B is no longer an issue.

B. Diode fabrication

The new doping method was successfully applied to fabricate high-quality Schottky diodes and ultra-shallow p^+n junctions. A schematic cross-section of the fabricated devices is shown in Fig. 1. The starting material was a 2-5 Ω -cm p-type Si(100) substrate. A 0.9 μm n-doped epitaxial layer ($\sim 10^{16} cm^{-3}$) was grown on an n^+ buried layer. The epi-doping concentration was increased to $\sim 10^{17} cm^{-3}$ by using P^+ implantations through a 30 nm thermal oxide. Then a 300 nm LPCVD TEOS oxide surface isolation layer was deposited in which the contact windows to be treated with a B deposition were plasma etched with soft landing on the Si. The boron

CVD deposition was carried out as described above for different B_2H_6 exposure times. The B-treated contact windows were directly covered by an Al/Si(1%) PVD metallization. After metal patterning, a 400 °C alloy step in forming gas was performed.

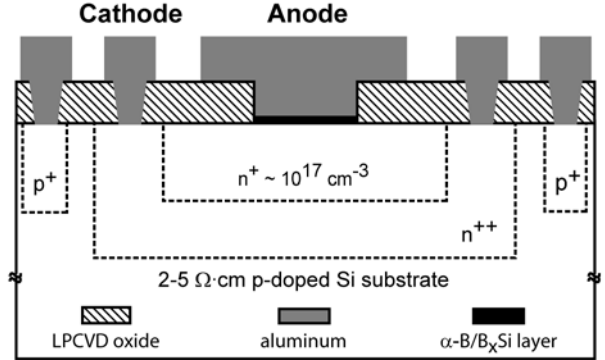


Fig. 1. Schematic cross-section of the fabricated diodes.

The uniformity of B-doped surface layers has been investigated by using a ring-shaped contact opening geometry. At a certain forward bias voltage, the total diode current can be expressed as sum of the bulk and perimeter components, according to the following relation:

$$I = I_{Bulk} + I_{Perimeter} = J_B \cdot A + J_P \cdot P \quad (1)$$

in which A and P are the area and the perimeter of the contact window, respectively. However, the test structures are designed with a constant perimeter (862 μm) and the area is given by $A = P \cdot W / 2$, where W is the width of the ring (1, 2, 4, 6, and 10 μm).

Therefore, the following linear dependence

$$\frac{I}{P} = \frac{J_B \cdot W}{2} + J_P \quad (2)$$

can be plotted as a function of W , and the bulk and perimeter current densities can be extracted from the slope and the intercept, respectively.

III. ELECTRICAL CHARACTERIZATION

The diode I-V characteristics for different B deposition times are shown in Fig. 2, which also includes the case without a deposited B-layer, i.e. a Schottky contact directly on the substrate is formed. All diodes show near-ideal characteristics with ideality factors lower than about 1.02. The B deposition effectively decreases the saturation current and a transition is seen from the high-current Schottky to the low-current p^+n diode situation as the deposition time increases [8]. In addition, the series resistance that attenuates the current at high forward voltages decreases dramatically as the B deposition starts and a minimum is reached for the 20 s deposition.

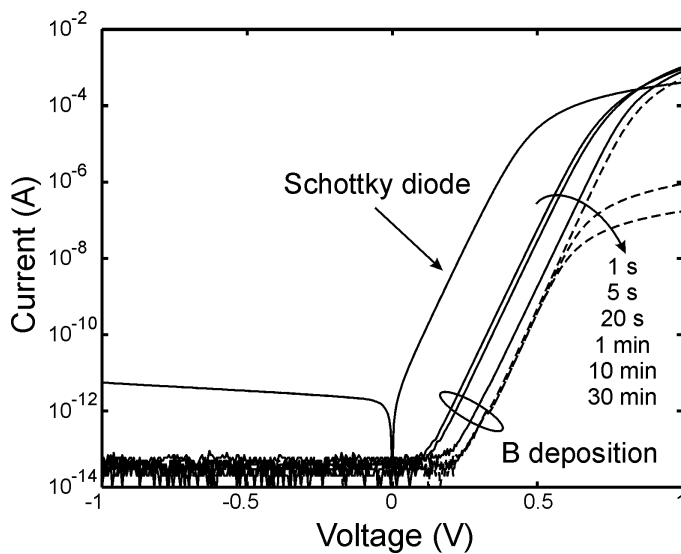


Fig. 2. Diode I-V characteristics for different B deposition times. The anode area is $2 \mu\text{m} \times 1 \mu\text{m}$.

This effect may be similar to what has been reported by Connelly *et al.* [9] where integration of sub-nm thick nitride layers was found to decrease the contact resistance of Schottky diodes. However, when a significant α -B layer has formed, the series resistance starts to increase dramatically. The influence of the α -B layer is also seen in the ideal diode current that decreases by a factor 4 from the 20 s to 1 min deposition. It is plausible that this effect is due to a low surface recombination velocity at the α -B/ B_xSi interface, since the extremely narrow B_xSi width would otherwise lead to a “Schottky-like” high current.

In Fig. 3 the bulk and perimeter effects of the boron-silicide layers are shown. In case of a Schottky diode (Fig. 3a), no linear dependence was achieved for any forward bias, and the relatively high current is dominated by the surface states at the silicon/oxide peripheral interface. Moreover, large variation of current level was found over the wafer.

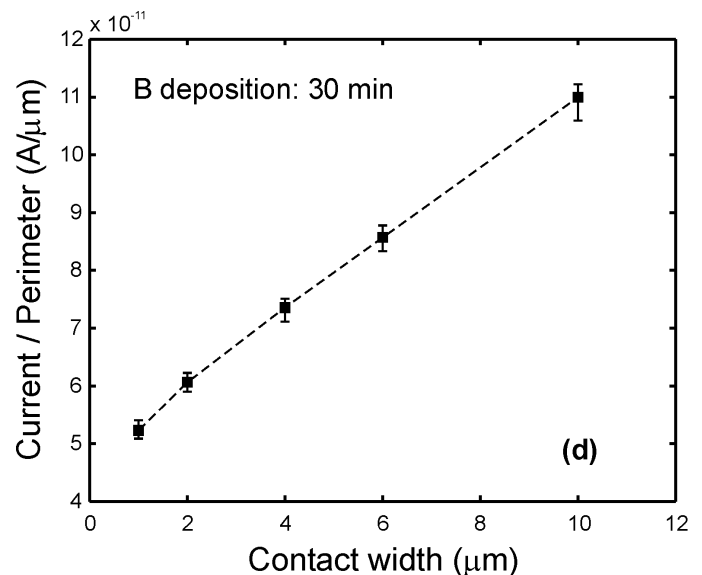
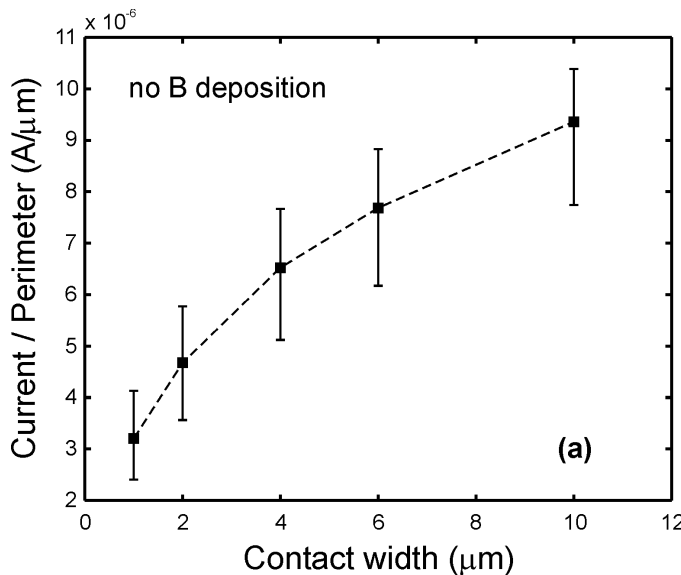
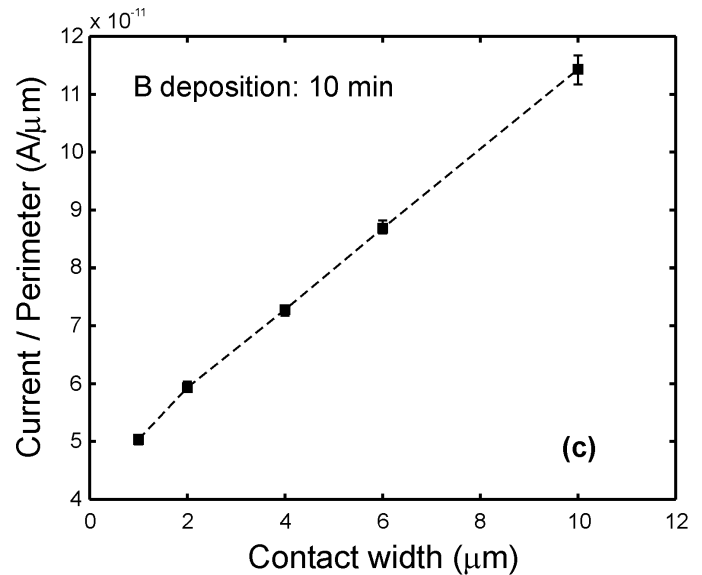
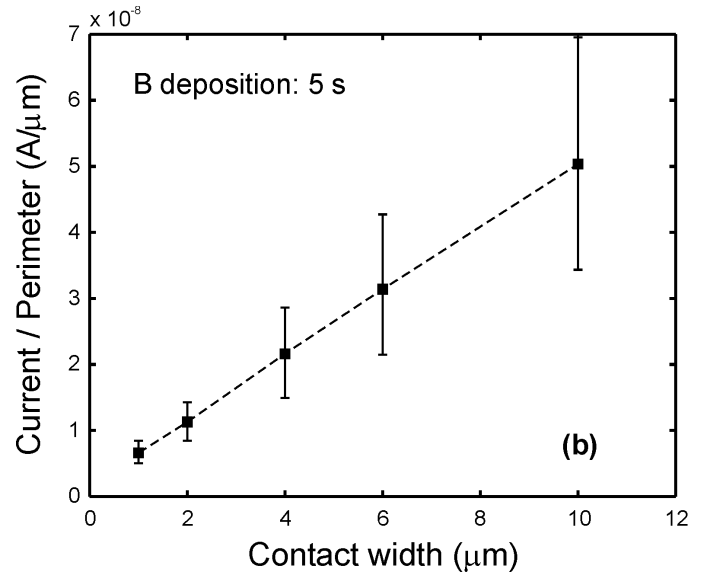


Fig. 3. Current/Perimeter vs. contact width for different B_2H_6 exposure times: (a) no B deposition, (b) 5 s, (c) 10 min, and (d) 30 min. The current levels correspond to forward bias voltage of 0.5 V. The measurements were performed in different positions of the wafer.

Instead, as the B deposition starts, the current components can be properly extracted according to (2). Significant reduction of bulk and perimeter currents is achieved during the first stage of the deposition and the spreading in the current levels is smaller for the 1 μm -wide structures. This clearly indicates that the B deposition is pattern dependent, in the manner that a higher sticking configuration takes place at the contact window edges. Moreover, the upper and lower limits in Fig. 3b correspond to diodes placed at the border and center of the wafer, respectively. While the perimeter current is almost equal, the bulk component is twice in the former case. This can be related to higher B_2H_6 exposure in the center of the wafer and more B atoms can chemically adsorb on the Si surface.

For long exposure uniform B-layers are formed over the wafer and perfect coverage is achieved for different diode sizes (Fig. 3c). It is worth noting that for a 30 min B deposition (Fig. 3d), the linear dependence of (2) is still valid, but the average of perimeter current increases while the bulk component slightly decreases. Probably, the level of boron-silicide/silicon interface might become lower and the effective peripheral area is increased. On the other hand, this does not significantly affect the current flowing through the vertical direction.

IV. CONCLUSION

In summary, it has been demonstrated that pure boron CVD deposition is a reproducible doping technique with which high-quality δ -doped boron-silicide layers with depths down to ~ 2 nm can be formed. The non-capped, as-deposited B_xSi layers are so thin that when used to form p^+n diodes the current level will be much higher than that of deeply diffused junctions. Adding the α -B layer will very effectively suppress the saturation current although the price is an undesirably higher series resistance. However, the α -B layer can be removed by cleaning and HF etching.

The uniformity of B-layers with respect to the contact pattern dependence has been investigated. The electrical results of diodes fabricated with the as-deposited α -B/ B_xSi stack have shown a more uniform B coverage for small size devices, since higher segregation takes place at the contact window edges. For long exposure, however, the uniformity is significantly improved. Such extremely shallow but efficient B-layers could be very interesting for use in numerous device applications.

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REFERENCES

- [1] J. Nishizawa, K. Aoki, and T. Akamine, "Ultrashallow, high doping of boron using molecular layer doping," *Appl. Phys. Lett.*, vol. 56, no. 14, pp. 1334–1335, Apr. 1990.
- [2] N. Saitoh, T. Akamine, K. Aoki, and Y. Kojima, "Composition and growth mechanisms of a boron layer formed using the molecular layer doping process," *Jpn. J. Appl. Phys.*, vol. 32, no. 10, pp. 4404–4407, Oct. 1993.
- [3] T. Inada, A. Kuranouchi, H. Hirano, T. Nakamura, Y. Kiyota, and T. Onai, "Formation of ultrashallow p^+ layers in silicon by thermal diffusion of boron and by subsequent rapid thermal annealing," *Appl. Phys. Lett.*, vol. 58, no. 16, pp. 1748–1750, Apr. 1991.
- [4] K.-S. Kim, Y.-H. Song, K.-T. Park, H. Kurino, T. Matsuura, K. Hane, and M. Koyanagi, "A novel doping technology for ultra-shallow junction fabrication: boron diffusion from boron-adsorbed layer by rapid thermal annealing," *Thin Solid Films*, vol. 369, pp. 207–212, July 2000.
- [5] T. Uchino, P. Ashburn, Y. Kiyota, and T. Shiba, "A CMOS-compatible rapid vapor-phase doping process for CMOS scaling," *IEEE Trans. Electron Devices*, vol. 51, no. 1, pp. 14–19, Jan. 2004.
- [6] F. Sarubbi, L. K. Nanver, T. L. M. Scholtes, "CVD delta-doped boron surface layers for ultra-shallow junction formation," in *Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS 2: New Materials, Processes, and Equipment*, 210th Meeting of The Electrochemical Society, *ECS Transactions*, vol. 3, no. 2, to be published.
- [7] H.-C. Tseng, F. M. Pan, and C. Y. Chang, "Characterization of boron silicide layer deposited by ultrahigh-vacuum chemical-vapor deposition," *J. Appl. Phys.*, vol. 80, no. 9, pp. 5377–5383, Nov. 1996.
- [8] M. L. Yu, D. J. Vitkavage, and B. S. Meyerson, "Doping reaction of PH_3 and B_2H_6 with Si(100)," *J. Appl. Phys.*, vol. 59, no. 12, pp. 4032–4037, June 1986.
- [9] D. Connelly, C. Faulkner, D. E. Grupp, and J. S. Harris, "A new route to zero-barrier metal source/drain MOSFETs," *IEEE Trans. Nanotechnology*, vol. 3, no. 1, pp. 98–104, March 2004.