A Wideband Flexible Power Upconverter for Software Defined Radios

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Abstract— **In a multi-standard radio transmitter it is common practice to use multiple narrowband PA's and filters: one for each standard and a switch before them. With the ever increasing number of different standards to be supported, this architecture becomes increasingly unpractical, as support for every new frequency band requires adding a dedicated external filter. Use of these discrete filters reduces the level of integration, thus making it difficult to realize low cost multi-radios on a single RF chip. This paper presents a polyphase multipath technique to relax or eliminate filters by canceling harmonics and sidebands. Using this technique, a wideband and flexible power upconverter with a clean output spectrum is designed in a 0.13µm CMOS for a software defined radio application. Additionally, a 33% duty cycle is used to cancel the problematic 3rd harmonic of the LO. The demonstrator prototype of the proposed power upconverter operates from DC to 2.4GHz with spurs <-40dBc over more than a decade in frequency. It can deliver 8dBm of power to a 100Ω load and consumes 228mW from a 1.2V supply. It uses no filters but only digital circuits and mixers, and no tuning of components is required.**

Index Terms—**Power upconverter, polyphase multipath circuits, distortion cancellation, nonlinear circuits**

I. INTRODUCTION

IN recent years, explosive growth in the wireless market has led to wireless transceiver terminals that have multiple applications and cover multiple standards. For consumer products, price and form factor are of primary importance, which is typically achieved by increasing the level of integration, and reducing the number of external discrete components. Generally in a wireless transmitter, filters are the main discrete components and those filters are considered inevitable to suppress the strong harmonics and sideband products generated during the mixing and amplification process.

Figure 1(a) shows a typical multi-standard transmitter, with multiple narrow-band Power Amplifiers (PA) which are limited in bandwidth by *dedicated filters*, one for each standard, selectable by a switch. With the ever increasing number of different standards to be supported, this architecture becomes increasingly unpractical, as support for every new frequency band requires *adding external dedicated components*. In this paper we aim at a much more flexible architecture as shown in Figure 1(b): one wideband integrated power upconverter with no dedicated external filters, with a digitally controlled output spectrum. If you insist on a visionary view: we aim for "the holy grail of software radio" [1, 2]. However, dedicated filters are there for a good reason. If we can significantly reduce unwanted spectral components via other more flexible techniques than frequency selective filters, this is likely to be a crucial step to new more flexible transmitter architectures. A recent step in this direction is the use of zero-order hold filtering in a mixer-DAC [3] to reduce DAC related spurs. However, this approach doesn't address the problem of mixer harmonics around odd LO-harmonics, caused by multiplication with a square-wave LO-signal (hard switching mixer). A harmonic rejection mixer canceling the third and fifth harmonics [4] does relax analog filter requirements. In this paper, we exploit the practical potential of the recently proposed polyphase multipath circuit theory [5], to reduce or even completely eliminate filters by canceling a large multitude of harmonics and sidebands. We apply the technique to realize a wideband *filter-less* power upconverter, using only digital circuits and switched transconductor mixers [6] [7], for possible future software defined radio applications in CMOS.

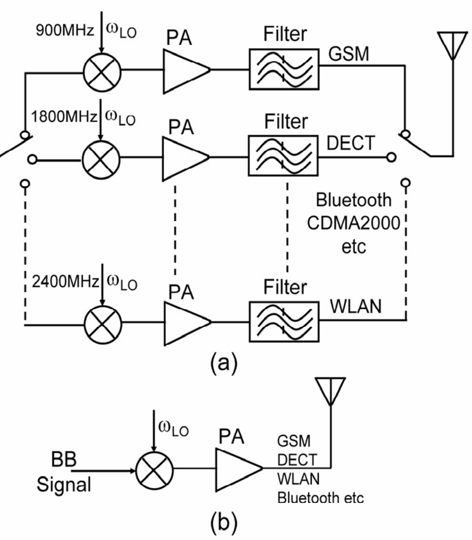

Figure 1(a) Conventional multi-standard transmitter architecture (b) Dream; one flexible upconverter, no filters.

II. POLYPHASE MULTIPATH TECHNIQUE

A. *Principle of Harmonic Cancellation*

Figure 2 shows a nonlinear circuit producing harmonics. Traditionally, such harmonics are removed using bandpass filters. Figure 2b shows a plyphase multipath circuit that also removes harmonics [5]. The basic idea is to divide the nonlinear circuit in Figure 2(a) into ‘n’ equal smaller pieces, and apply a phase shift ‘(i-1)×2π/n’ before and behind the nonlinear circuit in each path ‘i’, with equal but opposite phase. Figure 2(b) shows a polyphase n-path circuit consisting of n identical memory-less weakly nonlinear circuits [5]. An input sine wave results in 1st order harmonic components produced by the n paths, which are *in* phase and add constructively. However, nonlinearities produce higher harmonics with a phase proportional to the order of the harmonic, and the contributions of different paths can cancel each other except for the (j×n+1)th harmonic, where j is an integer [5]. Similar conclusions hold for inter-modulation products. In general, if the number of paths is higher, more harmonics and sideband products can be cancelled.

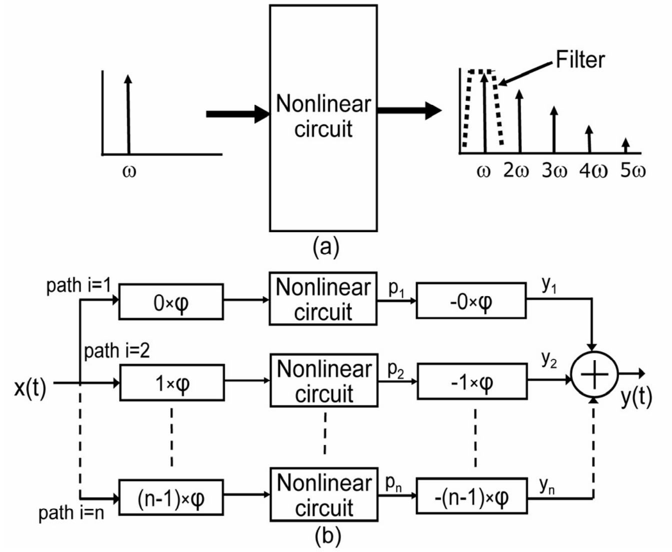

Figure 2(a) Nonlinear Circuit producing harmonics which are traditionally removed using a band-pass filter. b) Polyphase multipath circuits concept

B. *Polyphase 3-path circuit example*

A system with three paths is shown in Figure 3. In this case, phase shifts of 0°, 120° and 240° are added before the nonlinear circuits in path 1, 2 and 3 respectively, and equal but opposite phase shifts (0°, -120° and -240°) are introduced behind the nonlinear circuits. Since the phase rotation for the kth harmonic is k times the input phase, the fundamental component, the second harmonic and the third harmonic will have phase shifts of [0°, 120°, 240°], [0°, 240°, 120°] and [0°, 0°, 0°] respectively at the output of the nonlinear blocks in path 1, 2 and 3. Figure 4(a) shows how the phases of the harmonics at the output of each path combine. The fundamental components add up in phase, while the vectors for the second and third harmonics create a “balanced structure” at the output, resulting in a zero sum (cancellation). However, the fourth harmonic components align in phase again, and will add up like the fundamental. Figure 4(b) shows that the 2nd, 3rd, 5th, 6th, 8th etc harmonics are cancelled and the first non-cancelled is the fourth with a 3-path system. Similarly for a 4-path system the first non-cancelled harmonic will be the fifth harmonic and in general for the n-path system the (n+1)th harmonic is the first non-cancelled harmonic.

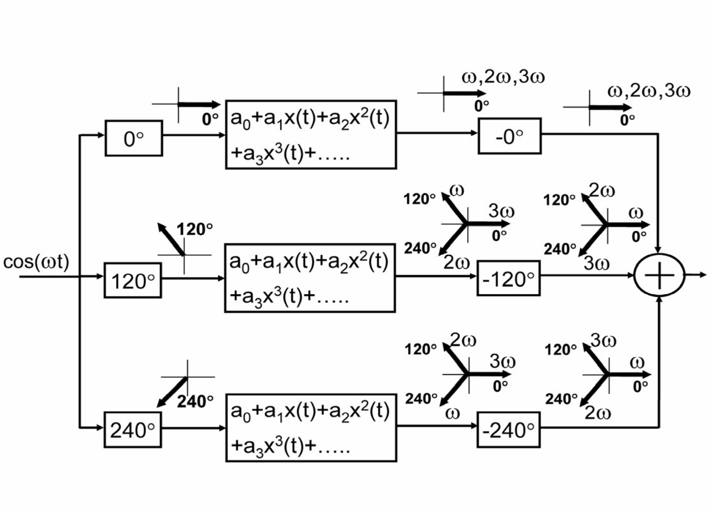

Figure 3 Polyphase 3-path circuit

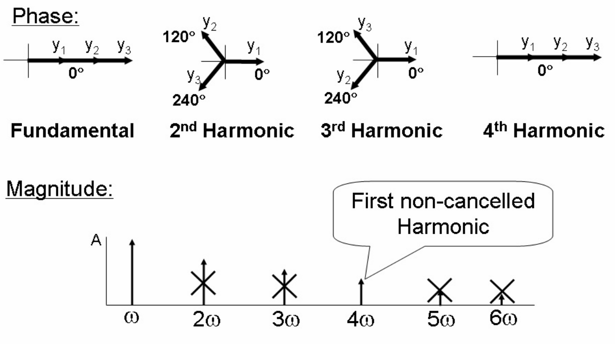

Figure 4 Output of the 3-path circuit in Figure 3: (a) phasor diagrams and (b) spectral plot

III. MIXER: PHASE AND FREQUENCY SHIFTER

To realize wideband harmonic rejection using a polyphase multi-path system, we need very wideband phase shifters before and behind the nonlinearity. This is because all phase shifters need to have a constant phase shift over all relevant frequencies involved in the cancellation process. In a DSP intensive radio transmitter, digital signal processing techniques can be exploited to realize phase shifters before D/A conversion and nonlinear power amplification. Therefore, a good solution can be to shift this polyphase generation problem to the digital domain, and use a DSP followed by multiple DACs to generate multi-phase baseband signals. However, behind the nonlinear element we are in the analog domain, and there can be many harmonics. In that case cancellation of a multitude of harmonics requires a constant phase shift over many octaves of frequency.

A very wideband phase shifter can be implemented with a mixer, since a mixer conveys phase information of both the “baseband” (BB) and “Local Oscillator” (LO) port to the RF-output. Whatever phase is added to the LO signal, it will appear at the output of the mixer. So by replacing the second set of phase shifters in Fig. 3 with mixers as shown in Fig.5, we can achieve a wideband phase shift but simultaneously we will have up-conversion. As up-conversion is desired in a wireless transmitter circuit anyway, this fits very nicely to our goal.

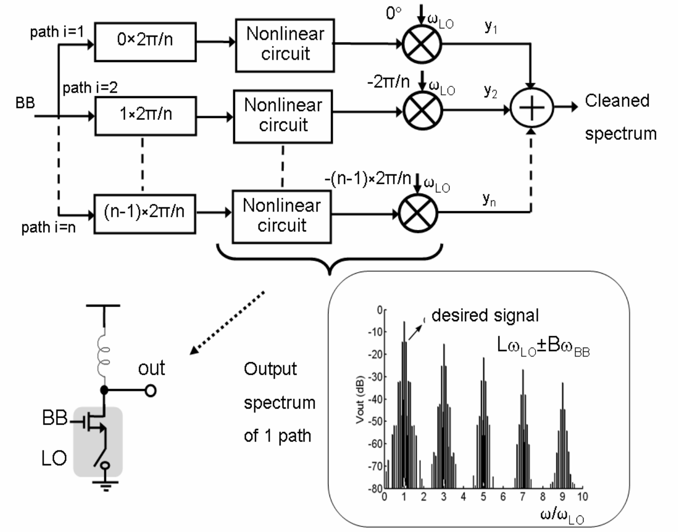

Figure 5. Polyphase Multi-path transmitter using mixers as phase shifter. Each section consists of a single transistor with switch. A single section has an output spectrum with countless harmonics and sidebands

However, a mixer produces both a sum frequency and a difference frequency, and usually only one of these is the wanted signal, while the other (“the image”) needs to be suppressed. Moreover, flexible frequency synthesizers rely on digital dividers and generally produce square-wave signals. For power efficiency reasons it is also highly desired to use a switching mixer and a large BB-signal swing, e.g. a single transistor with switch as shown in Fig. 5. However, the output spectrum for one path as shown in Figure 5 will now contain a forest of harmonics and sidebands at frequencies $L\omega_{LO} \pm B\omega_{BB}$, where L and B are integers, due to the multiplication of the square wave LO with the baseband input signal BB, and the nonlinearity of the circuit. In the next section we will see how we can exploit the polyphase multipath technique to cancel almost all the unwanted components.

IV. FILTERLESS POWER UPCONVERTER

Figure 6 shows the structure of a Power Upconverter (PU) as finally implemented on chip, combining the mixer and power amplifier functionality, with 18 paths contributing output current to the load. Since the wanted output signals all add up in phase, the total area and power of the PU-core is not increased by dividing it into 18 sections. Each path consists of a switched transconductor mixer [6]: a baseband (BB) signal is applied to a differential pair acting as transconductor, activated by a local oscillator signal (LO) driving a grounded switch. By doing so, the phase of the LO is added to the phase of the BB signal. The different LO-phases are generated on chip while the 18 BB-signals (9 differential) are generated off-chip, but should ultimately be generated by a BB processor with DACs.

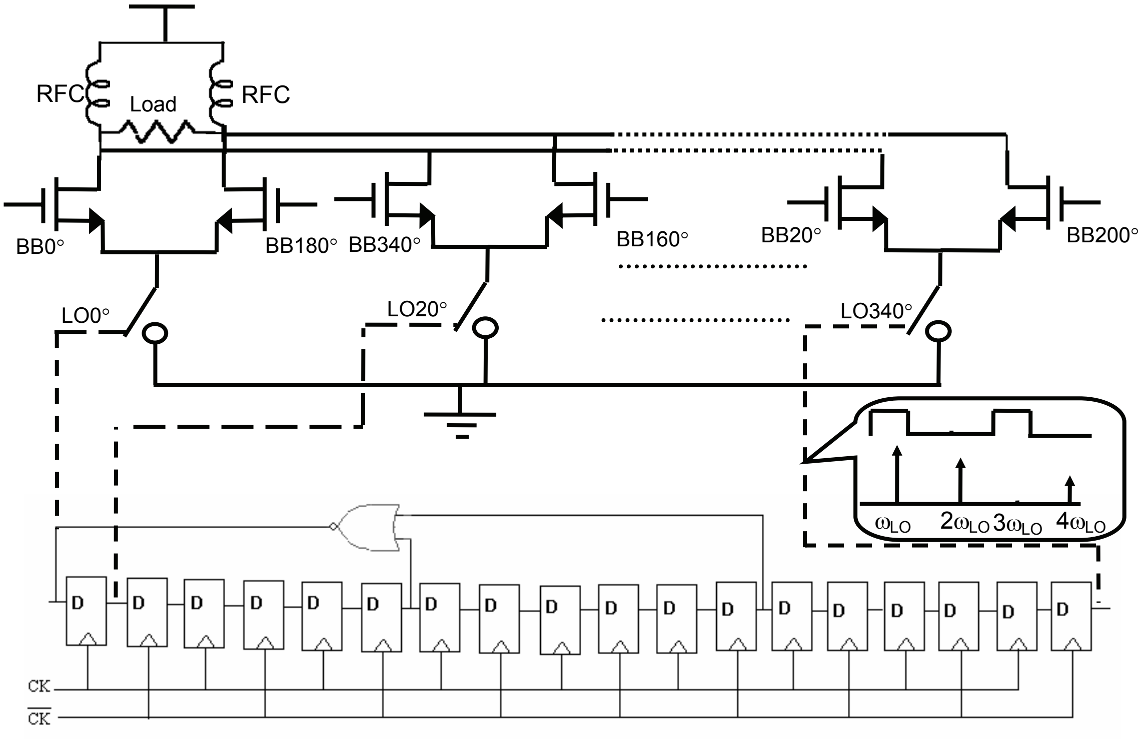

Figure 6 power upconverter using polyphase 18-path architecture

Table 1 The cancellation of unwanted products in a 18-path PU with different technicques: M=cancelled by multipath; D=cancelled by 33% duty cycle, B= cancelled by Balancing (Differential)

m ⟶	-4	-3	-2	-1	0	1	2	3	4
$1\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M		BM	M	BM
$2\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	B	M	BM
$3\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	D	BMD
$4\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	B
$5\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$6\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$7\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$8\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$9\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$10\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$11\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$12\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$13\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$14\omega_{LO}+m\omega_{BB}$	B	M	BM	M	M	M	BM	M	BM
$15\omega_{LO}+m\omega_{BB}$	BMD	D	BMD	MD	M	MD	BMD	MD	BMD
$16\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	BM
$17\omega_{LO}+m\omega_{BB}$	BM	M	BM		M	M	BM	M	BM

M=cancelled by multi-path, D=cancelled by 33% duty cycle, B=cancelled by balancing

Using a square wave LO signal and large output swing is good for the efficiency, but also produces many harmonics and sidebands at frequencies $k\omega_{LO}\pm m\omega_{bb}$, where k,m are integers. The products that are cancelled by the multipath technique are indicated by 'M' in the Table I for an 18-path system. However, products like $2\omega_{LO}+2\omega_{bb}$, $3\omega_{LO}+3\omega_{bb}$, $4\omega_{LO}+4\omega_{bb}$ etc have a phase of 0° at the output of each path and can not be cancelled by the multipath technique [5]. Among these non-cancelled harmonics, the $2\omega_{LO}+2\omega_{bb}$, $4\omega_{LO}+4\omega_{bb}$ etc are cancelled by the use of a differential transconductor ("B" in Table I). To eliminate the strong $3\omega_{LO}+3\omega_{bb}$ harmonic, we use a LO with 1/3 duty cycle, so that the 3rd harmonic term disappears from the Fourier series expansion ("D" in Table I). Other non-cancelled products like $5\omega_{LO}+5\omega_{bb}$, $7\omega_{LO}+7\omega_{bb}$ etc are typically smaller than residual products caused by inaccuracies like device and phase mismatch.

IV MEASUREMENT RESULTS

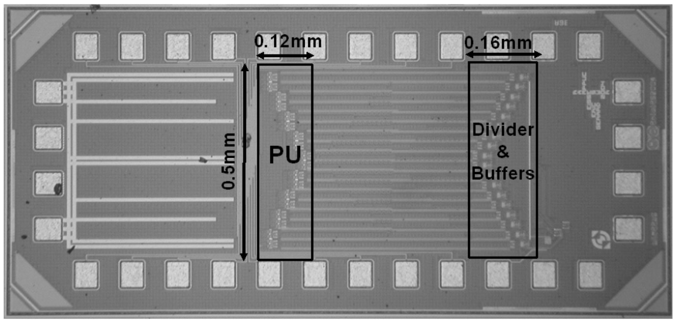

Figure 7 Demonstrator Chip Micrograph

A demonstrator chip of the proposed polyphase multipath power upconverter was designed and fabricated in a 0.13-µm CMOS process. The chip has a standard supply voltage of 1.2V and has an option to select a 6- and 18-path operation mode. The die micrograph is shown in Figure 7. The chip is clearly bond pad limited for reasons of experimental flexibility. The active area of the two rectangular blocks, PU and dividers and buffers, shown in the Figure 7, is only 0.14mm^2. Between them are just wires to connect them. The Baseband bandwidth is 0 to 50 MHz, but the input signal was arbitrarily chosen at 100 kHz, while varying the LO-frequency between 0 and 2.4 GHz. No filters are used at the output. The RF choke (RFC in Figure 6) and load are off chip. The RF choke is used to increase the drain efficiency of the PU as it is used in all power amplifier designs. It helps to increase the output swing by two times. RF chokes just bias the PU at the supply voltage and are not filters. Operating each individual mixer at the 1dB compression point, the PU is designed for large output swing ($2.54V_{\_pp\_diff}$) at the output to get a good efficiency.

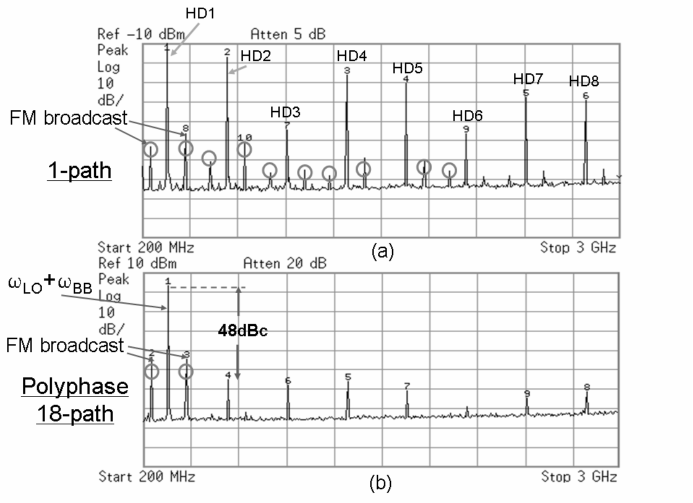

Figure 8 Output spectrum (a) before cancellation (b) after cancellation

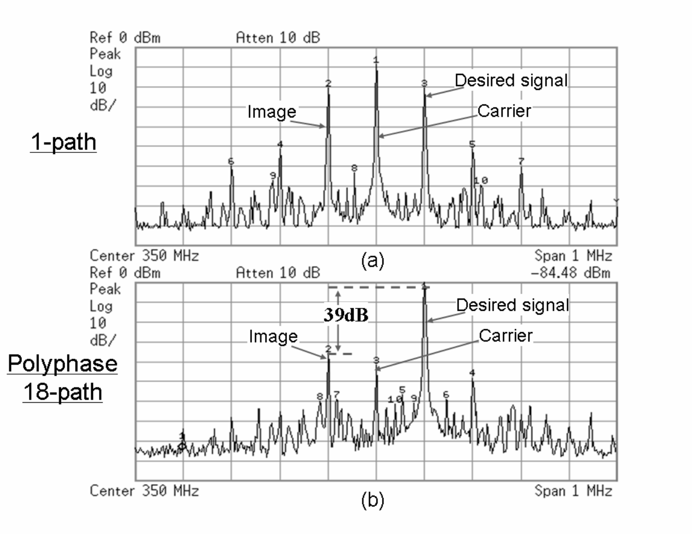

Figure 9 The LO leakage and image rejection performance (a) before cancellation (b) after cancellation

Figure 8 shows the output frequency spectrum (350MHz carrier) before and after the cancellation for a single path (upper) and multipath circuit (lower figure). Please note that the unfortunate FM radio spurs that are modulated with our output signal, are due to a 100.0MHz FM radio broadcast transmitter on the roof of our building. The suppression of the products having 3rd, 6th, 9th etc harmonics of LO in Figure 8 (a) is due to the 1/3 duty cycle of the LO signal. All the harmonic products are effectively suppressed to -48dBc.

Figure 9 (a) shows the measured upconverted signal (desired signal), its image and LO feed-through (carrier) with only one path. The suppression of the image and the LO feed-through due to the polyphase 18-path circuit is shown in Figure 9(b). All the sideband products are suppressed to 39dB below the desired signal.

Figure 10 shows results of the harmonic rejection over the entire 2.4GHz band of LO-frequencies, and also for image rejection and LO-leakage. The LO frequency is varied from 30 MHz to 800MHz for the 18-path PU and the strongest cancelled harmonics or sidebands are measured and plotted. For the 6-path PU this was also done, but now by varying the LO frequency from 30 MHz to 2.4 GHz. This figure shows that the worst case harmonic spur is smaller than -40 dBc in the entire frequency range. The maximum clock frequency at which the circuit works is 7.2GHz. The maximum LO frequency is thus 2.4 GHz for 6-path mode and 800 MHz for 18-path mode, as the clock frequency is divided 3 and 9 times respectively.

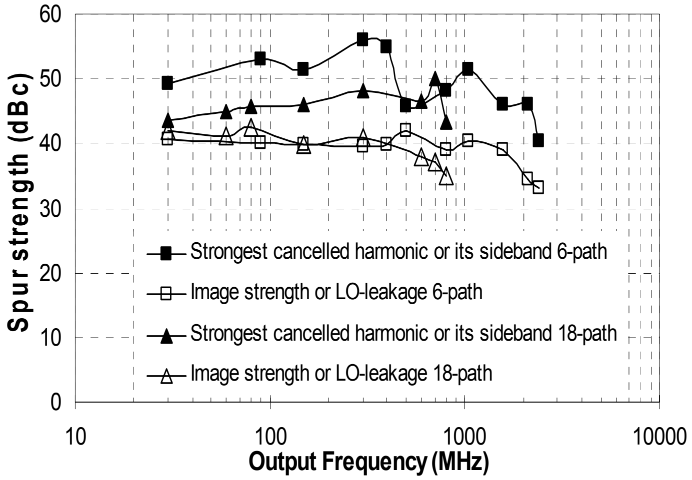

Figure 10 Measured suppression of undesired products over the full output frequency range

The total power consumption of the chip is 228mW; 156mW by the digital circuits (dividers and buffers) and 72mW by the PU core. High power consumption of the digital circuit is due to the brute-force multiple phase generation via 9x higher frequency, and the use of high bias currents in the current mode logic. It can significantly be reduced in a real application using for instance a DLL running at the LO-frequency. The magnitude of the cancelled harmonics depends on matching, both in time and magnitude. Identical paths and loads are used to reduce the phase mismatch between the paths. We also measured multiple samples of the IC and all 20 samples showed very similar behavior within 1-2dB.

V. CONCLUSION

A multipath approach in combination with a LO with 1/3 duty cycle results in a power upconverter with a clean output spectrum. It operates from DC to 2.4GHz with worst case harmonic rejection of -40dBc. It uses no filters, but only digital blocks and switched transconductor mixers, enabling this design to fit in future Software Defined Radio architectures. Frequency range limitation in the clock generator will be relaxed in newer CMOS technologies.

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