

High-aspect-ratio Bulk Micromachined Vias Contacts

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Abstract – This paper presents a process to form high-aspect-ratio via contact based on bulk micromachining technology. A combination of wet anisotropic etching and deep RIE of silicon is used to form the through-wafer holes. The approach followed reduces area consumption and preserve mechanical stability of the wafer. The deposition of a dielectric layer inside these high aspect-ratio vias is investigated. The thickness and uniformity versus via depth is evaluated. Finally, a modified Cu electroplating process is applied for the metallization of the through-wafer vias.

Keyword – Through-wafer interconnects, High-aspect-ratio vias, bulk micromachining.

I. INTRODUCTION

The emerging three-dimensional (3D) interconnect technology is a driving force for the realization of 3D integrated circuits, 3D packaging and advanced microelectromechanical system (MEMS). Stacking chips and connecting them through vias on the chips results in higher performance and smaller form factors. Furthermore, through wafer interconnects bring a possibility of stacking dissimilar ICs in the same device or stacked chip -- not just logic and memory, but optical ICs and CMOS, for example [1]. The shorter interconnect lengths associated with through wafer vias could increase device speed, provide lower power consumption, lower noise and reduce crosstalk.

In this paper, we present a process developed to realize electrical connections through the silicon substrate. Bulk micromachining technology is used to fabricate high-aspect-ratio (HAR) via contacts. The goal is to form through-wafer electrical connection based on 100-200 μm deep vias, with dimensions varying between 10 and 100 μm , through the bulk silicon substrate. Such vias can serve as connection from front to sub-surface metallization and to form Faraday cage shields in the substrate. The method to fabricate vias is a combination of anisotropic wet and dry etching of silicon. The wet

etching step is used to locally thin down the wafer while the dry etching step forms vias in these membranes. In this way, through-wafer high-aspect ratio vias are formed while the wafer mechanical stability is maintained. Further, the deposition of an insulation layer inside the vias, a crucial step in the formation of through-wafer interconnects, is addressed. Next to thermal oxidation and LPCVD of silicon oxide and silicon nitride, especially PECVD of silicon nitride is investigated. Results related to conformality and uniformity of the PECVD SiN coating in these high aspect ratio vias are presented and suggestions on alternative coating approaches for higher aspect ratio structures are discussed as well.

II. VIA FORMATION

Two methods to form HAR vias using wafer thinning or two-step wet etch have been reported [2]. Both methods result in either difficulty in wafer handling and processing (thin wafer) or consumption of large area (two-step wet etch). In this paper, the formation of HAR vias uses a combination of silicon wet etching and deep dry etching. The first etch step is used to locally remove the bulk silicon and thus create a silicon membrane of 100-200 μm -thick. The second etch step is employed to open the through-wafer via. As the wafers are locally thinned down, they are obviously expected to have a higher mechanical stability than uniformly thinned wafers. Moreover, the pillar-shaped vias formed by dry etching occupy less space than cone-shaped vias formed by wet etching.

Wet etching of Si using alkaline solution, as an etchant is a widely used method in MEMS fabrication. The etching is crystal orientation dependent and the etch rate can be well controlled by solution concentration and temperature. Therefore here we focus only on the deep dry etching process. Details on the anisotropic wet etch step can be found in [2].

Deep dry etching (DRIE) of silicon using the Bosch process is performed on an Adixen ASM 100 system. Etch depths of up to 300 – 400µm deep and aspect ratio of 1:20 can be obtained, with the proper process parameter adjustments. However when openings of different size are present on the wafer, a difference in etch rate, that is even more significant as the depth of the via increases, is observed [3]. This effect is called Aspect Ratio Dependent Etching (ARDE), i.e.

$$ARDE = (ER_{Max} - ER_{Min}) / ER_{Max}$$

As reported by Adixen, the ARDE observed is between 45%-18%. Process optimization can reduce the ARDE effect. However, the ARDE depends a lot on the dimension and the amount of open area on the wafer. Another solution is to use an oxide etch stop layer like a buried layer of SOI. Over-etching time can then be used to compensate the slow etch rate in smaller openings. However, if the difference in etch rate is too high, over-etching in large structure will cause notching. Therefore it is preferable to dry etch structures with comparable dimension. Figure 1a is a schematic drawing of the process flow to form vias with comparable dimensions.

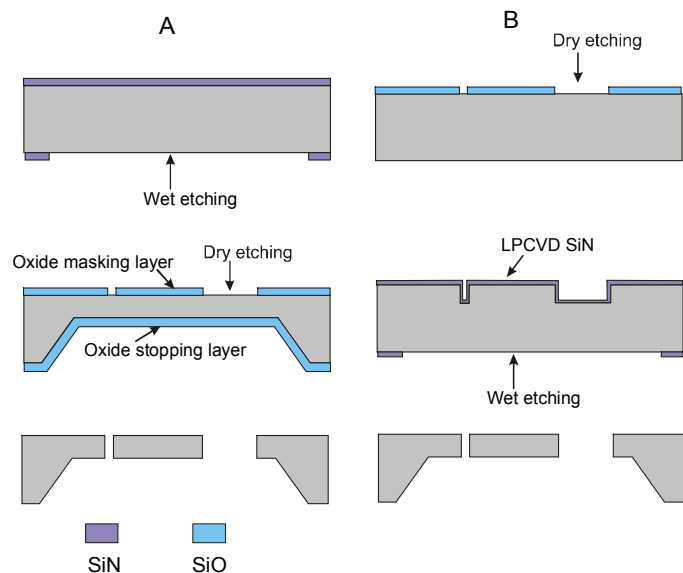


Figure 1. Vias formation process: A) for comparable vias dimensions; B) for vias with large variation in dimensions

In this case the wet etching is applied first followed by dry etching. If the dimensions of the vias are very different, the process flow depicted in Fig.1b is proposed as a more suitable alternative to fabricate well-controlled via without notching. In this process, dry etching is first performed on the frontside. A thin LPCVD SiN layer is then deposited to cover all the vias and to act as a wet etch stopping layer. Wet etching is carried out from

backside until it reaches the SiN stopping layer. The SiN layer will protect the shape of larger vias during the over etching required to reach the smaller ones.

In Fig 2, a SEM picture of several vias with lateral dimension of 50, 40 and 30 µm which are dry etched from the frontside are shown. The same vias looking from the backside of the wafer over the 400µm-deep cavity are illustrated in fig 3.

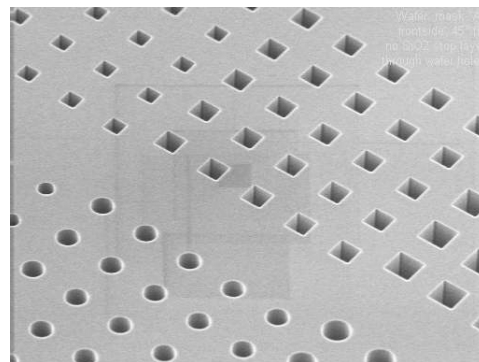


Figure 2. SEM picture of 50, 40 and 30µm wide vias dry etched (front side view)

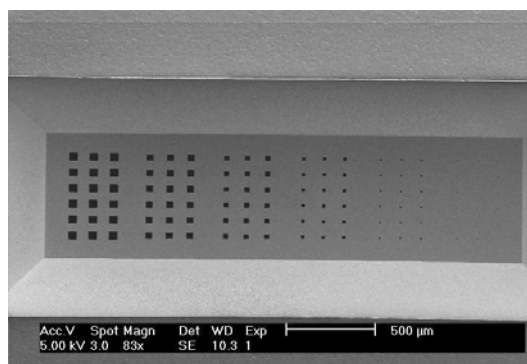


Figure 3. An array of through-wafer vias in a 400 µm-deep cavity viewed from the backside of the wafer

The ARDE can be clearly seen in fig.4 where the cross-section of vias with a width varying from 5µm to 50µm are shown. The decrease of etch rate for the narrower structures is clearly visible. The differences in etch depth as a function of via size is plotted in fig 5. The etch rate difference between the 5µm vias and 50 µm vias is 44%. For trenches, the ARDE is less pronounced. In fact for the larger trenches with the same length (1mm) only 8% difference is observed between a 900µm wide and 100µm wide trenches. This is due to the fact that despite the different dimensions, the variation in the open areas of these trenches is not as significant as for vias, thus resulting in a negligible variation of the etch rate.

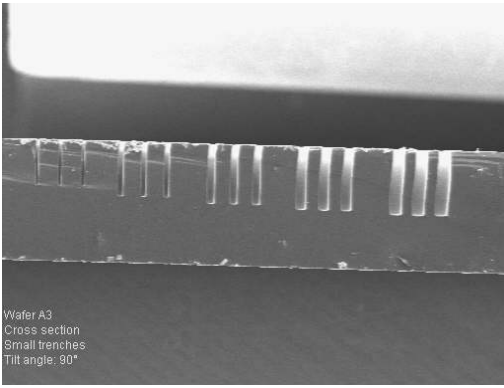


Figure 4. Cross-section of vias ranging from a width of 10 μm to 50 μm . The difference in etch rate vs size is clearly visible.

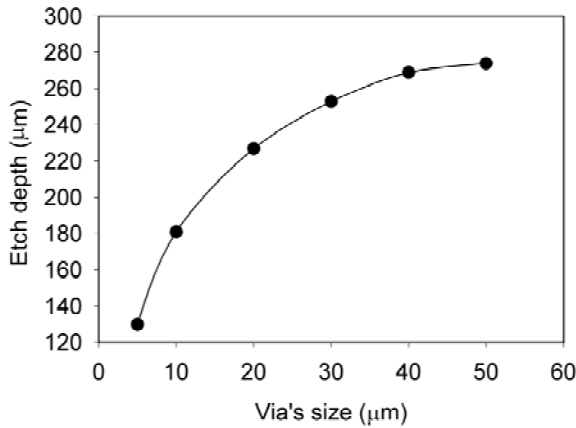


Figure 5. The etch depth dependence on via's size

III. DEPOSITION OF INSULATION LAYER IN THE VIAS

Deposition of an insulation layer in the vias is also an important step in the realization of through-wafer interconnects. Because of the high-aspect-ratio of the through-wafer vias, it will be difficult to apply Al metallization. Therefore, Cu metallization will be used for this process. This means that, the insulating layer should not only be a dielectric but also should act as a barrier layer preventing the diffusion of Cu into the substrate. For this reason, silicon nitride is chosen as an insulation layer [4].

Both LPCVD and PECVD SiN deposition could be used. The LPCVD layer gives a very conformal coating and a good quality layer. However it requires a higher deposition temperature. PECVD SiN although less conformal than LPCVD, uses a lower deposition

temperature ($\leq 400^\circ\text{C}$), which is suitable for CMOS compatible processing.

A test deposition of 500nm PECVD SiN was carried out on wafers containing vias and trenches of different sizes. After deposition the wafers are cut and inspected with a SEM to measure the thickness of the dielectric at the top, middle and the bottom of the trenches.

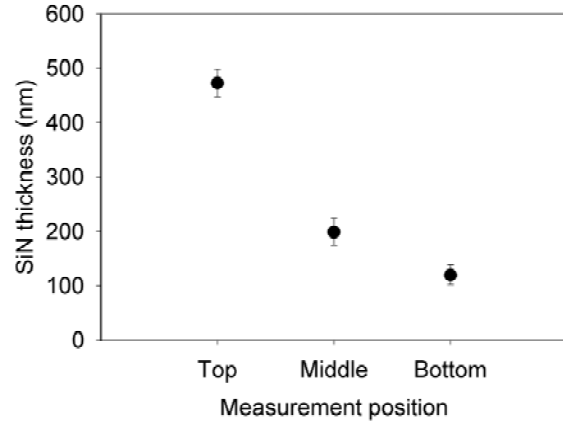


Figure 6. Thickness of SiN layer deposited by PECVD measured at the top, middle and bottom of the (10 μm wide, 1000 μm long and 150 μm deep) trenches

The SiN thickness is getting thinner when going deeper into the trenches. Measurements for a 10 μm wide trench are reported in fig. 6. The thickness at the bottom of the trench is only 25% of that at the top corner. Obviously, for vias (squares or round) or for deeper trenches, it might be quite difficult to get a good coverage of SiN. In case of the through-wafer vias, deposition of SiN on both sides of the wafer can improve the SiN coverage in the small vias. In this case, SiN layer at the middle of the vias will be thinner than other positions but the overall coating is acceptable.

IV. FILLING VIAS USING COPPER PLATING

A plating method recently developed to fill HAR through-wafer via with copper, called “bottom up plating” was employed [5]. It is usually preferable for small HAR vias, because it does not need the deposition of seed layer over the sidewall of the via. The scheme for this process is illustrated in fig.7.

After the deep dry etching step to form the HAR vias, a nitride insulation layer is deposited on both sides of the wafer and inside the vias. A 40nm Ti/TiN adhesion layer was deposited on both sides of the wafer. Then a 300nm Cu seed layer is sputtered on the backside of the wafer. By sputtering, copper islands are formed near the bottom of the vias but it doesn't reach deeply inside the vias. This can facilitate the quickly growing of copper that leads to partially blocking the bottom of the vias, which

is desirable for the bottom-up electroplating. Lithography is applied to define metal structures on this side and

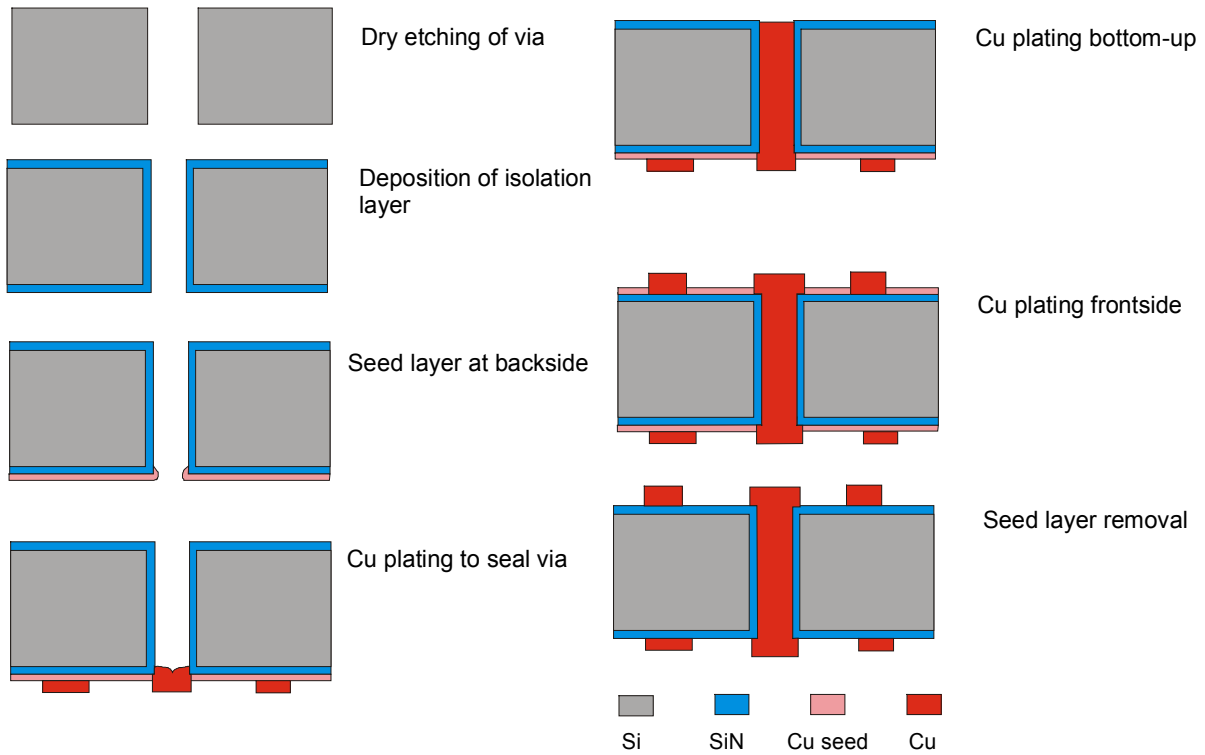


Figure 7. Process flow for via filling with Cu and devices fabrication at both sides of the wafer.

electroplating of Cu is carried out to increase the metal thickness of these structures. During this step, Cu grows inside the vias and blocks the bottom of the vias. Once reached the desired thickness of the Cu structures on the wafer backside, a photoresist layer is applied on this side to protect the Cu structures from undesirable overgrowth, while bottom-up copper electroplating is conducted until the vias are completely filled. Through-wafer copper plugs are thus obtained.

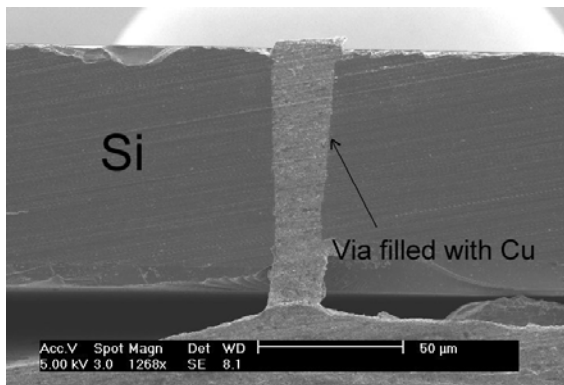


Figure 8. A 20 μm wide, 120 μm deep via filled with copper using the copper bottom-up plating technique

A photoresist layer is now applied on the frontside followed by a Cu-plating step if metal structures are needed on the wafer frontside as well. A HAR via completely filled with Cu is shown in fig 8. Fig 9 is a SEM photograph of the top view of an array of 20 μm wide vias fabricated by wet and dry etching. A close-up illustrates the same vias after copper bottom up plating in fig 10. As can be seen in these figures, all the vias are uniformly filled with copper.

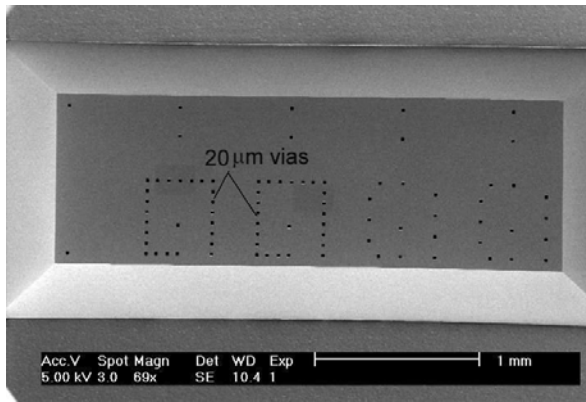


Figure 9. Arrays of 20 μ m vias using wet etch and dry etching

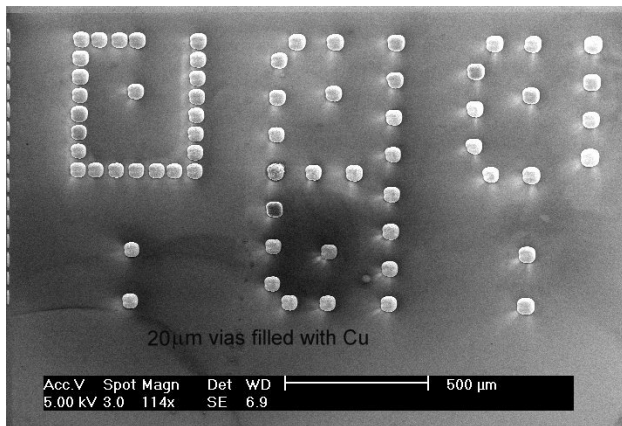


Figure 10. Close-up of 20 μ m vias filled with Cu.

V. CONCLUSIONS

A combination of wet and dry silicon etching is employed to fabricate HAR vias. Two processes (one for vias with large differences in dimension and one for vias with comparable dimensions) have been developed to take into account the non-uniformity effects related to via size and distribution during the deep dry etching. PECVD SiN layer can be used as isolation/barrier layer inside vias. The effect of coating non-uniformity and conformal coating are investigated. Suggestions to improve control on thickness throughout the via are presented. A process for the metallization of the through-wafer vias, the bottom-up Cu plating process, is tested and the initial results achieved are quite promising. Attempts to further reduce ARDE, as well as alternative coating methods for dielectric layers inside HAR vias are currently under investigation.

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REFERENCES

- [1] J.Chappell, "3D Interconnect Technology coming to light", Electronics News, April 2004.
- [2] Pham Phuong Nga, "Silicon Micromachining for RF technology", PhD thesis, Delft University of Technology 2003, ISBN 90-6734-235-1. Chapter 3
- [3] A. Rickard, M. Mc Nie, "Characterisation and optimisation of deep dry etching for MEMS applications", Proc. SPIE "Microelectronic & MEMS", Edingurgh (UK), 2001.
- [4] G.Adema et all, IEEE Trans. On Comp, Hybrids, and Manuf. Tech. 16, 53, (1993).
- [5] N.T.Nguyen, E.Boellaard, N.P.Pham, V.G.Kutchoukov, G.Craciun, P.M.Sarro, "Through-wafer copper electroplating for 3-D interconnects", J.Micromech.Microeng. 12 (2002), pp 395-399.