

# Noise Optimization of Integrated Switched-Capacitor Front-Ends with Wide Dynamic Range

A. Heidary and G.C.M. Meijer

**Abstract:** This paper presents the noise optimization of a switched-capacitor front-ends circuit with wide dynamic range for capacitive sensor. The interface is able to measure low capacitance value in the order of Pico farads, which is implemented with a modified relaxation oscillator. In order to modify the oscillator for better noise performance, first the noise performance of simple relaxation oscillator has been analyzed. For experimental evaluation of the interface, the chip has been designed in a  $0.7\mu$  standard CMOS technology process. Measurement will be performed in the near future.

**Index Terms**—Capacitive sensors, Dynamic range, Noise, Optimization, Resolution

## I. INTRODUCTION

Capacitive sensors are widely applied in cascade-sensor systems, such as liquid-level gages, pressure meters, accelerometers, and precision positioners, in which physical, chemical or mechanical quantities are converted into a capacitance value and further processed by an electronic circuit, the modifier. In these applications, the capacitances to be measured are often in the range of 0.1-10 pF and normally, a high resolution (low noise) is required.

Electronic interfaces whose output signals are period modulated are very attractive because they can directly be interfaced to a microcontroller. Such interface can easily be implemented with a simple relaxation oscillator and applied to capacitive sensor [1].

Always the random error (noise) can be averaged out. Therefore by increasing the measurement time we can increase the resolution. The main goal is increasing the resolution without increasing measurement time, or decreasing measurement time without decreasing the resolution. And improving the noise performance of the interface circuit can only do this.

In order to increase the noise performance of the relaxation oscillator, first we analyze the noise performance of simple

relaxation oscillator. From that we can find some clue to improve its noise performance. Then we try to change the oscillator, based on our finding.

## II. INTERFACE SYSTEM

Fig. 1-a shows the capacitive sensor interface with implemented second order switched-capacitor filter [2]. Also some important signals are shown in Fig. 1-b.

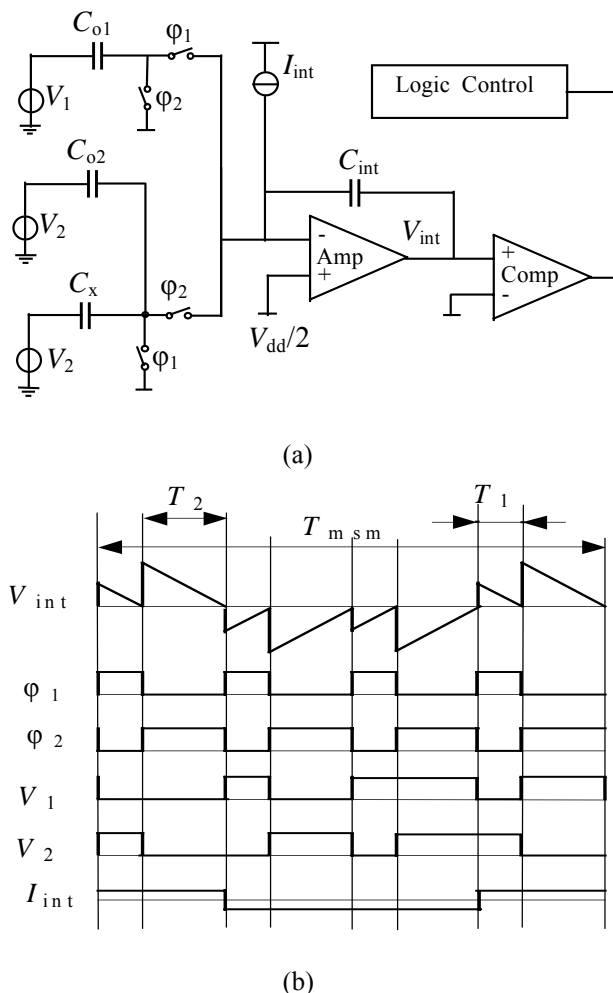


Fig. 1. (a) Capacitive sensor interface and (b) some relevant signals

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One measurement period ( $T_{\text{msm}}$ ), is equal [1]:

$$T_{\text{msm}} = 4 \frac{\widehat{V}C_x + \widehat{V}(C_{o1} + C_{o2})}{\widehat{I}_{\text{int}}} \quad (1)$$

Where  $\widehat{V}$  is the peak-to-peak amplitude of  $V_1$  and  $V_2$  and the best selection is  $\widehat{V} = V_{\text{DD}}$ . Also  $\widehat{I}_{\text{int}}$  is the amplitude of  $I_{\text{int}}$ .

In order to increase the resolution a divider (low pass filter) will be used. This divider also is useful for decreasing the quantization noise of period reading by a counter.

To get some idea about the value of capacitance we show an example below.

**Example1:** With  $C_{x,\text{max}}=10\text{pF}$  and  $V_{\text{DD}}=5\text{V}$ , we select  $C_{o1}$ ,  $C_{o2}$  and  $C_{\text{int}}$  for the step of  $0.5\text{V}$  of integrator output for  $\phi_1$  and  $2\text{V}$  for  $\phi_2$  with  $C_{x,\text{max}}$ . This can guaranty the linearity of integrator and having good dynamic range. The result will be:  $C_{o1}=C_{o2}=3.3\text{ pF}$  and  $C_{\text{int}}=33\text{ pF}$ .

### III. NOISE ANALYSIS

Here we consider two important noise sources,  $u_{\text{ni}}$  “the equivalent voltage noise of the amplifier in the integrator” and  $u_{\text{nc}}$  “the equivalent voltage noise of the comparator”. Also we suppose that chopper can completely remove flicker noise. Therefore we only consider the white noise. Fig. 2 shows the interface with these noise sources. Also parasitic capacitance of  $C_x$  in interface side is shown, because it can affect the noise performance of the interface.

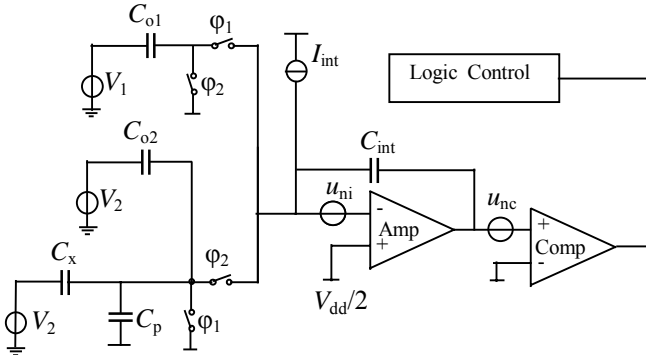


Fig. 2. The interface with important noise sources.

#### A. The effect of $u_{\text{ni}}$

In phase 1 the  $u_{\text{ni}}$  will be sampled on  $C_{o1}$  and  $C_{\text{int}}$  and we have:

$$q_{\text{ni}}^2 = u_{\text{ni}}^2 (C_{o1} + C_{\text{int}})^2 \quad (2)$$

And the jitter on  $T_1$  caused by this noise charge is:

$$\sigma_{T_1}^2 = \frac{u_{\text{ni}}^2 (C_{o1} + C_{\text{int}})^2}{I_{\text{int}}^2} \quad (3)$$

In phase 2 the  $u_{\text{ni}}$  will be sampled on  $(C_{o2} + C_{\text{int}} + C_p + C_x)$  and the jitter due to this noise charge will be:

$$\sigma_{T_2}^2 = \frac{u_{\text{ni}}^2 (C_{o2} + C_{\text{int}} + C_p + C_x)^2}{I_{\text{int}}^2} \quad (4)$$

Then the jitter of  $T_{\text{msm}}$  is:

$$\sigma_{T_{\text{msm}}, U_{\text{ni}}}^2 = 4(\sigma_{T_1}^2 + \sigma_{T_2}^2) \quad (5)$$

#### B. The effect of $u_{\text{nc}}$

At each decision time the noise voltage of comparator will cause variation in the period. This variation depends on the slope of integrator output voltage  $V_{\text{int}}$ , the higher the slop, the lower sensitivity of period to comparator noise. Based on this explanation we can easily derive the jitter of one measurement cycle due to comparator noise. The result will be:

$$\sigma_{T_{\text{msm}}, U_{\text{nc}}}^2 = 8u_{\text{nc}}^2 \left(\frac{C_{\text{int}}}{I_{\text{int}}}\right)^2 \quad (6)$$

Since the bandwidth of comparator is much higher than the integrator amplifier, for the same noise spectral density, the equivalent input noise voltage of the comparator will be much higher too. Therefore based on equations 5, 6 and typical capacitor value of example 1 we can conclude that, the noise of comparator will be dominant.

### IV. MODIFICATION OF INTERFACE

From section 3-2 we found that the noise of comparator is dominant. Therefore in order to improve the noise performance of interface we should decrease the noise contribution of comparator. And increasing the slope of  $V_{\text{int}}$  can do that. We can increase the slope by increasing the integrator current but this will decrease the period. And this can cause more problems. From reference [2] we know that  $T_1 = 10\text{ }\mu\text{s}$  and  $T_2 > 10\text{ }\mu\text{s}$  is good compromise. Then the only way is decreasing  $C_{\text{int}}$ . And this will cause the saturation of integrator. However if instead of pumping whole charge of  $C_x$  to  $C_{\text{int}}$  at once, we control the charge and discharge of  $C_x$  by  $V_{\text{int}}$  then we can prevent the saturation of integrator [3]. Figure below shows the modified Circuit.



For our design this value amount to 28.57 [ $\mu\text{s}/\text{pF}$ ]. The difference between theoretical value and simulated value can be caused by inaccuracy in integrator current source. Since by applying three-signal auto-calibration we can remove these kinds of errors, we don't need to be worry about that. But the non-linearity of transfer function in this case amount to 0.18% and can be the main source of error.

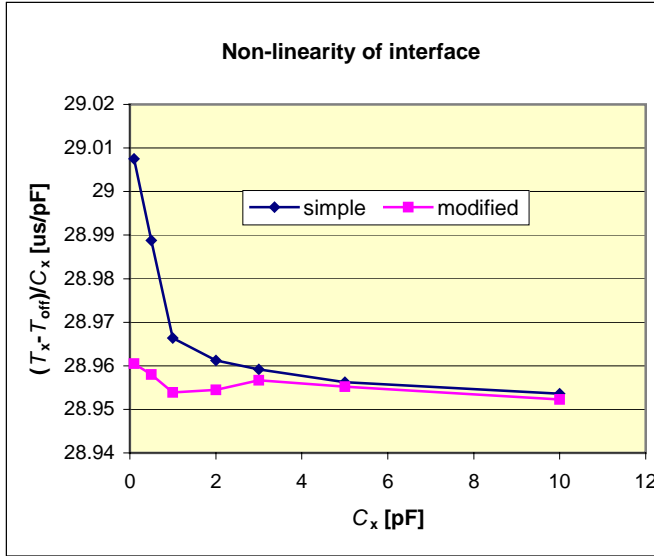


Fig. 6. The non-linearity of the interface.

So we investigate on that and instead of using 1pF as  $C_{\text{off2}}$  we used 0.15pF as  $C_{\text{off2}}$  and 0.85 pF as  $C_{\text{off3}}$  parallel with  $C_x$ . It means that we have the same offset capacitor and only the way of driving these capacitors is different. The results have been shown in the same figure with the label of modified and show considerable improvement and the non-linearity of modified circuit is only 0.03%.

## VI. CONCLUSION

Noise performance of a switched-capacitor front-end for capacitive sensor has been analyzed. Based on our analysis we changed the interface to improve its noise performance. The new interface has been designed in 0.7 $\mu\text{m}$  standard CMOS technology. The whole circuit has been simulated at transistor level in cadence. Simulation result shows 0.18% non-linearity for the range of 0.1-10 pF. By some minor change we could decrease the non-linearity to 0.03%. Measurement will be performed in near future.

## REFERENCES

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