

A 60-GHz Divide-by-3 Injection-Locked Divider

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Abstract— An injection-locked frequency divider that uses an oscillator and a harmonic mixer to perform a divide-by-3 operation is described in this paper. The 60-GHz divide-by-3 divider achieves more than 3 GHz locking range from a 300-mV_{peak} injected signal, while consuming 5 mW from a 1-V supply. The output buffers require another 5 mW from the same supply to provide a differential output swing of more than 200 mV_{peak} driving 50-Ω loads.

Index Terms— Divider, 60-GHz, CMOS

I. INTRODUCTION

Millimeter-wave circuit design for the 60-GHz band is gaining popularity [1-5]. The availability of 7 GHz bandwidth and the possibility of gigabit-per-second data transfer rates contribute to interest in this emerging band. Currently, circuits operating at such high frequencies are being realized in III-V semiconductor technology, which is prohibitively expensive. SiGe BiCMOS technology, while cheaper, have shown great potential in meeting these challenges at this frequency with transistors of transit frequency over 200 GHz [6]. Nevertheless, this technology is still more expensive than the traditional CMOS. Today, the rapid scaling of CMOS technology, e.g., 65nm and 90nm, leads to the emergence of transistors with transit frequencies over 130 GHz. There exists a possibility of designing circuits in CMOS to meet the challenges for the 60-GHz band.

Fig. 1 shows a generic block diagram of a phase-locked loop (PLL). The primary function of the PLL is to provide a stable local oscillating signal for the mixers to perform both up- and down-conversion operations. A crystal is often used to input a highly stable, low-frequency reference signal into the PLL. The phase comparator compares the phase difference between the reference signal and the output of the frequency divider (the voltage-controlled oscillator (VCO) drives the divider), and outputs a DC voltage to adjust the VCO until there is no phase difference. However, the output of the phase detector also contains high-frequency components, which needs to be suppressed by the low pass filter. As the crystals only work in the mega-Hertz range, a frequency divider is clearly needed for a PLL to function in the 60-GHz band. Thus, high-performance frequency dividers are needed to ensure the proper operations of a PLL. Digital frequency

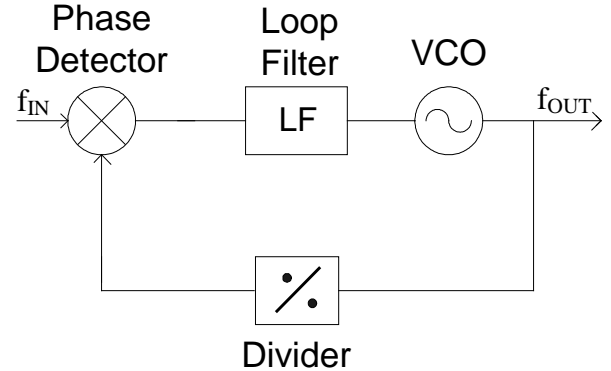


Fig. 1. Block diagram of a PLL.

dividers are commonly used for this purpose but they consume much power, especially at high frequencies. By comparison, injection-locked dividers can work at high frequencies, use less power and have better noise performance. However, they have a narrow operating frequency range [7].

In this paper, the design of a 60-GHz divide-by-3 injection-locked frequency divider (ILFD) in a 90nm CMOS process is described. Dividers with odd frequency division ratios are less common than their counterparts with even division ratios [7, 8]. The divider described in this paper has both an oscillator and a harmonic mixer to realize the odd division ratio. Simple circuits are used to realize both the oscillator and the mixer. In this way, more power is saved, and the design stage is simplified. As the output of this divider is at 20 GHz, a cascade of ILFDs (or digital dividers) will be required to bring the frequency of the signal down to the mega-Hertz range. However, the power consumption of these dividers reduces as the operating frequency decreases.

II. PRINCIPLE OF INJECTION-LOCKED DIVIDERS

A block diagram of the ILFD is shown in Fig. 2. The divide-by-3 operation is realized by a harmonic mixer in a negative feedback loop. An input signal, f_{in} , injects into the mixer, together with the output signal, $2*f_{out}$ or $2/3*(f_{in})$, of the frequency doubler. The doubler is driven by the output, f_{out} or

III. CIRCUIT REALIZATION OF THE ILFD

Although (as seen in Fig. 2) many circuit blocks, i.e., a mixer, a doubler, a bandpass filter and an amplifier, are required to implement an ILFD, the circuit realization consists of only a harmonic mixer, an LC-VCO and an optional buffer to drive 50- Ω external loads. The differential circuit schematic is given in Fig. 3.

In this implementation, a differential pair (M_3, M_4), biased at threshold, realizes the harmonic mixer. The second harmonic, (i.e., at 40 GHz), of the output of the LC-VCO drives the drain terminals of the differential pair. The LC-VCO consists simply of inductors (L_1, L_2) and a cross-coupled pair (M_1, M_2) to provide the negative resistance to compensate for the losses of the tank. When a 60-GHz source is applied at the gate terminals of the harmonic mixer, two output signals at 20 GHz and 100 GHz, respectively, are produced. The bandpass filter, formed by the LC tank of the VCO, rejects the 100-GHz signal but amplifies the 20-GHz output. The parasitics in the circuit also helps in attenuating the 100-GHz signal. An output buffer is required to minimize the loading on the LC-VCO, and also to drive external loads. As shown in Fig. 3, each buffer is an inductively loaded common source stage (M_5 with L_3 , and M_6 with L_4).

To maximize the operating frequency range of the ILFD, the inductors of the LC-VCO are resistively loaded to minimize their quality factors (note that these resistors are not shown in Fig. 3 for clarity). Also, single-ended inductors are preferred to differential implementations to maximize the amplitude of the second harmonic.

IV. SIMULATION RESULTS

The 60-GHz divide-by-3 ILFD consumes 5 mW from a 1-V supply. An additional 5 mW is required by the output buffers from the same supply. Without applying any incident source, the oscillator runs freely at 20 GHz, with a phase noise of -77.2 dBc/Hz at 1-MHz offset from the carrier. The phase noise plot of the LC oscillator is given in Fig. 4. Two

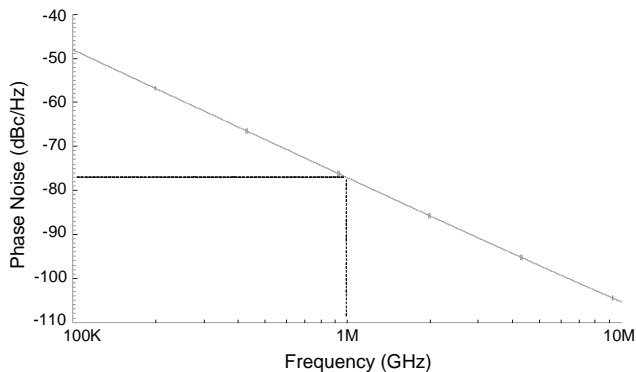


Fig. 4. Phase noise of the free-running oscillator at 20 GHz.

Locking Range vs Input Signal Amplitude

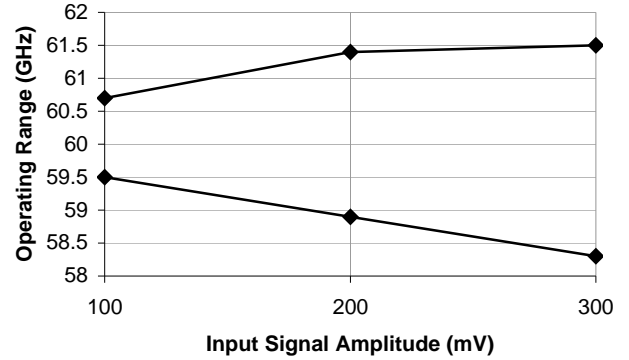


Fig. 5. Simulated minimum and maximum frequency operating range of the ILFD.

inductively loaded output buffers provide a differential swing of more than 200 mV_{peak} driving 50- Ω loads.

Fig. 5 shows both the minimum and maximum operating frequencies of the ILFD for a given injected signal strength. As expected, the operating range increases with injected signal amplitude, and the locked region is symmetric about 60 GHz. When injecting a signal with amplitude of 300 mV, the ILFD working range is more than 3 GHz, from 58.3 – 61.5 GHz. It is also interesting to note that an input signal swing of 200 mV_{peak} offers the largest increase in the operating frequency range.

V. CONCLUSION

The design of a 60-GHz divide-by-3 ILFD is presented. The ILFD consists of a harmonic mixer and an LC-VCO, with an optional buffer to drive external loads. The harmonic mixer is simply a differential pair, whereas the VCO uses a cross-coupled pair to compensate the losses of the single-ended inductors. Including the output buffers, the ILFD consumes 10 mW from a 1-V supply. Without applying any signal source, the ILFD becomes a free-running oscillator at 20 GHz, with phase noise of -77.2 dBc/Hz at 1-MHz offset from the carrier. The ILFD can work over 3 GHz, from 58.3 – 61.5 GHz, with an injected swing of 300 mV.

ACKNOWLEDGEMENT

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REFERENCES

- [1] B. Razavi, "A 60-GHz CMOS Receiver Front-End," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17-22, Jan. 2006.
- [2] B. A. Floyd, S. Reynolds, U. Pfeiffer, T. Beukema, J. Grzyb and C. Haymes, "A Silicon 60GHz Receiver and Transmitter Chipset for

- Broadband Communications,” *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb. 2006.
- [3] C.-H. Wang, Y.-H. Cho, C.-S. Lin, H. Wand, C.-H. Chen, D.-C Niu, J. Yeh, C.-Y. Lee and J. Chen, “A 60GHz transmitter with integrated antenna in 0.18um SiGe BiCMOS technology,” *ISSCC Dig. Tech. Papers*, pp. 659-668, Feb. 2006.
- [4] C. H. Doan, S. Emami, A. M. Niknejad and R. W. Brodersen, “Millimeter-Wave CMOS Design,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.
- [5] B. A. Floyd, S. K. Reynolds, U. Pfeiffer, T. Zwick, T. Beukema and B. Gaucher, “SiGe Bipolar Transceiver Circuits Operating at 60 GHz,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.
- [6] B. A. Orner, Q. Z. Liu, B. Rainey, A. Stricker, P. Geiss, P. Gray, M. Zierak, M. Gordon, D. Collins, V. Ramachandran, W. Hodge, C. Willets, A. Joseph, J. Dunn, J.-S. Rieh, S.-J. Jeng, E. Eld, G. Freeman and D. Ahlgren, “A 0.13um BiCMOS technology featuring a 200/280 GHz (f_T/f_{max}) SiGe HBT,” in *Proc. Bipolar/BiCMOS Circuits and Technology Mtg.*, Sept. 2003, pp. 203-206.
- [7] S. Verma, H. R. Rategh and T. H. Lee, “A Unified Model for Injection-Locked Frequency Dividers,” *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1015-1027, June 2003.
- [8] H. R. Rategh and T. H. Lee, “Superharmonic Injection-Locked Frequency Dividers,” *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813-821, June 1999.
- [9] R. L. Miller, “Fractional-Frequency Generators Utilizing Regenerative Modulation,” in *Proc. IRE*, vol. 27, no. 7, July 1939, pp. 446-457.
- [10] R Alder, “A study of locking phenomena in oscillators,” *Proc. IEEE*, vol. 61, pp. 1380-1385, Oct. 1973.