

# Parallel current-steering D/A Converters for Flexibility and Smartness

G.I.Radulov, P.J.Quinn, P.Harpe, H.Hegt, A. van Roermund

**Abstract**— This paper presents a new DAC architecture [12] built on parallel current-steering sub-DAC entities, see fig.1. This DAC architecture offers various advantages, e.g. easier design flow of complicated high resolution DACs based on low resolution sub-DACs. Furthermore, two main advantageous novelties are explored: flexibility and smartness.

Firstly, a number of available operating modes (op-modes) can set the overall DAC performance and functionality. These op-modes transfer some of the important design trade-offs to the end-user and constitute the DAC flexibility. The main examples include: resolution-power-number of DACs, static-dynamic performance, etc.

Secondly, specific signal processing techniques become possible. The main examples of such techniques include: full self-calibration, cancellation of harmonic distortion (HD) components, and linearity improvement through redundancy [8]. This paper concentrates on a method to suppress undesired HD components through DA processing of phase shifted replicas of the main input signal.

The presented theoretical concepts are realized in a 14-bit DAC built from 4 parallel 12-bit sub-DACs in a standard 180nm CMOS process, see fig. 2. Test chip measurements, HSPICE simulations and a layout design are also presented. The demonstrated flexibility characteristics of the new DAC architecture make the discussed concepts particularly suitable for FPGA integration..

**Index Terms**— Flexibility, Smartness, current-steering DACs.

## I. INTRODUCTION

**F**LEXIBILITY and smartness are two concepts that can successfully address the challenges of modern mixed-signal electronics. In the mixed-signal electronics field, these two concepts are elaborated in [1]. Time-to-market pressure, increased design complexity, advanced but unreliable CMOS technologies, numerous communication standards and requirements are among the important challenges of today's

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AD/DA Converter design [1, 2].

Through flexibility, some design trade-offs are transferred to the choice and the requirements of the end-users. The main aspects of AD/DA flexibility are mainly defined with respect to the performance, e.g. resolution, linearity, power consumption, etc. However, flexibility can also be considered with respect to functionality, e.g. number of independent converters. Such degrees of freedom for the customer are expected to broaden the targeted market niche and reduce the chip costs. Lastly but not least, flexibility can be also considered from the designers perspective. The design of newer generation products can be facilitated if it is based on already verified building blocks. The flexibility of the module-based design is believed to play an important role for the future generation product.

First attempts to introduce flexibility in the mixed-signal circuits were made for ADCs [2]. In [2], the end-users can control the ADC performance parameters: resolution, speed and power, through reconfiguration of the ADC architecture.

Apart from flexibility, smartness offers another answer to today's AD/DA Converters design challenges. It can relax some design trade-offs and hence improve performance [3, 4]. For example, design resources can be exchanged to achieve better overall specifications, better operational efficiency, improved chip yield, and reduced dependence on technology.

A new flexible DAC architecture is presented in section II. The main characteristics of flexibility and smartness are explored in sections III and IV, respectively. The paper shows how some design trade-offs can be transferred to the end-users and how other design trade-offs can be relaxed. It is also shown how smartness can support flexibility and how flexibility can create necessary conditions for smartness.

## II. PARALLEL CURRENT-STEERING DAC ARCHITECTURE

Current-steering DACs are based on parallel current sources, which are switched according to the input digital word to create the analog output signal. The current sources together with the switches define the DAC parallel current cells. With respect to the DAC architecture, the current cells can be grouped in several different ways, e.g. binary [5], thermometer [6], and segmented architectures [7]. This paper proposes a new way of grouping, in which every group is a separate (sub-) DAC, see figure 1. The new sub-DAC way of grouping can be also viewed as a special type of segmentation with more than one set of binary currents.

### III. FLEXIBILITY

To meet the requirements of more customers, a number of flexible DAC parameters are introduced. These allow control over a number of performance trade-offs. Two main such trade-offs can be underlined:

- number of independent operational DACs;
- DAC performance according to the application requirements, e.g. output power, processing power, speed, dynamic linearity, settling time, etc.

Selecting the number of operational DACs broadens the range of possible applications. For example, 3 matched DACs are often needed in video applications, 2 matched DACs are needed in the telecom for the I and Q frequency bands, etc. On the other hand, the customers can set the optimal balance between output power ( $I_{out}$ ), processing power (i.e. power for decoding, synchronization latches, and switch-drivers), speed ( $f_{in}, F_s$ ), and dynamic linearity ( $SFDR$ ). The main controllable DAC parameters are the LSB step current  $I_{lsb}$  and the DAC resolution  $N$ .  $I_{lsb}$  and  $N$  can be changed by connecting sub-DACs in parallel. There are a number of ways to achieve higher  $N$ , as long as the DAC input word is equal to the sum of the sub-DAC input words, e.g. from figure 2:

$$w(nT) = w_1(nT) + w_2(nT) + w_3(nT) + w_4(nT) + \dots \quad (1)$$

Note that [8] presents a fully integrated pre-correction method to optimize the terms of (1) with respect to the mismatch errors of the DAC analog unit elements. A linearity improvement of more than 4 bits is reported. Alternatively, time interleaving is also a possibility to realize higher resolution from several sub-DACs with lower resolutions. Furthermore, a dynamic-element-matching (DEM) technique based on 2 parallel DACs presented in [9] can also be applied to the terms of (1). Finally, if a sub-DAC is not used, its power supply can be turned off and so the system power consumption can be optimized.

To demonstrate such flexibility, a 14b flexible DAC based on 4 parallel 12b sub-DACs is designed in a standard 180nm CMOS technology. Figure 3 shows the Spurious Free Dynamic Range (SFDR) SPICE simulation results against the frequency of the input signal  $f_{in}$  for the main resolution op-modes:  $N \in \{12b, 2 \times 12b, 4 \times 12b\}$ , with  $2 \times 12b \approx 13b$  (2 sub-DACs in parallel) and  $4 \times 12b \approx 14b$  (4 sub-DACs in parallel). The fourth simulation graph  $2 \times 12b, \pi/3$  is for an op-mode discussed in the next chapter: 2 parallel sub-DACs converting phase shifted signal replicas.

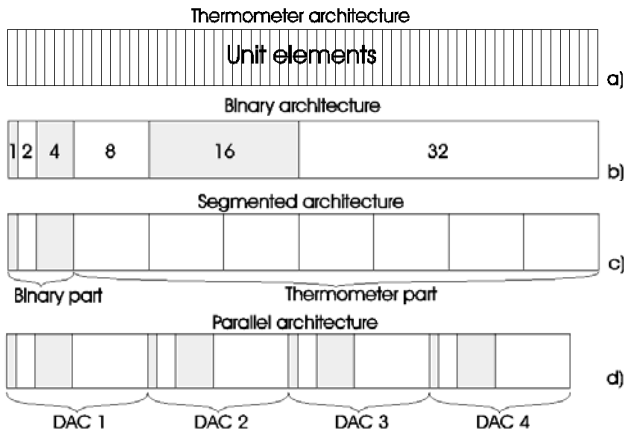


Figure 1. DAC architectures with respect to resource division: a) thermometer; b) binary; c) segmented; d) flexible;

Note that Figure 1d) shows an exemplary type of sub-DACs based architecture, in which the sub-DACs are binary. However, the architecture of the sub-DACs is not limited to binary DACs but can be a segmented architecture as well. Note that when the sub-DACs architecture is thermometer, then the overall DAC architecture would overlap with the conventional thermometer DAC architecture.

Flexibility is the most important advantage of this architecture. However, it also offers the possibility for the application of certain smart techniques to further improve performance. Note that no extra analog resources are required at this point, because the proposed architecture concerns only the grouping of the parallel current cells. Alternatively, the parallel sub-DACs can also be considered as parts of a System-on-Chip solution. In complex digital systems like FPGAs, DACs can be integrated into the Input/Output blocks (I/Os) for analog interfacing. Effectively, these DACs can operate in parallel and hence comply with the segmentation of figure 1d and the high-level scheme shown in figure 2. Integration in an FPGA has the advantage that available FPGA digital resources can be used to implement the digital pre-processing.

As shown in figure 2, the flexible DAC architecture has three distinct parts: digital pre-processor, DA conversion, analog current summation. The digital pre-processor sets the mode of operation (op-mode). It should redistribute the input digital word among the sub-conversion branches. The DA conversion part, i.e. the sub-DACs, contains synchronization latches, parallel current sources and current switches. The analog current summation can be done either on- or off-chip. The off-chip summation can be realized by simply connecting the appropriate outputs of the sub-DACs together. The off-chip connections may be preferred for minimizing the inter-DAC parasitic coupling and output DAC capacitance. Note that the architecture choice for the sub-DACs is open and it can be made according to the existing knowledge [5, 7].

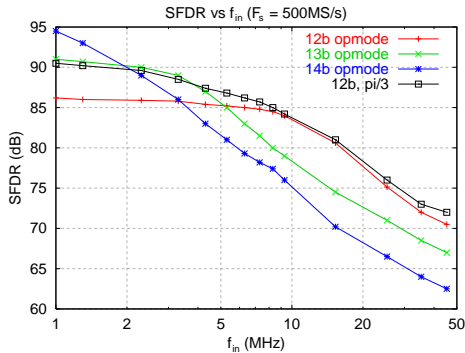


Figure 2. Simulated SFDR for different DAC op-modes (Spice).

At lower input frequencies  $f_{in}$ , the high resolution op-modes deliver better SFDR and the quantization noise is less than for the lower resolution op-modes. However, for each additional sub-DAC that is used, the processing power increases (e.g. 36mW per sub-DAC in this example). Therefore, the 12b op-mode consumes 4 times less processing power than the 14b op-mode, excluding the power of the pre-processor. At higher  $f_{in}$ , the lower resolution op-modes become superior. The dynamic limitations in the sub-DACs are predominant and they increase with the number of cells working in parallel. A few important dynamic limitations cause the major performance degradation for the high-resolution op-modes. Firstly, the input dependent DAC output capacitance increases when more sub-DACs work in parallel. Secondly, the DAC unit current has to be decreased for higher resolution op-modes, so that the DAC full-scale current is kept the same (usually 20mA). Less current requires more time to charge the parasitic capacitances in the DA cells and hence the error current related to the DAC output increases. Finally, the more DAC cells work in parallel, the bigger the synchronization problems. Therefore, lower resolution op-modes would be preferred for higher  $f_{in}$  while higher-resolution op-modes would be preferred for lower  $f_{in}$ .

#### IV. SMARTNESS

Redundancy is an important inherent characteristic of the parallel DAC architecture: there are more available resources than strictly necessary. Flexibility is one way to exploit the redundancy. Another way of exploiting it is by means of smartness to improve the performance. For example, in [9], a DEM technique is used with two parallel binary converters. This is a suitable candidate for the presented architecture. In [8], the redundancy in four parallel sub-converters is used to improve linearity by minimizing the effects of mismatch.

A common property of the above-mentioned techniques is that they focus on transistor mismatch errors. These errors are independent and random. Another big error concern is the class of the systematic errors [10]. These errors cause deviation from the ideal behavior that is identical for each identical unit source, and hence identical for each sub-DAC in the parallel architecture. Examples of these errors are clock-feedthrough, data-feedthrough, data-dependent disturbances of the substrate and power rails, systematic parasitics due to the layout, output glitches, etc. These errors result in harmonic distortion (HD) of the input signal. In the following, a method for the suppression

of harmonic distortion (MSHD) is proposed. MSHD is able to counteract the effect of the DAC systematic error mechanisms.

HD components that are generated by the sub-DAC branches can be made to suppress each other, when the sub-DACs convert phase-different input signals. A similar method completely in the analog domain has been previously applied for mixers, see [11]. Consider a DAC with systematic non-linearity due to some global errors. The output  $I_{out}$  can be generally described as a polynomial of the input code  $w$ :

$$I_{out} = a_1 w + a_2 w^2 + a_3 w^3 + a_4 w^4 + \dots \quad (2)$$

When an ideal sinusoidal signal of the form  $w = A \cdot \sin(\omega_{in} \cdot nT)$  is an input to the DAC, the output  $I_{out}$  will contain undesired HD components. Consider a DAC architecture based on  $k$  parallel and identical sub-DACs, e.g. figure 2. Each sub-DAC is fed with a phase-shifted version of the original input signal  $w(nT)$ , and the output  $I_{out}$  is constructed by summing the individual sub-DAC outputs  $I_{out_i}$ ,

$$i.e. I_{out} = \sum_{i=1}^k I_{out_i}. \text{ As long as the non-linearity of the sub-DACs}$$

is stemming from systematic errors, the outputs  $I_{out_i}$  can be modeled with the same polynomial function (2). It can be shown that the amplitudes  $A_h$  of the harmonic frequency

$$\text{components } h\omega_{in} \text{ of } I_{out} \text{ are } A_h = C_h \left| \sum_{i=0}^{k-1} e^{jh\varphi_i} \right|, \text{ where } C_h \text{ is a}$$

constant and depends on the coefficients  $a_i$ ,  $\varphi_i$  is the phase shift applied to the  $i$ -th sub-DAC. Thus, harmonic component  $h$  can be suppressed by reducing (or ideally nullifying) the term

$$\left| \sum_{i=0}^{k-1} e^{jh\varphi_i} \right| \rightarrow 0. \text{ Via choosing an appropriate number of parallel}$$

sub-DACs  $k$  and an appropriate set of digital phase shifters  $\varphi_i$ , any desired combination of HD components, stemming from systematic error mechanisms, can be suppressed or cancelled. Note that the suppression can be achieved without knowing the actual amount of distortion, i.e. for any coefficient  $a_i$  of (2).

For example, consider the suppression of the often dominant 3<sup>rd</sup> order distortion component, see figure 4 for a phase diagram. In this case, only two sub-DACs are sufficient:  $k = 2$ ,  $\varphi_1 = 0$ ,  $\varphi_2 = \pi/3$ . The relative amplitude of the main

$$\text{signal } (h=1) \text{ will be } \left| e^{j0} + e^{j\pi/3} \right| = \sqrt{3}, \text{ while the 3}^{rd} \text{ order harmonic distortion component } (h=3) \text{ is completely cancelled } \left| e^{j3 \cdot 0} + e^{j3 \cdot \pi/3} \right| = 0.$$

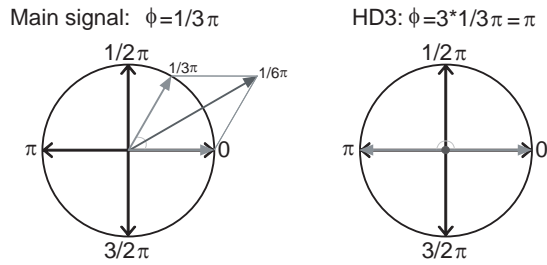


Figure 3 . Phase diagrams of the signal and the 3<sup>rd</sup> order harmonic distortion component for 2 parallel DACs.

Figure 3 shows the SFDR performance of the MSHD for the example given in figure 4, i.e. 2 12bit sub-DACs converting  $\pi/3$  phase shifted signals. The SFDR of the MSHD is limited by the 3<sup>rd</sup> order HD component, which is caused by the finite output resistance/impedance of the DAC and hence not addressed by the MSHD. At lower frequencies the performance is comparable with the 13b op-mode, while the digital input is only 12b. From 4 to 10MHz, MSHD op-mode delivers the best SFDR. At high frequencies, the global error mechanisms become predominant, e.g. data-feedthrough, DAC output glitches, etc. In these cases, the MSHD is particularly useful. Figure 5 shows the DAC output frequency spectrum both with and without MSHD for  $f_{in} = 80.3MHz$  at  $F_s = 500MS/s$ , where HD3 is suppressed by about 10dB! MSHD is particularly appropriate for OFDM (Orthogonal Frequency-Division Multiplexing) systems, in which the realization of phase delays in digital domain can be made with only one complex multiplier.

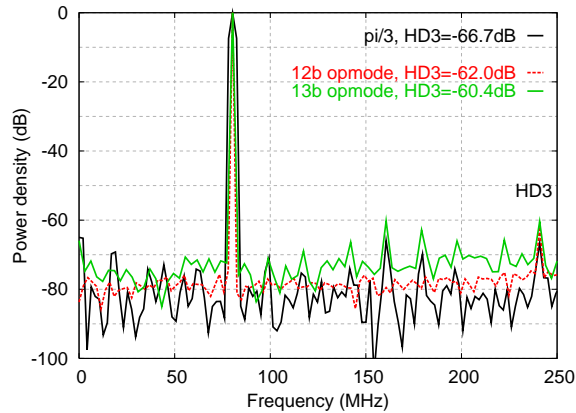


Figure 4 . Simulated DAC output spectrum for  $f_{in}=80.3MHz$  at  $F_s=500MS/s$  both with and without MSHD.

## V. FLEXIBLE DAC REALIZATION

The proposed DAC architecture has been realized as a 180nm test-chip which is presently being processed at the foundry. Figure 6 shows the layout of the 14b flexible DAC. Despite the flexibility extensions, the area of the DAC is comparable to the state-of the art reported in the literature [4-7,9]. The black dashed lines show the parallel sub-DACs. The chip micrograph is shown in Figure 7.

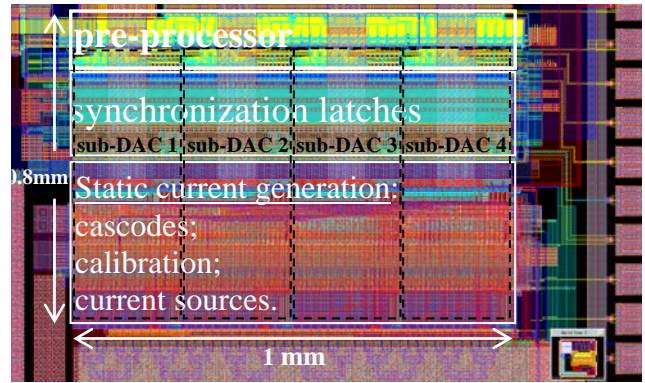


Figure 5 . Layout design of the 14b flexible DAC (180nm CMOS).

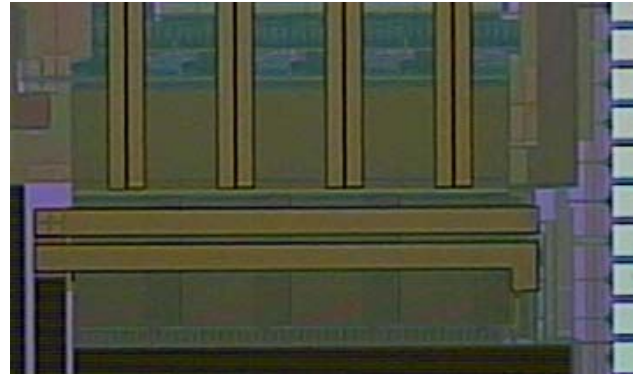


Figure 6 . Chip micrograph of the 14b flexible DAC (180nm CMOS).

## VI. PRELIMINARY CHIP MEASUREMENTS

By the time of writing this article, the measurements of the flexible DAC test chip are at a very initial phase. Therefore, only a few measurement results can be so far reported.

An important aspect of the test-chip flexibility is independently using the sub-DACs. That is why it is important that the output of one sub-DAC does not interfere through parasitic coupling with the output of another. In the following experiment the test-chip is fed by a digital pattern containing the codes of two interleaved tones. All even codes belong to the first tone of 8MHz and all odd codes belong to the second tone of 13.5MHz. When all codes are read by both sub-DACs, the output is a two tone signal as shown in Figure 7. When sub-DAC A reads only the even codes and sub-DAC B reads only the odd codes, the result is a single tone output with mutual interference lower than at each individual output 80dB, as can be seen from Figure 8 and Figure 9.

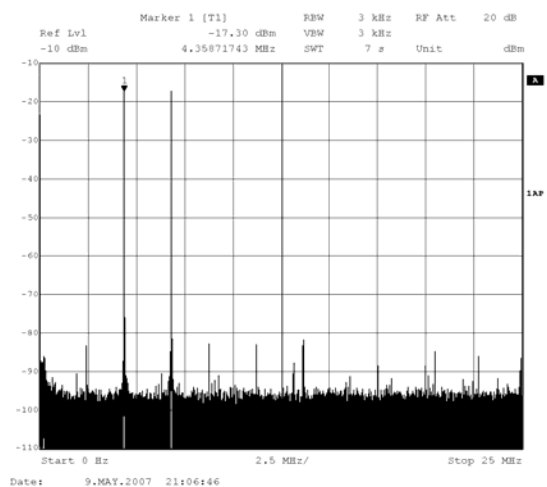


Figure 7. Output spectrum of two tone measurement, with sub-DAC A converting tone of 8MHz and sub-DAC B converting tone of 13.5MHz.

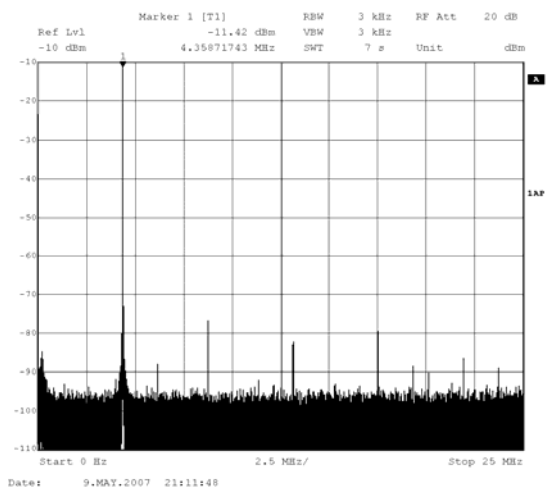


Figure 8. Output spectrum of a single tone measurement from sub-DAC A converting tone of 8MHz, while sub-DAC B is converting tone of 13.5MHz. The mutual interference is lower than the quantization noise.

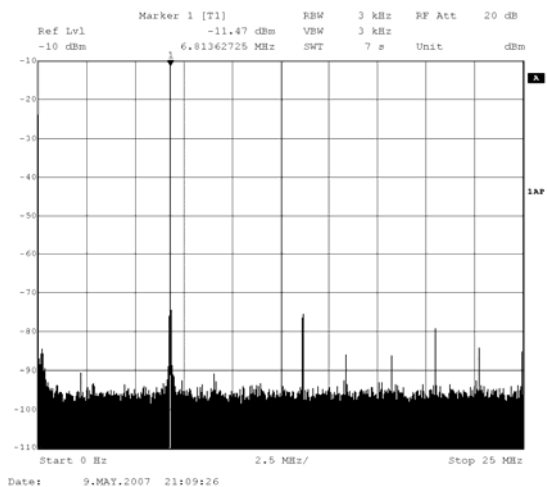


Figure 9. Output spectrum of a single tone measurement from sub-DAC B converting tone of 13.5 MHz, while sub-DAC A is converting tone of 8MHz. The mutual interference is lower than the quantization noise.

## VII. CONCLUSIONS

A new flexible DAC architecture based on parallel sub-DAC entities was presented. Its major advantage is that the end-user can customize the DAC performance and functionality via several op-modes. At lower input frequencies, better SFDR is achieved for higher resolution configurations, while at higher frequencies the lower resolution op-modes are advantageous. The DAC performance can be further improved through the smart techniques that are enabled by the parallel sub-DACs. Particular attention was put on a method to suppress harmonic distortion, which uses phase-shifted parallel DA sub-conversion branches to improve the DAC dynamic performance. The method addresses many systematic error sources and is particularly useful for very high signal frequencies when these error sources become predominant. Especially because of its flexibility, the new DAC architecture is particularly interesting for integration with FPGA.

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