Calibrating a device simulator on advanced CMOS devices using the substrate bias dependence

Pietro Andricciola and Hans Tuinhout

***Abstract*—Simulating advanced CMOS devices can be very helpful for understanding causes of a-priori unexpected effects encountered in measurements. However, this can not be done without having a good representation of the actual (silicon) device reproduced in the TCAD simulator. Creating such a representation becomes particularly challenging when most of the actual process parameters and settings are secret, as is the case with foundry supplied wafers. In this paper we address the most widely used methodology for TCAD tuning of advanced CMOS devices. We demonstrate how a very good agreement in the main transistor characteristics such as I_{ON}, I_{OFF} and V_T can be reached while in fact the underlying doping profiles are incorrect. We show that this can be discovered and corrected by taking the body effect properly into account. The novelty of the problem lies in the fact that in contemporary CMOS technologies the body effects are not only determined by the channel and well implants, but that they are also strongly affected by the halo constructions.**

***Index Terms*—TCAD calibration, advanced CMOS, substrate behavior.**

I. Introduction

TCAD simulations are extensively used as an eye into the device in order to explain effects observed through measurements or to evaluate different causes of variability in contemporary CMOS as well as future nodes [1]. Device simulations can help to link process parameters and electrical characteristics. To do so, a TCAD engineer needs to construct a virtual device that is as close as possible to the actual silicon.

The procedure to adjust the simulator's results to mimic real measurements is often indicated with the term TCAD calibration. Usually this is done by fitting current measurements in linear and saturation regimes for long devices first and then going down to the minimum dimensions, adjusting for instance the mobility model parameters, doping profiles etc [2]. This task becomes particularly challenging when the device is drawn from scratch, even when the architecture is based on common scaling principles and inputs from the ITRS roadmap. Quite often, detailed process parameters are unknown as they are considered trade secrets. This is for instance the case when the silicon is obtained from external foundries.

In this paper we discuss methodologies and techniques for such "blind" calibrations. Furthermore, we demonstrate that targeting only the first level parameters such as the saturation current measured at high gate and drain bias, I_{ON}, the threshold voltage, V_T, the current taken at zero gate voltage and high drain bias, I_{OFF}, the drain induced barrier lowering, *DIBL*, and the subthreshold slope, *SS*, can result in good agreement even with a doping profile far from the reality. It is a situation that must be avoided because such a device cannot properly reproduce second order effects for which TCAD is such a powerful investigation tool.

An excellent way to verify the doping profile is by evaluating the device behavior as a function of the substrate bias. The presence of halos (high tilt implants to improve short-channel behavior) for instance, makes the doping below the gate non-uniform in lateral direction. When a substrate bias is applied, the depletion region below the gate will change. Thus, if the doping profile is wrong, it will have a different impact on the threshold voltage compared to measurements. This paper demonstrates that the substrate bias behavior is not only the ultimate check on the calibration quality, but that it should be used from the start to calibrate the device construction.

II. TCAD Calibration

A. General considerations

In most cases a proper TCAD calibration is obtained by feeding a process simulator with the process parameters provided by the fab. Then, by adjusting some fitting variables, it is generally possible to create a device that is very close to the reality. This is for instance the approach when simulations are used to predict the effect of a process setting (an implant dose, a temperature step, etc) on the device or to analyze different possible process routes to improve device performances. However, when TCAD is not employed as predictive tool and no precise indications from the foundry concerning the exact device architecture are available, a different strategy can be followed. For the work underlying this paper this alternative approach to TCAD is used. In our case, the process simulations are skipped and the device structure is created directly with a so-called structure editor. The advantage of using this tool instead of a process simulator is the speed. As a matter of fact, since there is no need to solve any equation, it creates the structure in a few seconds

This work was supported by EU Marie Curie action MOICCO project.
P. Andricciola and H. Tuinhout are with the NXP-TSMC Research Center, HTC 37 5656AE Eindhoven, The Netherlands (e-mail: pietro.andricciola@nxp.com).

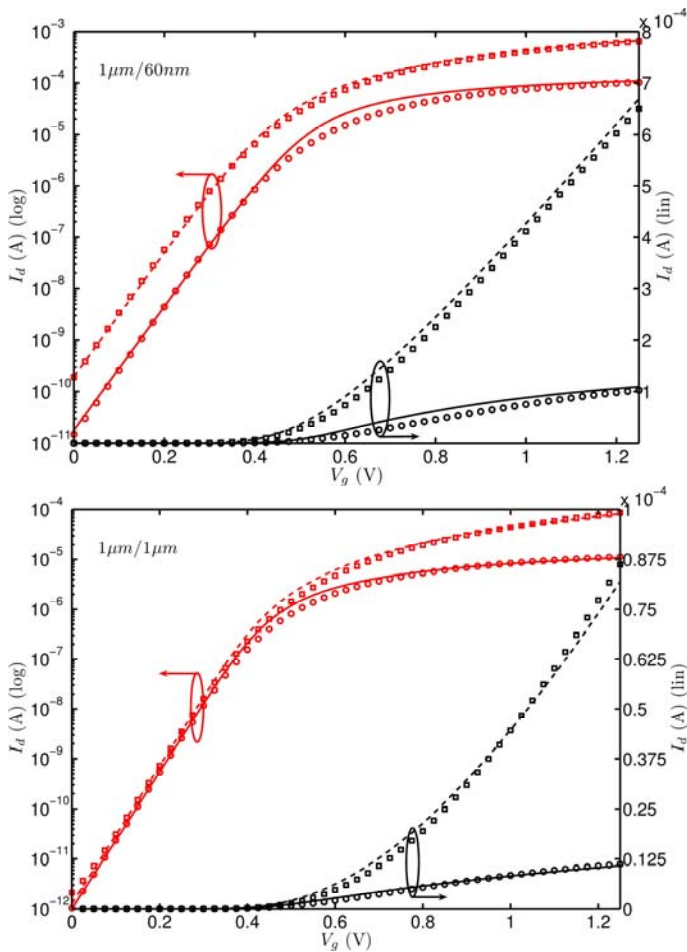

Fig. 1. Drain current versus gate voltage of simulations (lines) and measurements (symbols) after the first calibration in linear and logarithmic scale. Circles and solid lines represent low V_d (50mV) whereas squares and dashed lines represent current at high V_d (1.2V).

(compared to several hours needed for a process simulation). Once the structure has been created (following for instance ITRS roadmap guidelines [3]) and the simulation has been performed, a comparison with measurements takes place. A classical and simple method consists of comparing the simulations with the measured current in the linear region (low drain voltage) and in the saturation regime (high drain voltage). The main performance indicators of MOS devices, such as I_{ON}, I_{OFF}, V_T, *DIBL* and *SS*, can be determined using these two curves.

Once the measurement data have been collected, the real calibration begins. The simulator and the structure editor offer many fitting variables and tunable parameters. Unfortunately this means that an inexperienced user without sufficient knowledge of the physics underlying the device's performances can take forever in trying to get a reasonable calibration. To avoid this we want to summarize the main "knobs" and what they can do. Some of the main variables are:

- Doping profiles are obviously the most important device construction elements, as they play a role in any region of the device characteristic. In modern technologies due to the presence of halos and composite well implant there are many degrees of freedom related to doping profiles in the virtual device creation.
- Oxide thickness and dielectric constant predominantly affect the subthreshold slope and the current factor. The exact values of the thickness and the dielectric constant (in modern technology the dielectric is slightly nitrided to reduce leakage and to increase ε_r) are often unknown.
- Drain and source extension overlaps and lateral diffusions determine how far drain and source extend beneath the gate and hence determine the *DIBL* and the actual current factor.
- Gate work function adjustments are used to shift the curve in one or the other direction to get the correct threshold voltage.
- Mobility model parameters play an essential role in determining the current in strong inversion.

Of these five knobs, the mobility models probably are the most controversial in the semiconductor device physics and TCAD worlds, and hence deserve a more detailed explanation. In most of the commercial device simulators there is a variety of mobility models from which the user can pick. The total mobility is the result of a combination of different effects like the mobility reduction due to high doping or the velocity saturation. Moreover, for each effect there also are different formulations originating from different research groups. Once the effects that need to be taken into account have been chosen, the user must choose the different formulations (only one submodel per effect is allowed). Finally, the simulator calculates the overall mobility by adding the different mobility effects following the Mathiessen rule [4], [5]:

$$\frac{1}{\mu_{tot}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \ldots \tag{1}$$

where μ_{tot} is the total mobility and $\mu_{1\ldots2}$ are the mobility effects that are taken into account. According to (1) the dominant factor for the overall mobility is therefore the lowest value. This means that through modifying different submodels of the overall mobility, the user can affect the current under a particular bias condition while having a negligible effect on the others. For example the *high field saturation* model will uniquely affect the current for high drain bias while the *mobility degradation at interface* model will predominantly affect the current at low drain bias in long devices.

It is worth to point out that all parameters and variables should be kept identical for all the dimensions that will be considered during the actual analysis. A well-calibrated device architecture will then properly follow the behavior seen in measurements for instance when varying the drawn gate length.

B. *Experimental setup and calibration procedure*

All the simulation results shown in this paper have been obtained using a set of 2D Synopsys tools, namely the Sentaurus Structure Editor for the creation of the devices and

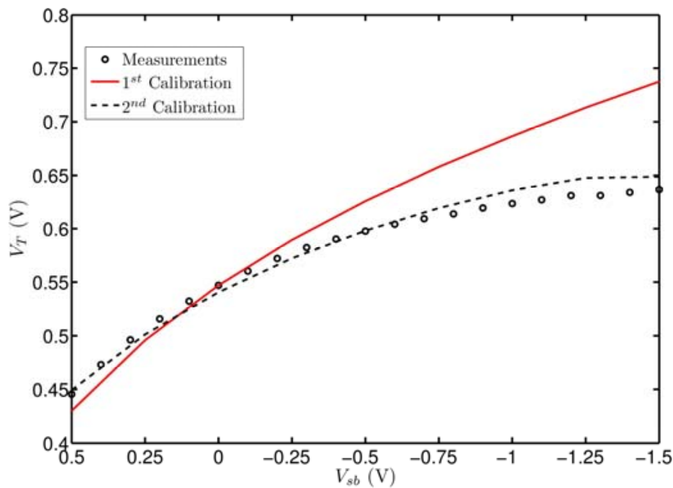

Fig. 2. Threshold voltage versus source-substrate bias for simulations (lines) and measurements (symbols) in the case of short device. The device after the first calibration deviates from measurements indicating a wrong doping profile.

Sentaurus Device for the simulation. The aim of our calibration was to create virtual devices close to the ones processed by TSMC in their Low Power bulk CMOS 65-nm process. The reference for the calibration was based on the median device performance of a population of 119 standard V_T N-type MOSFETs measured all over a 300 mm wafer at 25 °C. The test structure is described elsewhere [6]. Two gate lengths are used in this paper, namely W_1/L_1=1 µm/1 µm and W_2/L_2=1 µm/0.06 µm.

The best way to follow is by starting to create a structure with a plausible doping profile following the ITRS suggestions. The first characteristic that one should look at is the subthreshold slope since it is driven by the ratio between the gate and the depletion capacitances and therefore it is not influenced by the mobility. It can be modified by tuning the doping profile (especially on the upper region below the oxide) and the gate capacitance (i.e. changing thickness and dielectric constant of the oxide).

The next suggested step is the fine tuning of the drain and source overlaps to obtain a good *DIBL*, in particular for the short device. Once the *DIBL* is correct, the gate work function can be used to force the simulated curves and the measurements on top of each other in the subthreshold region.

In the final step the mobility parameters can be modified (if still needed) to get the right current value in the ON condition.

The full procedure may imply several cycles of tuning and refining because these “knobs” are by definition strongly correlated. This means that even if some characteristics are well reproduced, this might due to a compensating effect of two (or more) features of the device structure. To exemplify this statement one can take the *DIBL* as example. The same *DIBL* value can be obtained with high channel doping and long overlap or with low doping and short overlap.

Figure 1 shows the final result of the calibration procedure sketched above, compared to measurements for long and short channel devices. For most of the common purposes the agreement is more than good enough.

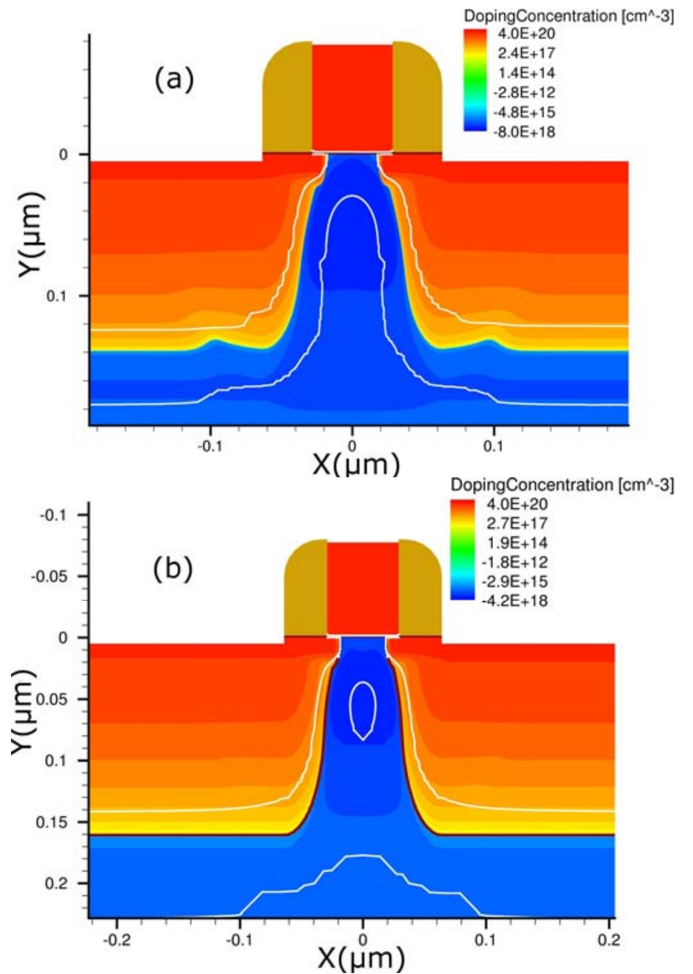

Fig. 3. Cross-section of simulated device with source-substrate bias of -1.5 V and gate bias of 1.2 V. The white lines represent the depletion region contours. Changing the doping profile the depletion region extends more in the region between drain and source. This makes the threshold voltage almost independent from substrate bias.

C. *Body effect*

The correlation between the calibration factors also leads to another problem. It is possible that the calibration obtained in this way is actually far from the reality. There is an additional way to check whether there is a difference between the virtual doping profile and the real one: the body effect, i.e. the dependence of the threshold voltage with the source-substrate bias. The body effect is dependent on the doping in the substrate. The threshold voltage changes accordingly with the movement of the depletion region in the channel region. Figure 2 shows V_T for the short device versus the source-substrate bias. For negative substrate biases the **measured** V_T tends to saturate whereas applying the same bias conditions at the simulated device the threshold voltage keeps increasing with the decreasing of source-substrate bias (red solid line in Fig. 2).

If we look into the simulated device, obtained after the first calibration, we see that the depletion regions from drain and source stay apart even after applying negative source-substrate biases (Fig. 3(a)). This determines the discrepancy between

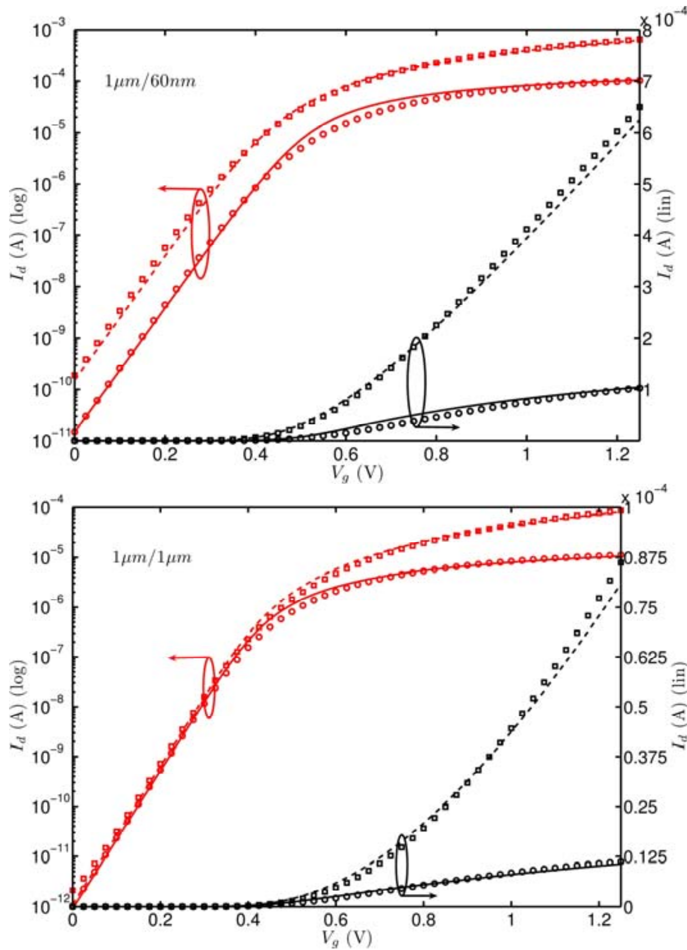

Fig. 4. Drain current versus gate voltage in linear and logarithmic scale of simulations (lines) and measurements (symbols) after the second calibration. Circles and solid line represent current at low V_d (50 mV) whereas squares and dashed lines represent current at high V_d (1.2 V).

measurements and simulations. The depletion regions have still room to extend below the gate resulting in the relatively big impact on the threshold voltage at any change of the back bias. On the other hand, when the dopant concentration underneath the gate is substantially decreased, the depletion layer extends all the way into the lower doped region of the substrate. Consequently, the threshold voltage becomes nearly independent from further decreases of substrate bias. Figure 3(b) shows a cross-section of a device with new doping profile under the same bias conditions. This device has been made by lowering the peak values of the halos and of the anti-punch-through implants. The original profiles had too high values preventing the depletion regions from penetrating the region between source and drain.

With the new doping profile the body effect seen in the measurements is reproduced very well (dashed line in Fig. 2). It is worth to point out that for long devices, measurements and simulations matched very satisfactory even after the first calibration.

Since the body effect proved to be very useful to check the overall calibration one can think of using it in the early stage of the calibration to extract information about the doping. For example a simulated V_T that varies faster than measurements in function of V_{sb} may indicate a too high doping or if it saturates earlier it can point towards a too shallow profile. A drawback of this strategy is the simulation time consumption. As a matter of fact, to check the body effect, at least nine additional simulated curves are required, which results in a simulation time that is about five times longer. In the early phase of a calibration such long simulation can be quite annoying considering that it must be repeated a number of times to reach a decent agreement.

Although it may seem a price too high to pay, good back bias behavior guarantees a high level of confidence in the calibration from the beginning and this is a case in which quality cannot be traded with speed.

Finally, after the correct substrate behavior has been obtained all the calibration steps have to be done again as described in Section II b. The agreement is excellent after the second calibration, as shown in Fig. 4. The obtained profiles form an excellent basis for some detailed device studies that we will report on in later work.

III. Conclusion

In this paper we discussed some guidelines for TCAD calibration of advanced CMOS devices. We showed that if the foundry does not provide all the relevant information about the actual device, the availability of too many degrees of freedom can lead to a calibration that seems good only after shallow analysis. The use of the substrate dependence can help to improve the calibration. Therefore we conclude that the body effect can be tested not only as the ultimate check on the calibration quality, but that it should be used from the start to calibrate the device improving the reliability of the calibration.

Acknowledgment

The authors wish to thank Anco Heringa from the NXP-TSMC Research Center for his guidance in the TCAD simulation field.

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