

Design of a Ring-Oscillator with a Wide Tuning Range in 0.13 μm CMOS for the use in Global Navigation Satellite Systems

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Abstract— In this paper, the basics of the three major satellite navigation systems (GPS, GLONASS and GALILEO) are explained. They are analysed regarding their RF-frequency usage and a specification for the receiver's local oscillator is derived. Different oscillator topologies are investigated to find a topology which satisfies the demands for a reception of all possible systems with a very low power consumption.

Keywords— GPS; Galileo; ring oscillator; voltage controlled oscillator.

I. INTRODUCTION TO GNSS

Global Navigation Satellite Systems are based on measurements of distances from the receiver's position on earth to satellites in orbit. These satellites are on non-geostationary orbits, which means that they do not have a fixed position in relation to the earth's center. The measured distance is called „pseudo-range“. These pseudo-ranges are determined by measuring the time which a transmitted signal from the satellite needs to reach the receiver. In first approximation this equals the distance divided by light speed. Four pseudo ranges are necessary to calculate the receiver's position in three-dimensional space. To distinguish between the received signals for each visible satellite, different methods are used in the three major satellite navigation systems. These are the the American GPS, the Russian GLONASS and the European GALILEO.

II. SPECIFICATIONS

The American GPS (Global Position System) was introduced in 1973. At present time it consist of 24 satellites, rotating around the earth in six different orbits. Each of those satellites transmits information in two frequency bands. This information consists of the satellite's current position in space, its own local reference time and some status bits about its condition. The center frequencies of these bands are 1575.42 MHz (equals 154x10.23 MHz)

and 1227.60 MHz (equals 120x10.23 MHz). The data rate of the signal is as low as 50 bit/s. For the transmission the signal is first BPSK modulated and than modulo-2 added to two different pseudo random noise (PRN) codes. These codes are based on the code division multiple access principle which enables the system to use the same frequency band for different satellites, without interfering each other. The PRN codes additionally work as a spread spectrum sequence which increases the bandwidth of the transmitted signal. One of these, the P-Code, is reserved for military use. It uses a bandwidth of 20.46 MHz, transmitted in both frequency bands. The civil code (C/A-Code) is only transmitted in the upper band (so called L1-Band) and requires a bandwidth of 2.046 MHz. The received signal power on earth's surface is at least -136 dBm and at most -123 dBm. In terms of a modernisation of the GPS-System a third frequency band (L5) will be introduced, to rise the capacity from three transmitted signals in two bands to seven in three bands. The L5-band will have a center frequency of 1176.45 MHz (equals 115x10.23 MHz). The expected bandwidth of the new signals is 24 MHz. Figure 1 gives an overview of the frequency ranges for GPS.

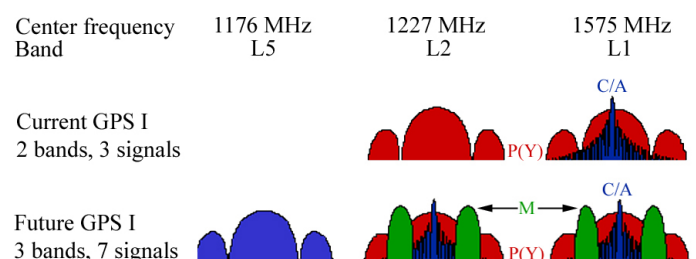


Fig. 1. Frequency Usage for the American GPS

The European Union works towards its own satellite navigation system called GALILEO, which is estimated for the year 2008. First signal transmissions are to begin in 2005. GALILEO will consist of 30 satellites with a distance of about 24.000 km to the earth surface. Compa-

rable to GPS it uses a CDMA-method to provide several services in different frequency bands. The data is modulated using a pseudo random noise spread spectrum code, a QPSK scheme and additionally protected by 1/2-rate viterbi codes. The signal power is expected to be about -125 dBm. GALILEO will consist of 6 bands, called E5a (1176.45MHz), E5b (1207.14MHz), E6a (1278.75MHz), E2-L1-E1 (1575.42MHz) and L6 (1544.10MHz).

In contrast to the European GALILEO and the American GPS, the russian GLONASS uses a frequency division multiple access method to distinguish between the signals from different satellites. Each satellite uses a 1 MHz bandwidth, which leads to an overall bandwidth of 12 MHz with 24 satellites (only half of them are concurrently visible on one earth's side). Due to the difficult political and economical situation of the former sovjet union, currently (concerning to the russian Coordination Scientific Information Center) only 8 satellites are still operational. In respect to this, GLONASS is not investigated any further in this paper.

It is obvious, that for a reception of all signals a system is necessary, which offers a frequency tuning range from 1164 MHz to 1591 MHz (Figure 2).

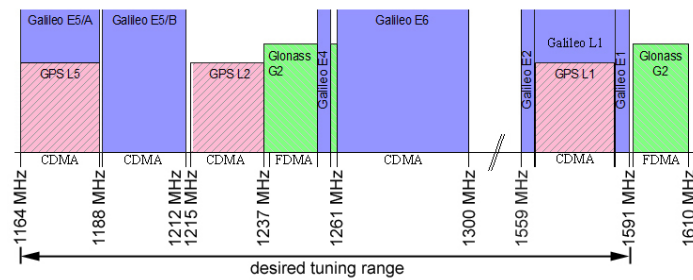


Fig. 2. Schematic display of the frequency bands for GNSS

For the derivation of the receiver specifications, the main lobe of a typical GPS signal is accounted. The main lobe has a bandwidth of 2 MHz, so the noise floor is $kTB \approx -111$ dBm at a temperature of 290K. With an average signal power of -133 dBm at the antenna, a signal to noise ratio of -22dB is aquired.

The coding gain of the spread spectrum code used in the modulation is $G_p = 10 \log \left(\frac{f_c}{f_b} \right) = 43dB$ with $f_b = 50Hz$ and $f_c = 1575.42MHz$. After correlation we obtain a signal to noise ratio of 21 dB, under the assumption of no further noise injection in the receiver. The size of a typical GPS-signal frame is 2560 bit, so a bit error rate of 10^{-5} must be achieved to ensure sufficient signal decoding. This can be achieved with a maximum SNR of approximately 14 dB. The receivers front-end can therefore be allowed to have additional 8 dB of noise.

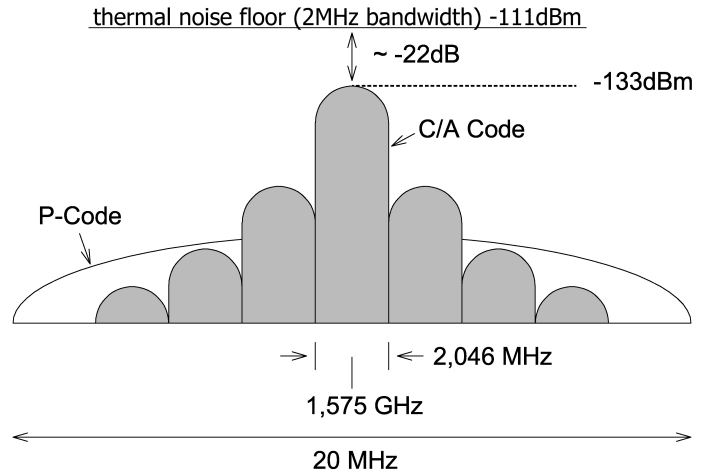


Fig. 3. Display of the received signal power for GPS

The calculation of the requirements for the spectral pu-reness of the local oscillator can be adopted from [Mon03], which allows a phase noise of -95 dBc/Hz at a 1 MHz off-set to the carrier frequency. The power dissipation of the oscillator should be below 20 mW according to the cited specifications.

III. OSCILLATORS

Several types of oscillators for RF frequencies do exist. Most of them use inductors and capacities (LC-Oscillators) to provide oscillation. These inductors are quite large and cannot be scaled by the same factor as the minimal dimensions of the technology is shrinking. In contrast to this ring-oscillators consists only of MOS-transistors and could therefore be more easily scaled to-wards newer technologies.

A ring-oscillator consists basically of a series of inver-ters, which is back coupled to provide an unstable state that leads to oscillation (Figure 4). The frequency of oscillation depends on the delay of each inverter, which is determined by the input capacity, that each inverter provides to its pre-decessor and the resistance that is inserted in the current path between the capacity and supply rails.

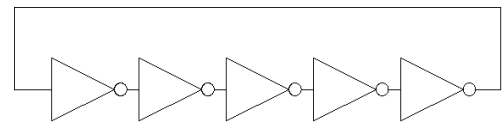


Fig. 4. Schematic version of a ring oscillator with 5 stages

In the simplest equivalent circuit, the inverter can be dis-played as a switched resistor between V_{dd} , G_{nd} and the load capacity.

The time constant for the transition from high to low level is then $t_{HL} = R_p \cdot C_{load}$ and from low to high level $t_{LH} = R_n \cdot C_{load}$.

$R_{p,n}$ is the path resistance of the preceding inverter stage and C_{load} the input capacitance of the transistor gates.

$$R_{p,n} = \frac{L}{W} \frac{1}{K'_{p,n}(V_{dd} - V_{thp,n})} \quad (1)$$

$$C_{load} = C_{ox,n} + C_{ox,p} \quad (2)$$

with

$$C_{ox,n,p} = \frac{W \cdot L}{t_{ox}} \epsilon_0 \epsilon_r \mu_0 \quad (3)$$

The static power consumption of such a circuit consists of just the leakage currents between power supply and Gnd through the inverter paths. Each inverter therefore consumes

$$P_{stat} = V_{dd} \cdot \bar{I} = V_{dd} \cdot (I_{n,off} \cdot \frac{W_n}{L} + I_{p,off} \cdot \frac{W_p}{L}) = 84nW \quad (4)$$

in a current $0.13\mu m$ technology.

The dynamic power consumption consists of two parts, which are both dependant on the oscillation frequency. The first part is the short circuit current flowing through the inverter path from V_{dd} to Gnd during its switching process. Regarding [Kla93] this is about 15% of the overall power consumption per gate. The main part is used for charging and discharging the load capacitance.

Viewed over a period T , this power equals

$$P_{dyn} = \frac{1}{T} \int_0^T u(\tau) \cdot i(\tau) d\tau. \quad (5)$$

With maximum utilization of the power swing this equals

$$P_{dyn} = f_0 \cdot C_{load} \cdot V_{dd}^2 \quad (6)$$

This leads to the conclusion, that it's necessary to find a compromise between power consumption and the noise performance of the oscillator.

To trim this basic version of the ring oscillator to a desired frequency, different alternatives are possible. By current starving the inverter with additional transistor based loads in the paths towards V_{dd} and Gnd , it is possible to vary the delay by biasing the transistors M1 and M4 in Figure 5(a).

Another approach is to add a transmission gate in the path between the two inverter stages. The current through the transmission gate is (in triode region)

$$I_{TG} = I_{TG_n} + I_{TG_p} \quad (7)$$

$$I_{TG_{n,p}} = k_{n,p} \cdot \left[(V_{bias_{n,p}} - V_{th_{n,p}}) \cdot V_{dd} - \frac{1}{2} V_{dd}^2 \right] \quad (8)$$

$$k_{n,p} = \mu_{n,p} \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L} \quad (9)$$

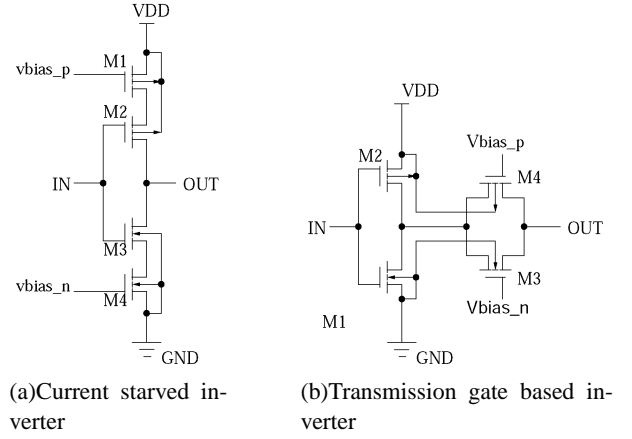


Fig. 5. Different variants for the inverter structure

It is remarkable, that in addition to the desired change of the transmission gate's resistance, the parasitic capacitance towards the load capacitance is varied as well.

IV. DIFFERENTIAL SETUP

For a differential setup of the two mentioned inverter structures, we use a 4 stage ring oscillator. This eliminates the need of a special phase shift circuit to provide the in phase and quadrature phase signals for QPSK demodulation, because the 0° and 90° shifted oscillation can be tapped directly from the oscillator.

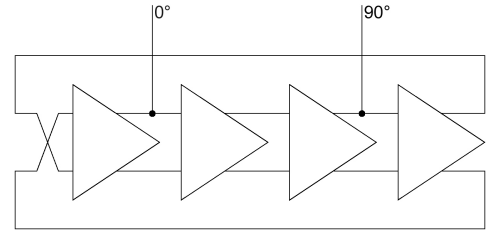


Fig. 6. Differential ring oscillator with even number of stages and I/Q taps

The transmission gate based topology uses a pseudo differential approach (compare figure 7), which essentially is just a second line of inverters, which are driven with differential signals. Nevertheless, this topology has the main benefits of a fully differential approach [Par01]. Simulations show a stable phase difference between both signals of 180° .

The second differential approach is the assisted current starved topology (figure 8, which was modified from a pure pseudo differential version by adding two inverters (M7,M8 and M5,M6) to provide an even more stable phase difference between the two signal paths. It can be shown, that different transistor types with different threshold voltages for the transistors M1-M4 and M5-M8 lead to a very

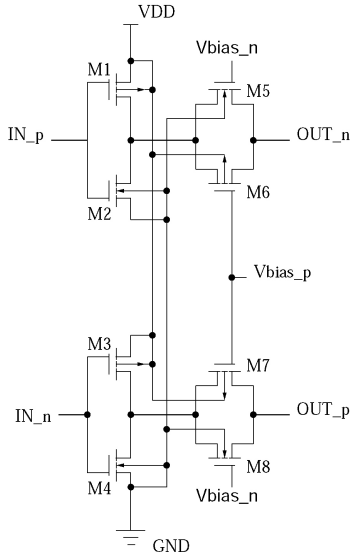


Fig. 7. Differential Transmission Gate Topology

good phase noise behaviour. In the presented simulations M1-M4 have a high V_{th} of about 0.4V and M5-M8 a medium V_{th} of about 0.2 V.

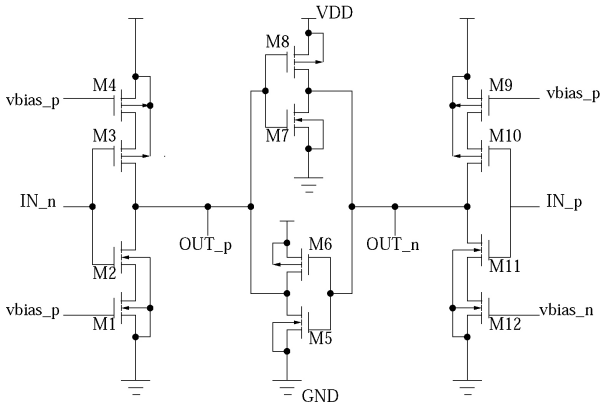


Fig. 8. Assisted Current Starved Inverter

V. NOISE IN INTEGRATED CIRCUITS

Each transistor acts as a noise source, which consists basically of two parts - the thermically induced noise and a frequency dependant part. The thermically induced noise can be displayed as a noisy resistor, which adds noise with the well known relation

$$\overline{u_{N_{Therm}}^2} = 4kTR\Delta f \quad (10)$$

The frequency dependant part (also so called $\frac{1}{f}$ -noise) can be displayed as

$$\overline{u_{N_{freq}}^2} = \frac{K_f}{fC_{ox}} \propto \frac{1}{fWL} \quad (11)$$

This is modeled in the BSIM3v3 model from the University of California, Berkeley as a noise current with

$$\overline{i^2} \propto \frac{1}{L_{eff}^2} \quad (12)$$

for the frequency dependant part and with

$$\overline{i^2} \propto W_{eff}L_{eff} \quad (13)$$

for the thermically induced part.

This leads to the assumption, that it's preferable to make the length of the transistors as large as possible to reduce the noise influence. Enlarging the width to keep the aspect ratio, enlarges the noise from equation 13 and additionally slows down the oscillation by enhancing the load capacitance. The task is now to find the ideal dimensions for the aspect ratio for a minimum power consumption and minimum phase noise.

These noise sources can be thought of as the reasons for a jitter in the oscillation signals which leads to a short-time variation of the oscillation frequency. In the frequency domain, an ideal oscillator has a delta-impuls at it's oscillation frequency. The noise results in a smearing effect around that frequency. This measurement is called „phase noise“ and is displayed in dBc/Hz at a specified offset (Figure 9). It is measured as the noise power in a 1 Hz bandwidth with an offset $\Delta\omega$ to the carriers center frequency ω_c , divided by the power of the carrier.

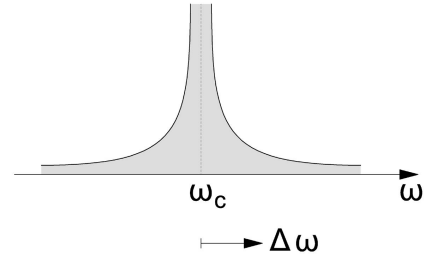


Fig. 9. Schematic display of a typical phase noise measurement

VI. SCHEMATIC DESIGN

The delay of a capacitive loaded CMOS Inverter is

$$-\frac{C_L}{I_D} \cdot dU_{out} = dt \quad (14)$$

$$Q_C = C_L U_{out} \Rightarrow \frac{d}{dt} Q_C = I_D = C_L \frac{d}{dt} U_{out} \quad (15)$$

$$\Rightarrow -\frac{I_D}{C_L} = \frac{d}{dt} U_{out} \quad (16)$$

A look at the capacity that is precharged to V_{dd} , leads

to

$$t_f = \int_{V_{dd}-V_{th}}^{0.9 \cdot V_{dd}} \frac{2C_L}{\beta_n} \cdot \frac{dU_{out}}{(U_{GS} - V_{th})^2} + \int_{0.1 \cdot V_{dd}}^{V_{dd}-V_{th}} \frac{2C_L}{\beta_n} \cdot \frac{dU_{out}}{[2(U_{GS} - V_{th}) - U_{out}]U_{out}} \quad (17)$$

Simplifying equation 17 with $U_{GS} = V_{dd}$ and $V_{th} \approx 0.2V_{dd}$ leads to

$$t_f \approx \frac{4C_L}{\beta_n V_{dd}} \quad (18)$$

The delay $t_{df} = \frac{t_f}{2}$ is therefore

$$t_{df} = \frac{2C_L}{\beta_n V_{dd}} \quad (19)$$

The same calculation for the rise time leads to

$$t_r \approx \frac{4C_L}{\beta_p V_{dd}} \quad (20)$$

and its delay

$$t_{dr} \approx \frac{2C_L}{\beta_p V_{dd}} \quad (21)$$

Two different ideas for the determination of the width ratio for the n-channel and p-channel transistors exist. One for equalizing the rise- and fall-time of the inverter and the other one for minimizing the total delay of one inverter stage.

The load capacitance of one stage is

$$C_L = C_{Gn} + C_{Gp} \quad (22)$$

$$= W_n \cdot L_n \cdot C'_{ox} + W_p \cdot L_p \cdot C'_{ox} \quad (23)$$

$$= W \cdot L \cdot C'_{ox} \left(\frac{\mu_n}{\mu_p} + 1 \right) \quad (24)$$

The total delay t_d of one stage consists of the addition of the rise- (t_r) and fall-time (t_f).

$$t_d = t_f + t_r \quad (25)$$

$$= \frac{4C_L}{\beta_n V_{dd}} + \frac{4C_L}{\beta_p V_{dd}} \quad (26)$$

$$= \frac{4(W_p + W_n)LC'_{ox}}{V_{dd}} \left(\frac{1}{\beta_n} + \frac{1}{\beta_p} \right) \quad (27)$$

Minimizing the delay time by derivation

$$\frac{\partial t_{ges}}{\partial W_p} \Big|_{W_n=const} \equiv 0 \rightarrow \frac{W_p}{W_n} = \sqrt{\frac{\mu_n}{\mu_p}} \quad (28)$$

The other idea is to equalize the rise and fall time and leads immediately to

$$\frac{W_n}{W_p} = \frac{\mu_p}{\mu_n} \approx 0.37 \quad (29)$$

The simulations showed, that equation 29 is preferable (concerning the phase noise) in contrast to dimensioning the transistors for a minimum delay (equation 28).

There is an ideal size for the inverter transistors (Figure 5(a) - M1,M4) for a given size of the transistors used to vary the delay (M2,M4), which minimizes the delay of the inverter and thereby enhances the maximum oscillation frequency, so the length can be maximized later (compare equation 12).

To calculate the optimal width, the length of the transistors (L_{INV}) is set to the minimal value allowed by the technology specifications.

To determine the optimal width, it is sufficient to look at the charge time. Its time constant is

$$\tau_r = (R_{CS,p} + R_{INV,p}) \cdot C_{INV} \quad (30)$$

with the proportionalities for the equivalent resistor and capacity of the inverter stage

$$R_{INV,p} \propto \frac{L_{INV}}{W_{INV}} \cdot R'_{inv} \quad (31)$$

$$C_{INV} \propto C'_{ox} \cdot W_{INV} \cdot L_{INV} + C_{ov} \cdot W_{INV} + C_j \cdot (W_{INV} + L_{INV}) \quad (32)$$

This term is derivated for W_{INV} and set to zero to find the local minimum:

$$\frac{\partial \tau_r}{\partial W_{INV}} = \frac{1}{W_{INV}^2} \cdot (L_{INV}^2 \cdot R'_{INV} \cdot C_j - R_{CS} \cdot W_{INV}^2 \cdot C_{ox} \cdot L_{INV} - R_{CS} \cdot W_{INV}^2 \cdot C_{ov} - R_{CS} \cdot W_{INV}^2 \cdot C_j) \stackrel{!}{=} 0 \quad (33)$$

Equation 33 is solved for W_{INV}

$$\Rightarrow W_{INV} = \frac{1}{R_{CS} \cdot (C_{ox} \cdot L_{INV} + C_{ov} + C_j)} \cdot \sqrt{R_{CS} \cdot R'_{INV} \cdot L_{INV}^2 \cdot C_j \cdot (C_{ox} \cdot L_{INV} + C_{ov} + C_j)} \quad (34)$$

This optimum is based upon the fact, that the width of the transistor not only reduces its resistance, but also enhances its capacity. This is a simplified solution, because essentially the resistance and capacity is additionally time dependant, because the voltage over the transistor changes

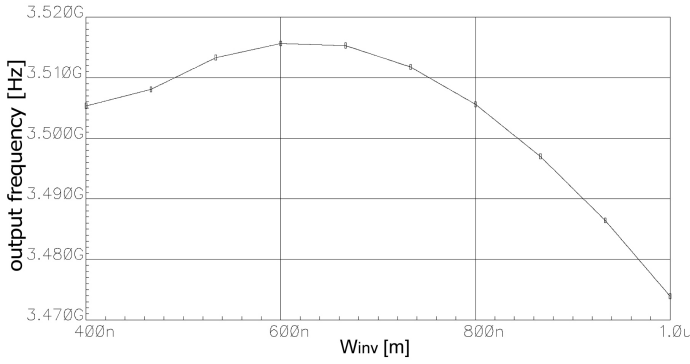


Fig. 10. Determination of the optimal width W_{INV} for the single ended current starved topology

during one period of oscillation. An analytic solution is therefore very complicated and is not necessary here. The simulations prove the existence of the local optimum.

The same calculation and simulation is made for the transmission gate based topology.

$$\tau_r = (R_{TG} + R_{INV,p}) \cdot (C_{TG} + C_{INV}) \quad (35)$$

again with the proportionalities

$$R_{INV,p} \propto \frac{L}{W} \cdot R'_{INV} \quad (36)$$

$$C_{INV} \propto C'_{ox} \cdot W \cdot L + C_{ov} \cdot W + C_j \cdot (W + L) \quad (37)$$

This equation is derivated and set to zero

$$\begin{aligned} \frac{\partial \tau_r}{\partial W} &= \frac{1}{W^2} \cdot (-L \cdot R'_{INV} \cdot C_{TG} \\ &- L^2 \cdot R'_{INV} \cdot C_j + R_{TG} \cdot W^2 \cdot C_{ox} \cdot L \\ &+ R_{TG} \cdot W^2 \cdot C_{ov} + R_{TG} \cdot W^2 \cdot C_j) \stackrel{!}{=} 0 \quad (38) \\ \Rightarrow W &= \frac{1}{R_{TG} \cdot (C_{ox} \cdot L + C_{ov} + C_j)} \end{aligned}$$

$$\sqrt{R_{TG} R'_{INV} L (C_{ox} \cdot L + C_{ov} + C_j) (C_{TG} + C_j \cdot L)} \quad (39)$$

In contrast to the solution of the single ended topology, it is observable that in the transmission gate based topology the parasitic capacity of the transmission gate transistors influences its value for the optimum width (compare figure 11).

VII. DESIGN STRATEGY

The previous simulations and calculations lead to a design strategy for an optimal ring oscillator. The simulation results, which will be shown in the last section, are the results of designs with this strategy.

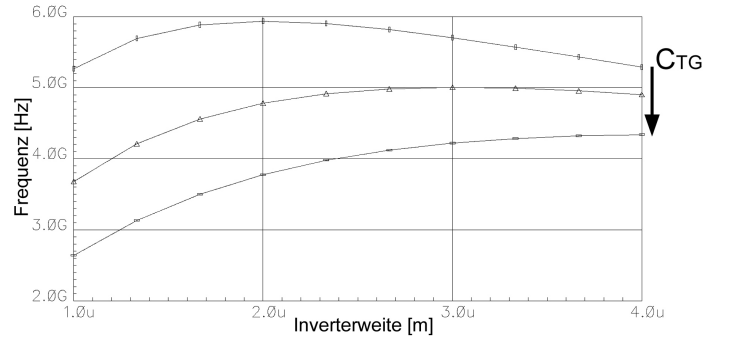


Fig. 11. Determination of the optimal width W_{INV} for different transmission gate capacities

At first, for a given schematic, the ideal width W_{INV} is derived, for which the ring oscillator has the highest frequency. This frequency is then reduced by enlarging the channel length, until it nearly reaches the specification border. With the so specified design, the previously defined parameters (phase noise, power consumption, tuning range) are determined. Depending on these parameters, the width of the delay elements is varied so that the specifications are met with the lowest possible power consumption. In the iterative process it is possible to show that enhancing the power consumption by two leads to a phase noise degradation of about 3 dBc/Hz.

VIII. RESULTS

To compare the phase noise measurements from different topologies with varying power consumption, we approximated a standardised value PN_{norm} , that consist of the measured phase noise related to the power consumption by the equation

$$PN_{norm} = PN + 10 \cdot \log \left(\frac{P}{1mW} \right) \quad (40)$$

The lowest achievable value is therefore the result, for which the phase noise is at the lowest, for a standardised power consumption of 1 mW.

Figure 12 shows the tuning range for both differential topologies. The transmission gate based topology has a very linear characteristic compared to the current starved variant. Nevertheless, the K_{VCO} is rather high ($\approx 1\text{GHz/V}$), due to the limited control voltage and a tuning range of over 1 GHz. To reduce the tuning range and lower the K_{VCO} , a bypass of the transmission gate with an additional resistor might be a possible solution.

In figure 13 the phase noise at a 1 MHz offset is displayed versus the achieved oscillation frequency. The power consumption for this measurement was 8.124 mW.

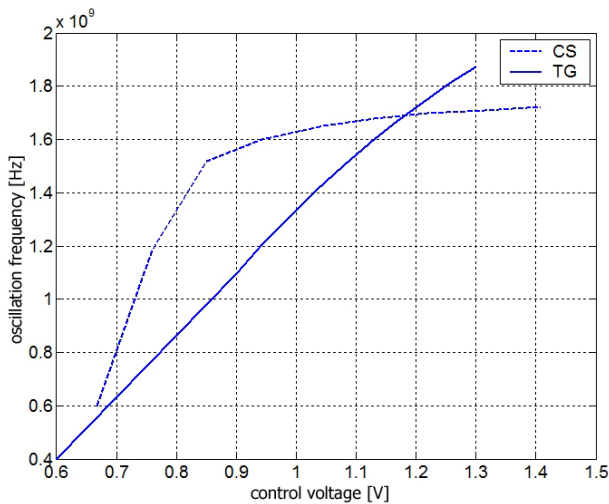


Fig. 12. Comparison of the tuning range for current starved and transmission gate based structures

It can be seen, that the phase noise requirements are achieved over the complete tuning range.

Nevertheless, Table I shows, that the overall power consumption is lower for the current starved structure. At the current state a trade-off must be chosen between achievable linearity (transmission gate based favoured) and minimal power consumption (current starved based version favoured).

IX. CONCLUSION

Four different types of ring oscillators were investigated for the use in global navigation satellite systems. Therefore, specifications for the needful pureness of the oscillation signal were derived. The differential variants of the inverter stages were compared for power consumption, linearity over the tuning range and phase noise. It was shown that it's possible to fulfill the specifications for GPS and GALILEO, with a power consumption of less than 1 mW.

Topology	Tuning Range [Hz]	meas. PN @1MHz	stand. PN	Power Consumption
Current Starved Single Ended	300 M - 1.6 G	-90.68 dBc/Hz	-99.1 dBc/Hz	0.144 mW
Transmission Gate Single Ended	200 M - 2.0 G	-95.17 dBc/Hz	-90.85 dBc/Hz	2.7 mW
Ass. Current Starved	400 M - 2.5 G	-98.17 dBc/Hz	-98.24 dBc/Hz	0.984 mW
Diff. Transmission Gate	300 M - 1.9 G	-101.6 dBc/Hz	-92.5 dBc/Hz	8.124 mW

TABLE I

RESULTS FOR THE DIFFERENT TOPOLOGIES AT A CENTER FREQUENCY OF 1.56GHz

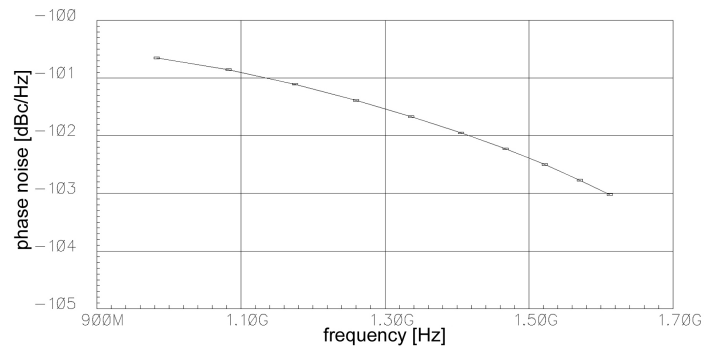


Fig. 13. Phase noise at 1MHz offset versus frequency for transmission gate based structure

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