

A 1.2 V Broadband Low Noise Fully Differential Amplifier in a 65 nm CMOS Technology

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Abstract—A fully differential operational amplifier in a 65 nm CMOS technology is presented. It is designed for low power, low noise and high bandwidth applications. Transistors in a 65 nm CMOS technology suffer from increased short channel effects and noise contribution. Nevertheless, thermal noise density as low as 5 nV/ $\sqrt{\text{Hz}}$ and a $1/f$ -corner Frequency below 1 MHz are achieved. The operational amplifier has a gain of 96dB consuming 6 mW from a 1.2 V supply. Its transit frequency is 700 MHz with a phase margin of 56° .

Index Terms—fully differential amplifier, CMOS, class AB, gain boosting, low noise, low power

I. INTRODUCTION

DIGITAL circuits as embedded in Mp3-players, mobile phones, microcomputers etc. have become an integral part of our life. While the size of these devices is decreasing, their functionality is increasing. Along with this increasing functionality goes the decreasing feature size of modern CMOS processes and the increasing integration of digital circuits. The decreasing feature size comes with faster transistors that allow for higher frequency operation [1].

While digital circuits benefit from a decreased feature size, it becomes a serious problem for analog circuits. The smaller the gate length of a transistor, the more it is influenced by short channel effects. In a 65 nm technology, the Early-voltage of a minimum transistor is below 1 V. As a consequence, the ratio g_m/g_{DS} as a measure for the maximum gain a transistor can attain is very low and has a maximum of 40.

Along with the channel, the gate oxide thickness is decreased and amounts to be as narrow as 1.2...1.8 nm. The supply voltage has to be below 1.2 V to avoid a transistor breakthrough. Moreover, the threshold voltage V_{Th} does not scale by the same amount, decreasing the input voltage range of an amplifier stage. The narrow gate oxide is subject to quantum mechanical gate tunnelling which is source for mismatch, noise and parasitic input current.

As a matter of fact, flicker noise is inversely proportional to gate area [2]. Therefore, a small transistor in a 65 nm technology inherently has a higher flicker noise contribution than a transistor in a technology with taller feature sizes. In conjunction with the lower supply voltage, the signal to noise ratio of analog circuits is decreased.

As an important element of various analog systems like A/D converters, filter circuits or voltage references, an operational amplifier suffers seriously from these drawbacks. The design of analog circuit blocks is becoming even more challenging,

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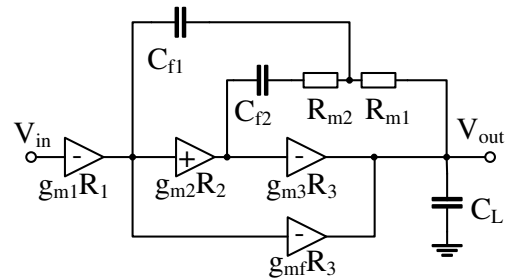


Fig. 1. Structure of the presented Op including compensation scheme.

as both – analog and digital circuit – are integrated on a single chip. In this work a concept for a low noise and low power operational amplifier is presented, that promises high gain and high bandwidth in a 65 nm CMOS technology optimized for digital circuits.

Section II gives an introduction into the amplifier structure. Section III immerses into the circuit implementation and illustrates the circuit blocks. In section IV the simulation results are shown and discussed before in section V conclusions are drawn.

II. OVERVIEW

The structure of the operational amplifier is shown in Fig.1 for simplicity in a single ended version. The operational amplifier basically consists of three cascaded amplifier stages and a parallel feedforward path. For high gain and high speed operation, a very high gain input stage is cascaded with a very fast output stage. Around 80 dB of the 96 dB gain of the amplifier is originated in the first amplifier stage.

The output stage consists of a fast low gain path g_{mf} and a slow high gain path g_{m2}, g_{m3} that combine at the output. This combination allows for fast and accurate push-pull operation.

The overall speed of the amplifier is dictated by the transconductance of the first amplifier stage and its capacitive Miller-effect boosted load. The gain bandwidth product is thus given by

$$GBW = \frac{g_{m1}}{C_{m1}} \quad (1)$$

The whole amplifier is compensated by an enhanced version of the well-known nested Miller compensation scheme [3]. The transfer function of this scheme is given by equation (2). The Resistors R_1, R_2, R_3 and C_3 are the load impedances of the respective amplifier stages. The open loop gain of the operational amplifier A_0 is specified by equation (3).

$$A_v = A_0 \frac{1 + s \left(\left(R_{m1} + R_{m2} + \frac{g_{mf} - g_{m2}}{g_{m2}g_{m3}} \right) C_{m2} + R_{m1}C_{m1} \right) + s^2 \left(R_{m1}R_{m2} + \frac{1 - (g_{m3} + g_{mf})R_{m1}}{g_{m2}g_{m3}} \right) C_{m1}C_{m2}}{\left(1 + sR_1(g_{m2}R_2g_{m3} + g_{mf})R_3C_{m1} \right) \left(1 + sC_{m2} \left(R_{m2} + \frac{g_{m3} + g_{mf} - g_{m2}}{g_{m2}g_{m3}} \right) + s^2C_{m2}C_3 \frac{g_{m2}R_{m1} - 1}{g_{m3}g_{m2}} \right)} \quad (2)$$

If the compensation elements are chosen according to equations (4) to (6), a pole-zero cancellation effect is achieved and the transfer function becomes a single pole system.

$$A_0 = g_{m1}R_1(g_{m2}R_2g_{m3} + g_{mf})R_3 \quad (3)$$

$$R_{m1} = \frac{1}{g_{m3} + g_{mf}} \quad (4)$$

$$R_{m2} = \frac{C_3}{g_{m3}C_{m2}} \quad (5)$$

$$C_{m2} = \frac{g_{m2}}{g_{m3} + g_{mf} - g_{m2}} C_{m1} \quad (6)$$

III. CIRCUIT BLOCKS

A. Input Stage

In Fig.2 the architecture of the input stage is shown. A fully differential folded cascode amplifier is the basic building block of this first stage. The differential stage consists of transistors M_1 and M_2 , transistors M_{12} , M_{13} , M_{22} , M_{23} are cascode devices and transistors M_3 , M_{V3} , M_{11} , M_{21} , M_{14} and M_{24} are current sources. The transistors M_{15} and M_{25} are used for common mode feedback whereas transistors M_{V1} , M_{V2} , M_{V5} , M_{V6} and M_{V7} form a common mode feedforward path.

For the sake of lower equivalent input noise, the input stage consists of p-channel devices. It is well-known that p-channel devices have a lower noise contribution than n-channel devices. On the other hand, n-channel devices allow for higher speed operation.

The design goal of high gain in the first stage can not be achieved easily. By inserting a cascode device into an

amplifier circuit the output resistance increases by a factor of approximately g_m/g_{DS} and along with it the gain of the amplifier stage. Because of the low g_m/g_{DS} of transistors in 65nm technologies, the output resistance of this folded cascode stage is very poor. Along with the low output resistance goes a low gain of in this case approximately 40 dB.

To overcome this drawback, the effect of the cascode devices is improved by the use of gain boosting amplifiers. The gain boosting is realised using two stage simple Miller compensated operational amplifiers. These amplifiers form a feedback path by comparing the voltage at the drain of the cascode transistor with a given bias voltage and control the gate of the cascode device. The cascode transistor appears to have an increased transconductance of $A_v \cdot g_m$, leading to a higher output resistance. The gain of the gain boost amplifiers is designed to be 40dB so that the overall gain of the first stage reaches 80 dB. The stability of this feedback path is ensured if the gain boost amplifiers are designed according to [4].

Although the output resistance of the folded cascode stage is very low compared to former technologies, it still is very high compared to a resistor that is designated for on chip integration. That is the reason why the common mode voltage cannot be sensed using a resistive voltage divider. Despite the drawback of increasing the load capacitance of the first amplifier stage, feedback transistors in the linear region are used to control the common mode voltage of the amplifier. The output voltage swing is limited by the threshold voltage of the feedback transistors M_{15} and M_{25} . Regarding the output stage, this is an unimportant drawback of this solution.

To ensure a reliable startup of the circuit from all possible conditions, a common mode feedforward circuit is implemented. A second path consisting of a second differential pair of reduced size is added. The current through this additional path is proportional to the current in the main differential amplifier path and is used to control the current that is fed into the cascode path. As a result, this operational amplifier has a very high common mode rejection even if the matching of the input stage transistors M_1 and M_2 to the sensing transistors M_{V1} and M_{V2} is very bad.

B. Output stage

The output stage is a rail-to-rail stage using transistors in common source configuration, as shown in Fig.3. The output transistors should not switch off, because it takes long to switch them on again [5]. The output voltage of the first stage is limited to $V_{DD} - V_{Th,p}$, so that p-channel transistors are chosen to be the input transistors for the second stage.

The feedforward controlled output stage consists of two paths. The transistors M_{34} and M_{44} realise the fast path, referred to as g_{mf} in Fig.1. The transistors M_{31} and M_{41} have a diode connected load, mirroring the current into the output node. This way, a class AB characteristic is achieved.

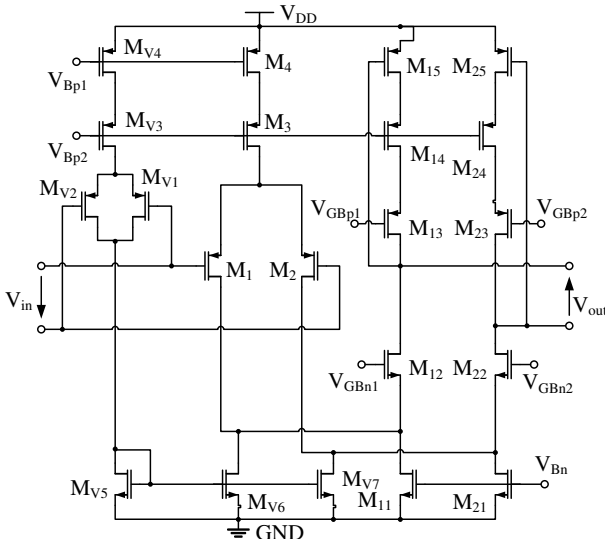


Fig. 2. Fully differential folded cascode stage with common mode feedback and common mode feedforward.

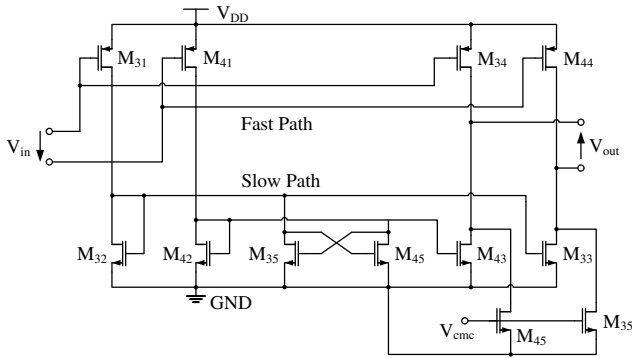


Fig. 3. Class AB output stage.

The common mode voltage at the output node is controlled using a simple resistive voltage divider for common mode sensing and a single stage differential amplifier to compare the common mode voltage to the reference voltage. The output transistors of the slow path are split to feed the common mode control signal into the circuit. Thereby the common mode rejection ratio of the output stage is inherently good. In case of a common mode signal at the input, all output transistors are affected the same way, changing the quiescent current of the output node only. Common mode signals are suppressed, when g_{m44} is equal to $g_{m41}g_{M43}/g_{M42}$. That is a major benefit of the current mirror based class-AB circuit.

The cross coupled pair M_{35} and M_{45} increases the gain of the slow path to be approximately $g_{m41}/(g_{m42} - g_{m45})$. The main reason for this is to compensate for losses that originate in the common mode control circuit. According to basic feedback theory, this circuit is stable as long as $W_{M42} > W_{M45}$.

IV. SIMULATION RESULTS

The proposed operational amplifier was simulated with Cadence Spectre simulator. Fig.4 shows the differential gain frequency response in amplitude and phase. The amplifier has a gain of 96dB with a dominant pole around 10kHz. The gain curve crosses the 0dB at the unity gain frequency of 740MHz with an associated phase margin of 56° .

The noise performance versus frequency is depicted in Fig.5. The thermal noise floor of the amplifier is lower than $5 \text{ nV}/\sqrt{\text{Hz}}$. Flicker noise dominates noise performance for frequencies below 1MHz. This is the lower bound for circuits that use this amplifier in low noise bandpass filter applications.

Fig.6 depicts the performance of the amplifier under different common mode voltages. The speed of the amplifier is higher than 700 MHz until the common mode input voltage reaches 0.75 V. Increasing the common mode input voltage further, decreases the unity gain frequency of the amplifier rapidly but rests above 100 MHz for another 150 mV. The decreasing unity gain frequency goes along with the decreasing gain of the amplifier, that is caused by the decreasing current through the differential pair of the input stage.

The transient behaviour of the amplifier is simulated by putting the operational amplifier in unity gain feedback configuration. The results of the simulation provide information

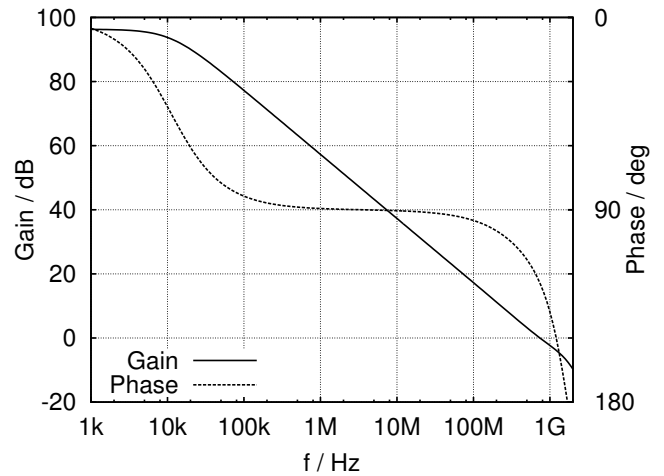


Fig. 4. Amplitude and phase frequency response.

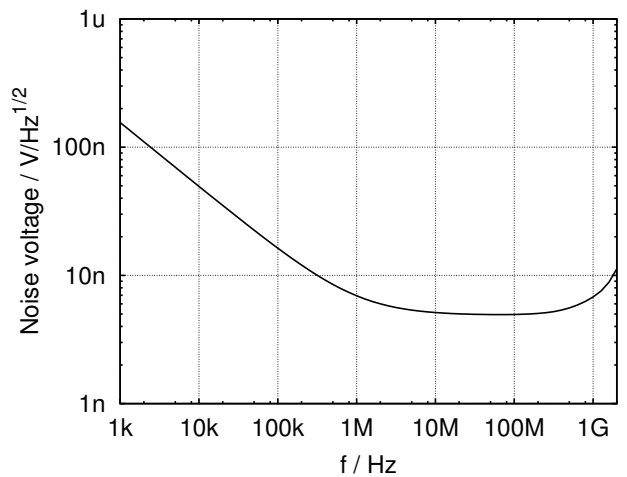


Fig. 5. Equivalent input noise voltage versus frequency.

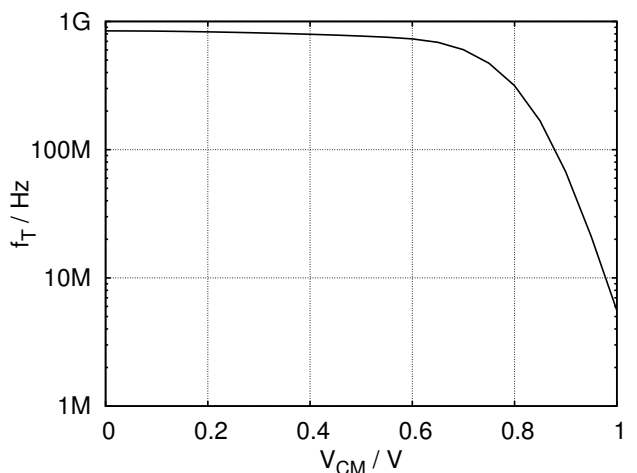


Fig. 6. Transit frequency versus common mode input voltage.

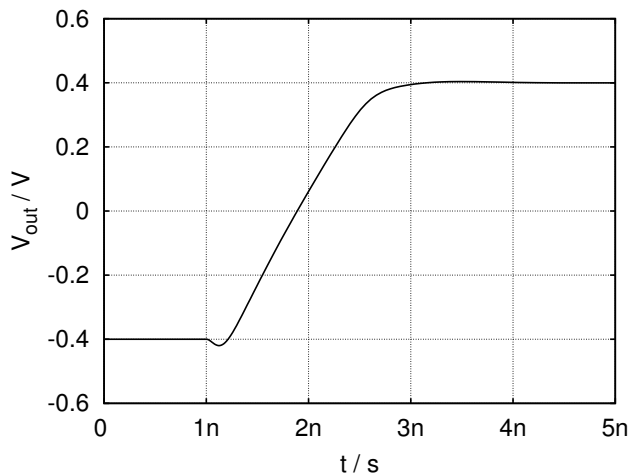


Fig. 7. Step response for an input voltage step of 0.8 V.

TABLE I
SIMULATION RESULTS SUMMARY.

Power consumption	6 mW
Voltage gain	96 dB
Phase margin	56°
Unity gain frequency	700 MHz
Slew rate	570 V/ μ s
Input common mode range	0 . . . 0.75 V
Common mode rejection ratio	146 dB
Power supply rejection ratio	110 dB

about the stability and the large signal behaviour of the amplifier. A 0.8 V voltage step at 1 ns is applied to the input of the amplifier in resistive feedback unity gain configuration. The results in Fig.7 show, that after a small negative peak caused by feedthrough, the voltage rises with a slew rate of 570 V/ μ s. Thereby the overshoot never exceeds 1 percent of the end value.

Due to the common mode control circuits, the common mode gain of the amplifier amounts to be -50 dB at DC and never exceeds the 0 dB border. From that follows a common mode rejection ratio of 146 dB and an unconditionally stable common mode feedback behaviour. The PSRR is simulated to be $PSRR^+ = 110$ dB at DC and is equal to $PSRR^+ = 70$ dB at 1 MHz. The $PSRR^-$ is 2 dB lower over the whole frequency range of interest.

The supply voltage can be as low as 1.1 V and a operating temperature range of -40° to 125° is attained

The output voltage range of the output stage $V_{out,max}$ amounts to ± 1.16 V and provides a maximum output current of 7 mA.

V. CONCLUSION

The design of the proposed operational amplifier shows the challenges of analog design in modern sub-micron technologies. While it is rather simple to create a high speed amplifier,

it is difficult to achieve high gain. The complexity and with it the current consumption of high gain amplifiers increase.

In addition to the increased current consumption comes the larger area usage. In [6] a operational amplifier based on a comparable concept is used. The authors come to the conclusion, that in a 65 nm technology the supporting circuits consume more area than the actual amplifier itself.

In this work a high gain operational amplifier has been designed, that allows for high speed operation. The main design goal of low noise operation in a modern CMOS technology optimized for digital circuitry is accomplished. The low supply voltage in addition to a comparatively large threshold voltage limits the input common mode operating range of the transistors. Anyway this operational amplifier has a large common mode input range of constant operation.

Furthermore, a low noise operation is achieved with a very low equivalent input noise voltage. This is essential to attain a high signal to noise ratio SNR.

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