

High-Speed Sigma-Delta Converters

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Abstract—High-speed sigma-delta ADCs sampling in the GHz frequency range can replace most of the analog circuitry used for channel selection and down conversion in wideband communication systems. This paper presents the design techniques of such high-speed sigma-delta ADCs and discusses the limitations such as quantizer metastability, quantizer delay and DAC non-idealities.

Index Terms— CMOS, Sigma-Delta Modulators, Multi-bit Quantization, Wideband, Power efficiency.

I. INTRODUCTION

NANOMETER CMOS technologies enable data converters with increased speed. Sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADC) trade sampling speed for resolution and can relax requirements on the analog circuits compared to nyquist-rate ADCs. Therefore, $\Sigma\Delta$ -ADCs can benefit from the high f_T of nm-CMOS technologies. Due to the oversampling operation of $\Sigma\Delta$ -ADCs, the internal quantizer may reach sampling frequencies (f_s) in the order of GHz. At these frequencies, the delay of the quantizer degrades the stability of the sigma-delta modulator, and this is one of the main bottlenecks for expanding the signal bandwidth in $\Sigma\Delta$ -ADCs.

A $\Sigma\Delta$ -ADC can be designed by using switched-capacitor (SC) circuit techniques; however, the sampling speed of the modulator cannot exceed the unity gain frequency of its operational amplifiers (opamp) [1], [10]. On the other hand, the sampling speed of a continuous-time (CT) sigma-delta modulator is not limited by the unity gain frequency of its opamp. Therefore, the continuous-time approach is preferred in the design of high-speed sigma-delta ADCs.

The design of a sigma-delta modulator is not straightforward and requires extensive simulations to verify the stability of the modulator. As the sampling frequency of the $\Sigma\Delta$ -ADC increases, the second order effects such as parasitic poles in the loop filter and the delay of the quantizer start to effect stability of the modulator. Consequently, both the architectural and circuit level design choices must be modified to overcome these problems.

CT $\Sigma\Delta$ -ADCs achieved sampling speeds ranging up to 40 GHz over the last decade and presented in Table-I. The design techniques used in such high-speed sigma-delta

modulators are presented in this paper. Section II presents the overview of the high-speed $\Sigma\Delta$ -ADCs and discusses the architectural trade-offs. The limitations of high-speed sigma-delta modulators such as quantizer metastability, quantizer delay and DAC non-idealities are discussed in section III, and conclusions are presented in Section IV.

II. HIGH SPEED SIGMA-DELTA MODULATORS

A. Applications

High-speed sigma delta modulators are widely used in wideband communication systems, radar receivers, and digital radio receivers. In these applications, the input signal is either directly sampled at the antenna with little or no filtering or down converted to an intermediate frequency (IF) and then digitized. In both cases, $\Sigma\Delta$ -ADCs are popular because they can achieve high dynamic ranges and have inherent anti-alias filtering. Recently published high-speed modulators digitize bandwidths up to 1000 MHz [1], [3], [5], [11].

B. IC Fabrication Process

High-speed $\Sigma\Delta$ -ADCs require an IC process, which can enable circuit design in the GHz frequency range. From Table-I, it can be observed that the majority of the high-speed $\Sigma\Delta$ -ADCs use heterojunction bipolar transistor (HBT), high electron mobility transistor (HEMT), SiGe BiCMOS processes. The designs in late 1990s choose HBT and HEMT processes to achieve high sampling speeds, however recently, SiGe processes ($f_T \sim 200$ GHz) are used to increase the sampling frequency of the ADC. Recent advances in nm-CMOS have pushed f_T above 170 GHz [16] and nm-CMOS can be used to design high-speed sigma-delta ADCs operating in the GHz frequency range. Compared to SiGe, nm-CMOS solution can lower the manufacturing cost and enable additional digital functionality.

C. Sigma-Delta ADC Architecture

There are two main $\Sigma\Delta$ architectures: single-loop and cascaded. Figure 1 illustrates a general model of a single-loop sigma-delta modulator, which consists of an n^{th} order loop filter $H_L(s)$, a quantizer, and a DAC. Moreover, a cascaded architecture consists of two or more single-loop sigma-delta modulators where the input of the next stage modulator is the quantization noise of the previous stage modulator. The outputs of the single-loop modulators are combined by using a digital noise-cancelling filter. Even though the cascaded

TABLE I
HIGH SPEED SIGMA-DELTA MODULATORS

Ref.	Year	Technology	Architecture	f_T [GHz]	f_s [GHz]	BW [MHz]	OSR	Power [mW]	DR [dB]	SNDR [dB]	FOM
[1]	1995	HBT	2LP	70	3.2	50	32	1000	50	55	21.8
[2]	1997	HBT	4BP	80	4	62.5	32	1400	45	44	86.5
[3]	1998	HEMT	2LP	30	5	100	25	400	43	39	27.5
[4]	2001	HBT	2LP	200	18	990	9	1500	35	33	20.8
[5]	2003	HBT	2LP	205	8	250	16	1800	-	40	44.1
[6]	2004	HBT	4BP	130	4	60	33	3500	-	48	142.1
[7]	2004	CMOS	2LP	40	2	1.2	810	18	80	79	1.0
[8]	2006	HBT	4BP	-	4	180	11	7700	48	40	261.8
[9]	2007	SiGe	4BP	150	40	200	100	1600	53	52	12.3
[10]	2007	SiGe	4BP	47	3.8	1	1900	75	65	58	57.8
[11]	2008	SiGe	2LP	170	40	1000	20	650	38	37	5.6

2LP: 2nd order Lowpass Loop filter, 4BP: 4th order Bandpass Loop Filter

architecture is capable of achieving wider bandwidths for a given sampling frequency, the single loop architecture does not require a high-speed digital noise-cancelling filter and the DC gain requirement of the opamps in the single-loop architecture is more relaxed. Therefore, the single loop architecture can achieve sampling frequencies in the GHz frequency range.

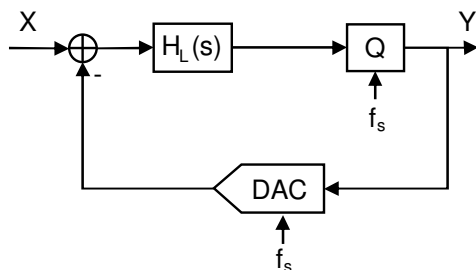


Figure 1 Single Loop Sigma-Delta Modulator

The signal-to-noise ratio (SNR) vs. oversampling ratio (OSR) of a single-bit sigma-delta modulator is shown in Figure 2. The optimal loop filter order of a single-bit single-loop sigma-delta modulator depends on the OSR and the target SNR. For example, the majority of the high-speed $\Sigma\Delta$ -ADCs in Table-I use a 2nd order loop filter with an OSR between 10 and 32 and achieve SNR around 50dB.

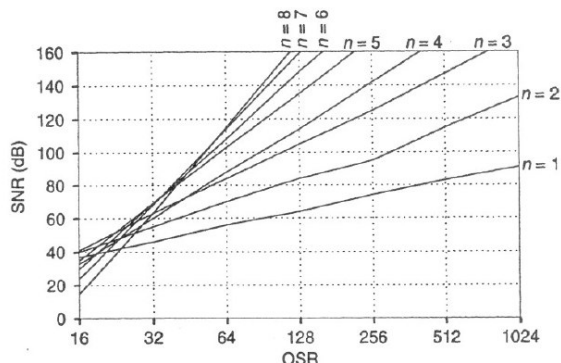


Figure 2 Maximum SNR achievable by modulators of order n with coincident zeros, as a function of oversampling ratio [17].

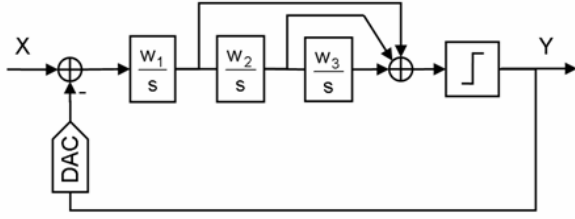
The resolution of a high speed sigma-delta modulator can be increased by using a multi-bit quantizer followed by a multi-bit DAC. A multi-bit quantizer can relax the requirements of the loop filter and reduce the OSR, however the design of an N-bit quantizer requires 2^{N-1} comparators and DAC units which operates at GHz sampling speeds. The resolution gained by a multi-bit quantizer can be reduced by the mismatches among the channels of a multi-bit DAC. In order to correct these mismatch errors, the multi-bit DAC can be trimmed or a dynamic element matching block can be introduced between the quantizer and the DAC. In both cases, the additional blocks increase circuit complexity and power consumption. [8] uses a 3-bit quantizer where a noise shaping technique is proposed, which can dynamically update the reference voltage connected to each comparator. This technique shapes the DAC mismatch errors without introducing an additional delay to the operation of the quantizer and DAC but the ADC dissipates 7.7W.

Due to the above-mentioned drawbacks of a multi-bit quantizer, 1-bit latched comparator designed in current-mode logic is used as a quantizer for achieving high-speed sampling. The quantizer should complete its operation less than a clock period and must generate a valid output to operate the DAC. Errors introduced during the operation of the quantizer such as metastability and signal dependent quantizer delay can degrade the SNR considerably and will be further discussed in Section-III.

A 1-bit DAC can be designed as a current steering differential amplifier, which achieves higher sampling speeds than the resistor-ladder DAC architectures [18]. Both return-to-zero (RZ) and non-return-to-zero (NRZ) format can be used in DACs. The designs with NRZ format relies on the differential matching of the DAC topology and in [1] it is reported that the DAC output rise and fall waveforms are inherently symmetric. On the other hand, designs with the RZ DAC demonstrate that SNR loss due the possible quantizer metastability errors can be minimized and most importantly,

the sigma delta modulators are stable for quantizer delays less than half of the sampling period [5].

(a) 3rd order Feed-Forward $\Sigma\Delta$ Modulator



(b) 3rd order Feedback $\Sigma\Delta$ Modulator

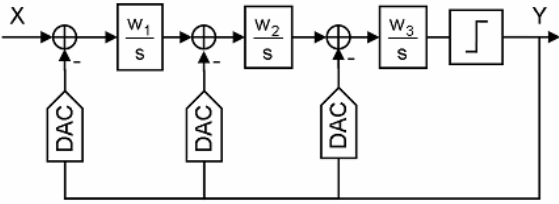


Figure 3 Feedback and Feed-Forward Architecture for a 3rd order Sigma-Delta Modulator

Once the order of loop filter and the number of quantizer bits have been decided, two different types of loop filter architectures can be considered: feedback and feed-forward as shown in Figure 3. The same loop-filter transfer functions can be designed using these two filter architectures. The feed-forward architecture uses only one DAC but requires a high-speed summation node, which introduces a parasitic pole at the output of the loop filter. On the other hand, feedback architecture have better anti-aliasing filter but requires n-DACs, where n is the order of the loop filter.

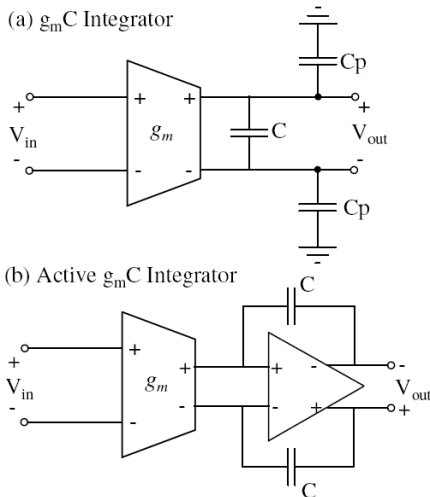


Figure 4 g_mC and active g_mC Integrators

The last critical block in the design of the high-speed sigma delta modulator is the continuous-time integrators. There are many integrator topologies such as: a transconductance amplifier-capacitor (g_mC) or an active g_mC as shown in Figure 4. The g_mC based integrators are easily tunable, and

can achieve high unity gain frequency, expressed as $\omega_u = g_m/C$. For sigma-delta converters where the sampling frequency is a fraction of the f_T , g_mC integrators are a natural choice for implementing the loop filter. However, this type of integrator is sensitive to the parasitic capacitances C_p and the non-linear voltage-to-current conversion limit the linearity of the integrator. Active g_mC , based integrator shown in Figure 4.b can be used to overcome the drawbacks of the g_mC filters. This architecture is less sensitive to the variations in C_p , however the linearity of the integrator is still limited by the transconductance amplifier.

Bandpass loop filters can be designed by using g_m -LC resonators in which the integrator capacitance is replaced by a LC tank resonator. By tuning the g_m , the bandpass sigma-delta modulator can adjust its bandwidth. However, additional circuitry might be required to compensate the losses of the on-chip inductors.

D. Oversampling Ratio (OSR)

Sigma-delta modulators trade sampling speed for resolution and for a second order modulator every doubling of f_s will result in 15 dB of SNR increase. In [12] the dynamic range (DR) of a second order sigma-delta is modeled as

$$DR \approx 15 \log_2(OSR) - 13 \quad (1)$$

and given the SNR values in Table-I one can calculate the minimum required OSR factor for each design. A *useful* OSR can be defined based on this calculation. For example, [4] and [11] achieve a dynamic range of 35 dB and 38 dB and bandwidths of 990MHz and 1000MHz respectively. From (1) it is clear that for a dynamic range of 38 dB, an oversampling ratio of 10 is enough, which is used by the design in [4]. This calculation shows us the efficiency of the OSR for a measured SNR. However, this approach can only be applied to lowpass modulators. For bandpass modulators the result might lead to a subsampling bandpass sigma-delta modulator, which has a poor SNR performance due to aliasing of high frequency components into the signal bandwidth.

The *useful* OSR for a high-speed second order lowpass sigma-delta modulator targeting 50dB signal-to-noise ratio is around 16 [12]. This trend can also be observed in high-speed sigma delta modulators reported in Table-I and DR does not improve for increasing OSR because SNR is limited by the non-idealities such as quantizer delay or clock jitter.

E. Power Consumption

The sigma-delta modulators designed in HBT and HEMT technologies require supply voltage ranging from 3.3V to 10V, and these modulators consume 400mW to 7.7W [1-6],[8]. The power consumption of the decimation filter is not mentioned and more often, a high-speed demultiplexer was designed to parallelize the output and enable off-chip signal processing. On the other hand, the sigma delta modulators fabricated using SiGe consume less power due to the reduced supply voltage. [9], [11] report the power consumptions of the circuit blocks such as: loop filter, quantizer, DAC, and clock

tree. For sampling frequencies reaching 40 GHz, only 10% of the power is dissipated by the loop filter. Higher supply voltage and increased sampling speed raise the power consumption of the clocked circuit blocks drastically, which is proportional to $f_{clk} \cdot C \cdot V^2$.

From Table-I, it can be observed that the low pass sigma-delta modulators have lower figure-of-merit (FoM) than the bandpass sigma delta modulators, where FoM is expressed as:

$$FoM = \frac{P_{DC}}{2^{ENOB} \times 2BW} \quad (2)$$

with P is the power dissipation of the ADC, ENOB is the effective number of bits. Low pass sigma delta modulators are more power efficient than the bandpass counterparts. On the other hands, bandpass sigma delta modulators can simplify system level architecture, therefore saving additional power which is not included in the FoM.

III. LIMITATIONS OF HIGH-SPEED SIGMA-DELTA MODULATORS

High-speed sigma-delta modulators have three common limitations, which are quantizer metastability, quantizer delay, and clock jitter.

A. Quantizer Metastability & Delay

In a 1-bit latched comparator, there exist two valid output states: +1/-1, which represents the sign of the input signal. For an input signal equal or close to 0, there is a third output state which is called the metastable state. A quantizer operating in this state can not generate a valid output. Practically, the circuit noise will force the quantizer output to one of its valid states, however this operation might take more time than the clocking period of the quantizer. In this case, the output of quantizer is invalid, and the circuitry following the quantizer can not operate correctly.

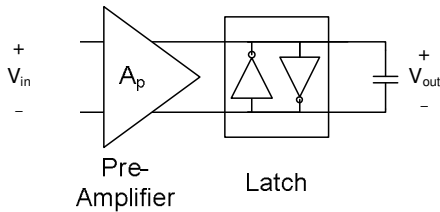


Figure 5 Comparator Model with a pre-amplifier and a latch

Any comparator can be modeled as a preamplifier followed by a latch as shown in Figure 5. The probability of a metastable state in a quantizer is

$$P_m = \frac{2 \cdot (2^N - 1) \cdot V_L}{V_{in} \cdot A_{comp}} \quad (2)$$

where N is the number of quantizer bits, V_{in} is the input voltage range, V_L is the minimum output signal swing for a

reliable digital signal processing [13]. A_{comp} is the voltage gain of the quantizer, which is given by

$$A_{comp} \approx A_{pre} \cdot A_{latch} \cdot e^{(T_{latch} - t_{pre})/t_{reg}} \quad (3)$$

A_{pre} and A_{latch} are the voltage gains of the preamplifier and latch respectively, t_{pre} is the delay of the preamplifier, t_{reg} is the regeneration time constant of the latch and T_{latch} is the time period allowed for latching.

The probability of a metastable state can be reduced by increasing the comparator gain or by decreasing the number of quantizer bits. For a given T_{latch} , the achievable comparator gain is fundamentally limited by t_{reg} which is proportional to $1/f_T$. Due to this limitation, the high-speed sigma-delta modulators (except [8]) use a single-bit quantizer, which is also inherently linear.

The third option, which is often used in high-speed flash converters, is to cascade additional latch stages to further increase T_{latch} . However, this technique delays the input signal of the DAC, which results in larger voltage swings at the outputs of the integrators in the loop filter. These outputs can clip and decrease the SNR.

It has been shown that comparator delays up to 1-clk period delay can be compensated in a sigma-delta converter without any SNR loss [5, 6]. In Figure 6, the technique used to compensate the quantizer delay (T_Q) is illustrated. In this topology, an additional DAC is introduced which bypasses the loop filter and directly connects the quantizer output to its input. The DAC and loop filter coefficients can be scaled such that the input signal of the quantizer with and without T_Q matches exactly.

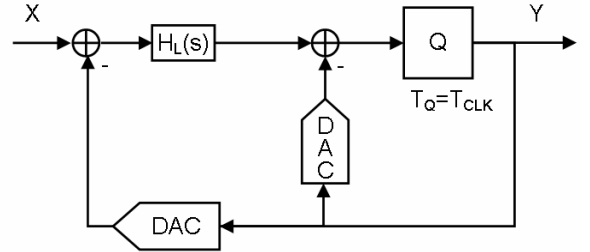


Figure 6 Sigma-Delta Modulator with Quantizer Delay Compensation. (T_Q is the delay of the quantizer, which is equal to 1-clock period.)

At very high sampling speeds, a quantizer may require more than 1-clk period to generate a valid output. In this case, an extra DAC around the quantizer can still be applied but the SNR loss is inevitable. [5], [11] study quantizer delays more than 1-clk period and [7] applies 2.5-clk period delay to reduce the metastability errors of the quantizer. Figure 7 illustrates the effect of quantizer delay on the dynamic range of a second order sigma-delta converter [11]. It is shown that even if the quantizer gain increases with the quantizer delay, the dynamic range decreases almost 5dB for every 1-clk period delay. Therefore, for a high-speed sigma-delta modulator an optimum quantizer delay can be found. On the other hand, the reported power spectrums exhibit 10 to 15 dB peaking, which is located approximately between $f_s/5$ and

$f_s/4$. This peaking in the spectrum puts additional constraints on the design of the decimation filter and further reduced useful OSR.

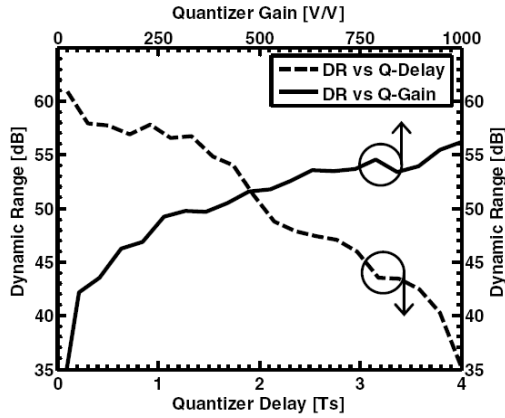


Figure 7 DR versus quantizer delay and gain [Fig. 5 in 11]

B. Clock Jitter

Clock jitter can be modeled as an additional error source at the DAC output of a sigma-delta modulator. The error introduced by the clock jitter depends on the input signal amplitude and frequency. The SNR of a lowpass sigma-delta modulator in the presence of clock jitter is calculated in [19] and is given as:

$$SNR = 10 \log_{10} \left(\frac{OSR}{4 \cdot f_s^2 \cdot \sigma_j^2} \right) \quad (4)$$

where σ_j is the rms value of the clock jitter.

The SNR of a bandpass SDM is calculated in [15] and repeated here.

$$SNR = 10 \log_{10} \left(\frac{OSR}{4 \cdot f_s^2 \cdot \sigma_j^2} \cdot \text{sinc} \left(\frac{w_o}{2 \cdot f_s} \right) \right) \quad (5)$$

where w_o is the center frequency of the bandpass filter.

In both expressions, the OSR increases the SNR for a given clock jitter. Bandpass sigma delta modulators generally have smaller SNR for a given σ_j because w_o is positioned close to f_s and the $\text{sin}(x)/x$ is less than 1.

The high-speed $\Sigma\Delta$ -ADCs in Table-I use off-chip clock sources to test the effect of clock jitter and report that SNR is not limited by the clock jitter. As discussed in the previous section, the quantizer non-idealities are limiting the achievable SNR by these designs. On the other hand, a sigma-delta modulator, which uses a lower OSR to increase the signal bandwidth, can be limited by the clock jitter. In that case, a switch-capacitor DAC [14], or a multi-bit quantizer can be used to reduce the effect of clock jitter. In that case, a switch-capacitor DAC [14], or a multi-bit quantizer can be used to reduce the effect of clock jitter. The first technique will increase the power dissipation of the loop filter and implementing a switch-capacitor DAC might be impossible at high sampling frequencies. On the other hand,

the advantage of using a multi-bit quantizer can be limited by the increased metastability errors.

IV. CONCLUSIONS

The sigma-delta ADCs, which trade sampling speed for resolution, can benefit from the speed advantages of nm-CMOS technologies. The single loop architecture with 1-bit quantizer is suitable for GHz sampling frequencies. A 2nd order loop filter can be used to achieve 60 dB SNR with a moderate OSR between 16 and 32. Both feedback and feed-forward loop filter architectures are used in high-speed sigma-delta ADCs, and the loop filter architecture is based on architectural level specifications such as: power budget, anti-aliasing, out-of-band interferers, etc. $g_m C$ based integrators are preferred because they can achieve high bandwidths but the effect of parasitic poles should be carefully simulated.

At high sampling speeds, the maximum SNR achievable by the $\Sigma\Delta$ -ADCs is limited by the quantizer delay and metastability, and the clock jitter. Quantizer delays up to 1-clk can be compensated in sigma-delta modulators, but quantizer delays larger than 1-clk period will reduce the SNR considerably. Using high OSRs can relax the clock jitter requirements; however the errors introduced by the quantizer become more dominant at GHz sampling frequencies.

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