Tuning of DRIE process for Capacitive Sensor in Inkjet Nozzle

J. Wei[1], T. Chu Duc[1], M. van der Velden[2] and P. M. Sarro[1]

Abstract—**This paper presents a study on DRIE (Deep Reactive Ion Etching) of silicon for integration of silicon-based vertical electrodes on channel sidewalls, aiming at meniscus monitoring in inkjet nozzles. The 3D micromachining process contains different DRIE steps. The specific requirements of each step are discussed and the influences of the main process parameters on the characteristics of the etched structures are described. By properly modifying the etching process parameters, correct recipes are found that allow to successfully address the issues encountered in the fabrication process of electrically insulated vertical electrodes for a capacitive sensor integrated in the inkjet nozzle.**

Index Terms—**3D MEMS, deep reactive ion etch, microfabrication**

I. INTRODUCTION

Inkjet technology, capable of dispensing pico-liter level droplets contactlessly on a wide range of substrates, has spread its application from document printing to many other fields, such as biomedical sample handling and electronics fabrication. However, current inkjet systems lack the mechanism to detect the generation of droplets directly. Consequently, the defects in the printed pattern, due to the failure of jetting a droplet from a nozzle, will be ignored, causing a reliability issue. For these reason, a capacitive sensor integrated in the inkjet nozzle is proposed [1], which monitors the movement of the ink meniscus, offering a feedback possibility for better precision and reliability.

To fabricate the proposed sensor, schematically depicted in Fig.1, a new process is developed to form vertical silicon electrodes on the sidewall of the nozzle channel. First, a thick oxide layer is created selectively on the front surface of the silicon wafer. After the substrate preparation, conventional IC processes can be performed for electronic structures and interconnections. Finally, the microfluidic channels are etched from both sides of the wafer. At the same time, vertical silicon electrodes are formed and separated by using the pre-defined oxide walls.

Two DRIE steps are involved in this process, and each step has different goal and requirement. Therefore, the DRIE plasma conditions need to be carefully tuned. The main process parameters are altered in order to achieve the desired etching profile and characteristics for each step. The DRIE processes are studied in detail and the specific issues discussed in detail. The obtained recipes are not limited to this application, as the same tuning principle can be used in general purposes.

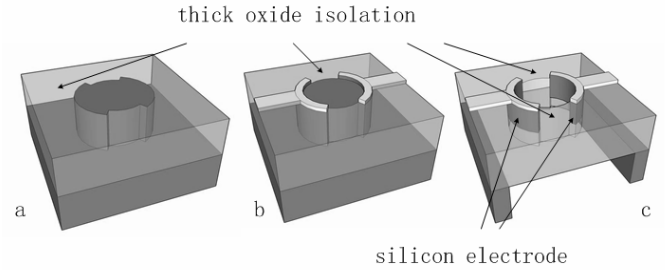
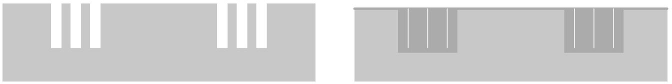


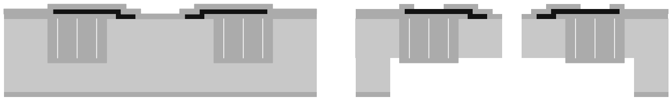
Figure 1. Fabrication of electrically insulated vertical electrodes on the nozzle channel sidewalls.

II. EXPERIMENT

The sensor fabrication flow is presented schematically in Fig.2. First, deep silicon trenches are etched with Deep Reactive Ion Etching (DRIE) and transferred into thick oxide layer by thermal oxidation (Fig.2a & 2b). The wafer surface is then planarized, and further processed with conventional IC technology up to the metallization step, creating electrical paths to the electrodes (Fig.2c). Finally, a fluidic channel is etched by DRIE on the both sides of the wafer, and the remaining silicon blocks, surrounding the channel, function as separated electrodes (Fig.2d).



a) HAR trench etching b) oxidation and surface palanrization



c) aluminum connection d) nozzle etching

Figure 2, The process flow with the two DRIE etching steps used to fabricate the sensor.

The two DRIE steps involved in this process need to fulfill quite different requirements. The high aspect ratio (HAR) deep trenches (see Fig. 2a) need to be etched into bulk silicon with a slight negative sidewall angle but without undercuts, as

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demanded by the subsequent oxidation process. The etching of the nozzle (see Fig. 2d), on the other hand, needs to produce a straight (or slightly negative) sidewall and a small undercut to ensure the electrical isolation between the silicon electrodes.

To meet these challenging requirements, the DRIE plasma conditions need to be carefully tuned. In our experiment, a standard DRIE recipe (*Recipe A* in Table I), which offers acceptable result in general DRIE etching, is used as starting point.

TABLE I

DRIE RECIPES USED IN THIS PAPER

Recipe	Steps	SF_6/C_4F_8 sccm	Energy W	Time s	T °C	Dist.[a] mm
A	Passivation	0/280	1500	2	10	200
	Etching	400/0	1500	5		
B	Purge	0/0	0	3	-10	200
	Passivation	0/140	1500	2		
	Etching	200/0	1500	5		
C	[b]Etching	400/0	1500	5	10	150
	Passivation	0/280	1500	2		

[a] The distance between the substrate holder and the plasma source.

[b] In this recipe, the DRIE cycle starts with a SF_6 etching step.

Based on DRIE plasma etching mechanism [2], correct recipes with desired etching profile, sidewall angle, undercut, sidewall erosion and aspect ratio can be found, by tuning the main process parameters, such as gas flow, chamber pressure, etching sequence and temperature. The DRIE process is performed in an Alcatel Microsystems AMS 100 system [3] in this experiment.

A. *Deep trench etching for thick layer oxidation*

To create a thick oxide layer, an array of HAR trenches is etched into the silicon wafer, and a thermal oxidation is performed by driving oxygen into the deep trenches to oxidize the Si structure laterally.

There are three important issues that need careful consideration:

1) The profile of the thick oxide layer should have a negative sidewall angle in order to insure reliable electrical isolation between the electrodes [4].

2) The selected bulk Si should be oxidized completely, so that an effective isolation from the substrate can be achieved as well.

3) The openings of the pre-etched trenches should be sealed without voids during oxidation, in order to allow further micromachining on the surface.

These issues translate in specific requirements which the DRIE process needs to satisfy. Using *Recipe A,* unsuccessful oxidation results are achieved, as can be seen in Fig.3. Two problems can be observed in these SEM pictures. First, undercuts appear at the opening of the HAR trenches. This unexpected erosion on the sidewall surface decreases the width of the silicon structure, causing a serious problem when attempting to close the trench opening by oxidation. Second, a positive sidewall angle appears at the bottom of the HAR trench, causing fins-like residuals after oxidation. Such residuals may degrade the future isolation between the electrodes.

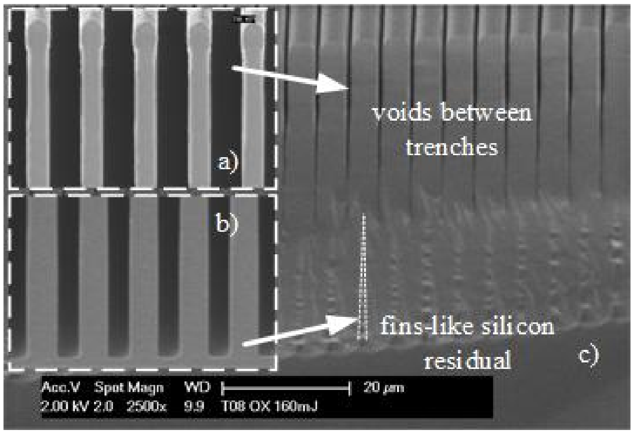

Figure 3. SEM images of an unsuccessful DRIE trench etching, leading to an unacceptable oxidation result. a) DRIE undercut due to the erosion of passivation layer at the opening of the HAR trench; b) the shrinkage of the trench width at the bottom due to the positive sidewall angle; c) voids in the oxide at the trench opening and silicon residuals at the bottom.

In order to achieve a successful HAR etching with a negative sidewall angle and no undercut, three important process parameters are modified as described here.

The pressure in the reaction chamber should be kept at a lower level, so that the ions and radicals have a longer mean free path. Thus an effective etching can be achieved at the bottom of the HAR trenches due to the sufficient exchange of reactant and product, leading to a slight negative sidewall angle. The pressure control can be achieved by either increasing the pump speed, or reducing the reactant gas flows. In the modified recipe (*Recipe B* in Table I), the flow of both gases has been decreased to half of the original value, thus the process pressure has been reduced, while the balance between etching and passivation is kept unchanged.

A good quality of passivation polymer layer at the trench opening is essential to avoid undercut. A general Bosch process cycle contains two steps: etching and passivation. During the passivation step, a polymer layer is coated on the sidewall, which should be thick enough to protect the silicon sidewall from chemical erosion in the following etching step. However, these two opposite steps can not be switched ideally in practice. At the beginning of the passivation step, the etching radicals still present in the plasma, degrade the formation of the passivation layer. To overcome this, a purge step is inserted between the etching and the passivation step, pumping all the etching gases away before the passivation starts. This extra step ensures a thicker polymer deposition, especially on the sidewall close to the trench opening, forming an extra protection against undercut.

The temperature during the reaction influences the erosion of the passivation layer significantly. A low temperature environment will strengthen the passivaiton layer against the ion bombardment on the sidewall. For this reason, the etching process is performed at - 10ºC.

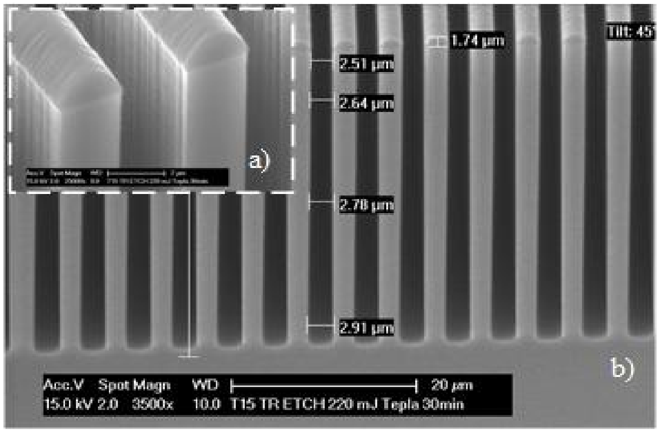

Figure 4. SEM images of a successful DRIE trench etching with slightly negative sidewall angle and no undercut: a) a properly etched trench opening without erosion; b) HAR trenches with a slightly negative sidewall angle.

Fig.4 shows the etching result with the modified recipe (*Recipe B* in Table I). HAR trenches with negative sidewall angle and no undercut are etched successfully. The same structure is shown in Fig.5 after oxidation. During the about 13 hours during oxidation, an array of bulk trench structure is transferred into thick oxide layer. The scalloping structures can be observed clearly, which follows the DRIE sidewall topography before oxidation, indicating a successful etching without undercut. The trench structures are completely oxidized and nicely closed. The thickness of the oxide layer is about 50 µm, which creates a reasonable isolation to the substrate.

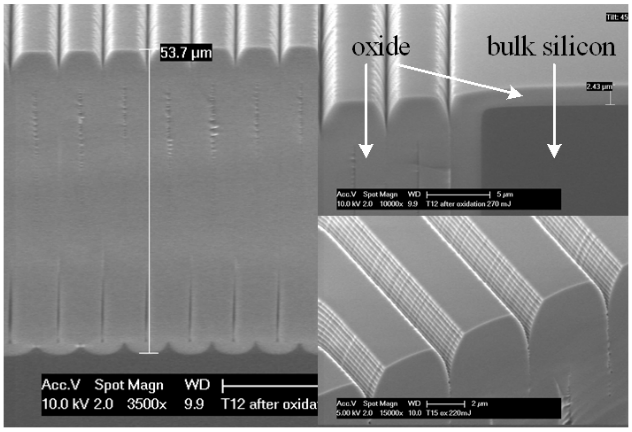

Figure 5. SEM image of the selective thick layer oxidation into the bulk silicon

B. Channels and Electrodes Etching

In order to create a through wafer channel with vertical electrodes, the DRIE process needs to be performed on both sides of the wafer. PECVD oxide is used as the mask material. First, a fluidic chamber is etched on the backside of the wafer, about 480 µm deep into the silicon, until the deep bulk oxide structure can be observed on the bottom of the back chamber. Then, a thin layer of Al (100 nm) is sputtered on the backside, forming a stop layer for the front side channel etching. Finally, the channels and electrodes are defined simultaneously by the DRIE on the front side, and the thin Al stop layer is removed later by wet etching.

For this step, the backside chamber etching is not a critical step. Only the uniformity issue should be taken into account. The nozzle etching on the front side of the wafer, on the other hand, needs more consideration.

1) The nozzle etching should have a straight (or again a slight negative) sidewall angle. The reason is shown in Fig.6 a&b. A positive sidewall angle could possibly result in a thin layer of silicon residual attached on the vertical oxide isolation surface, which may lead to a short circuit between the separated electrodes. Such positive sidewall angle is typically obtained when etching silicon in deep holes with small diameter. In these structures the plasma is blocked by the mask and sidewall in two dimensions, causing insufficient ion bombardment on the bottom of the holes. To compensate for this, the plasma density is increased by moving the wafer closer to the plasma source.

2) A slight undercut is helpful to ensure a completed etching of the silicon close to the nozzle opening. Due to the process variation, a thin piece of silicon residual could be hidden under the mask (Fig.6 c&d). To avoid this, a small undercut produced by starting the DRIE sequence with an SF_6 etching step is proved to be helpful.

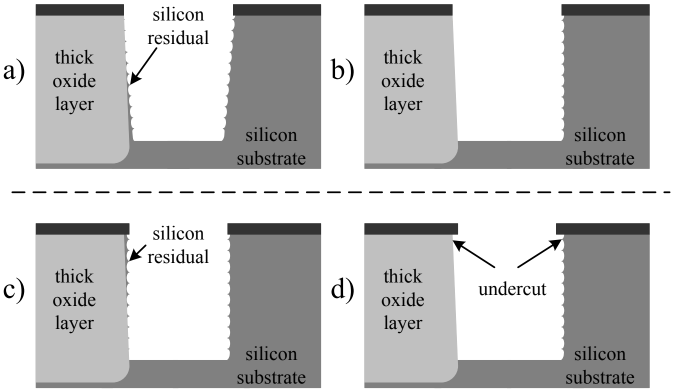

Figure 6. A schematic drawing showing two possible silicon residuals (a)&(c) created by the improper DRIE etched profiles.

The SEM image in Fig. 7 shows a comparison between of an unsuccessfully (a) and successfully (b) etched nozzle structure. The above mentioned residual issue can be clearly observed (Fig.7 a), and by using *Recipe C* in Table I, the problem is solved (Fig.7 b).

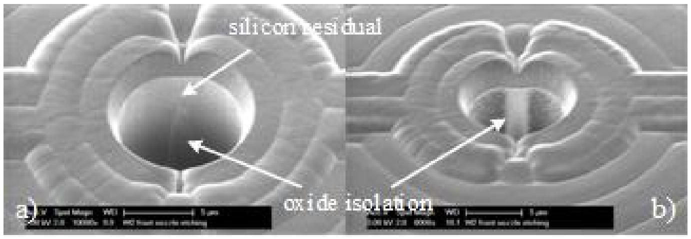

Figure7. SEM images of the nozzle etched with different recipes: a) nozzle with silicon residual close to the orifice; b) successfully etched nozzle with the modified recipe.

III. RESULT

Figures 8 and 9 show the SEM photos of a fabricated microfluidic dispenser nozzle, with a capacitive sensor fabricated, using the above discussed etching recipes.

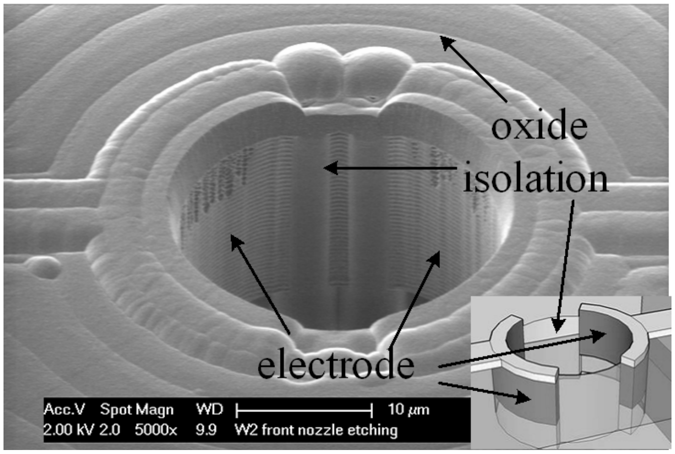

Figure 8. Fabricated vertical electrodes and oxide isolation on the nozzle sidewall (front side view)

The diameter of the nozzle is 25 µm, aiming at detection of 10~50 pico-liter droplets. The isolating thick oxide layer is 50µm deep. Two vertical electrodes are located inside the nozzle, separated by the deep oxide structures. Each electrode is 25 µm high, 30 µm wide and 2.5 µm thick. When the liquid meniscus moves inside the nozzle, by measuring the capacitance change between the two vertical electrodes, the position and velocity of the liquid meniscus can be estimated. Such information can be used as a feedback signal in high precision microfluidic dispenser systems.

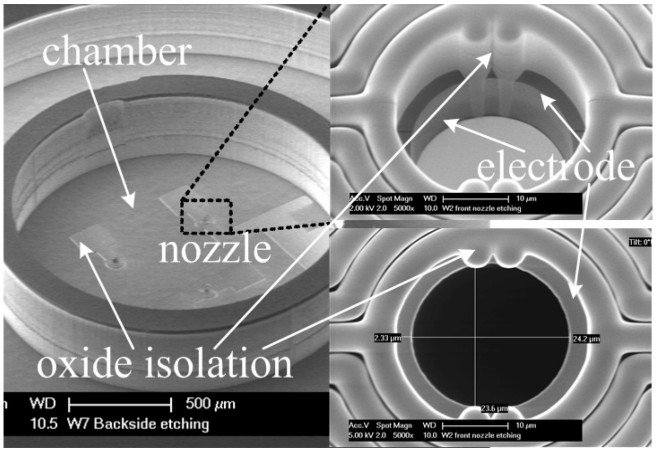

Figure 9. The liquid chamber and micro nozzle with electrodes (backside view)

IV. CONCLUSIONS

The DRIE steps used in a capacitive sensor integration process for inkjet nozzle have been discussed individually. By tuning the process parameters during the DRIE etching, correct recipes have been obtained from a starting recipe to meet the different requirements in those steps respectively. An inkjet nozzle with a capacitive sensor has fabricated successfully with the recipes developed in this paper.

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REFERENCES

[1] J. Wei, M. van der Velden, P.M. Sarro, “Fabrication of vertical electrodes on channel sidewall for picoliter liquid measurement”, Transducer 2007, Lyon, France, Jun, 2007.

[2] Michiel Alexander Blauw, “Deep anisotropic dry etching of silicon microstructures by high-density plasmas”, Delft PHD thesis, 2000.

[3] http://www.adixen.com/all/dyn/products/products.php?id_prod=52&lg=avt&vu=&vu2=

[4] Brosnihan T J, Bustillo J M, Pisano A P and Howe R T, “Embedded interconnect and electrical isolation for high-aspect-ratio”, Transducers 97, Chicago, USA, pp 637–640, 1997