Device and Stress Simulation of MOSFETs with Crystalline High-k Gate-Dielectrics Manufactured with Replacement Gate Process

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***Abstract*—Damascene gate technology has allowed to manufacture MOSFETs with crystalline high-k gate dielectrics and metal gate electrodes without damaging the gate stack by high temperatures or plasma etching steps. Mechanical stresses introduced by nitride layers of dummy gate required in that specific process are investigated using device simulation and measurements. The impact on charge carrier mobility and density of interface states is estimated. It is shown that mechanical stresses are one of the relevant degradation factors of device performance.**

***Index Terms*—Crystalline high-k gate dielectric, damascene metal gate, interface state density, stress simulation.**

I. Introduction

By now high-k materials have been considered as gate dielectrics in the standard CMOS process to further continue with the superior transistor performance all the while reducing the equivalent oxide thickness (EOT). However, the thickness of the gate dielectric is the main limiting factor at present. Scaling down for sub 32nm technologies will require an EOT well below 1nm.

In order to replace SiO_2, mainly amorphous and poly-crystalline high-k materials, such as HfO_2 and ZrO_2, have been investigated as alternative gate dielectrics. However, a major drawback of these materials is the need of a SiO_2 buffer layer between the silicon surface and the high-k dielectric, which increases the equivalent oxide thickness and eliminates the chance to achieve an EOT well below 1nm. Therefore epitaxially-grown crystalline dielectrics with a lattice constant near to silicon have been proposed as alternatives. Praseodymium oxide (Pr_2O_3) was the first epitaxially-grown rare-earth material which has been investigated as gate dielectric [1], [2]. Fully functional MOSFETs have been realized using conventional poly-silicon gate electrodes for the first time by our group [3], [4]. Electrical properties and discussion of device properties can be found in refs. [5-9]. Very recently, devices manufactured using a replacement gate process have been successfully fabricated with crystalline gadolinium oxide (Gd_2O_3) as dielectric and metal gate electrodes [10], [11]. Metal gate electrodes do not suffer from gate depletion, like poly-silicon electrodes, thus remote coulomb scattering (RCS) is eliminated and carrier mobility is expected to improve. However, metal gates seem to introduce other undesirable effects, which negate the elimination of RCS. In [12] compressive strain in the channel induced by the metal gate and surface roughness are proposed to describe this behavior. Simulation data obtained from process and device simulations were fitted to electrically measured device characteristics in [13] showing how transistor parameters are dependent on interface state density and surface roughness.

The impact of mechanical stress on device performance is shown in this work using the Sentaurus process and device simulation package by Synopsys. Mechanical stress is introduced by the use of the replacement gate manufacturing process. This process necessitates the deposition of a dummy gate stack consisting of silicon nitride layers serving as polish stop for the chemical mechanical polishing (CMP) step. The plasma enhanced chemical vapor deposition (PECVD) process used to manufacture the silicon nitride layers is described in detail in [14].

II. Device Fabrication and Structure

A brief outline of the replacement gate process is given in Fig. 1. According to the EXITGATE (i.e. gate first) approach [15], dummy gate structures are formed on blank silicon wafers covered with a silicon nitride / poly-silicon / silicon nitride sandwich. Subsequent to source / drain implantation, a SiO_2 layer is deposited via PECVD and the ion implantation is activated by a brief rapid thermal annealing (RTA) step at 1000°C, which also stabilizes the top nitride layer against the following CMP step. After the CVD oxide is polished down to the top of the dummy gate, the dummy gate itself is removed completely by wet etching and all harsh process steps like reactive ion etching (RIE) and high-temperature anneals are done. Now, the final gate stack with either high-k oxide or SiO_2 reference dielectric is manufactured. Molecular beam epitaxy (MBE) is used for growing epitaxially a thin Gd_2O_3 layer and subsequent in-situ metal deposition (tungsten) is performed.

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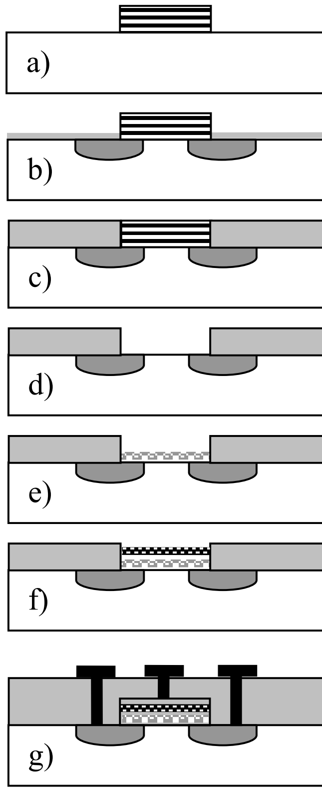

Fig. 1. Outline of the CMP-based metal gate damascene fabrication process: a) dummy gate stack formation, b) source-drain formation, c) alignment oxide formation, d) dummy gate stack removal, e) gate dielectric growth, f) metal gate formation, g) back-end processing.

All devices manufactured are of n-type and feature a gate length of 4µm. The reference devices exhibit conventional SiO_2 gate dielectrics (k ≈ 3.9) with a physical thickness of t_{ox} = 50Å. Gate electrodes were implemented with tungsten-titanium. Devices with Gd_2O_3 gate dielectrics (k ≈ 10.1) were manufactured with EOTs of 21Å and 53Å and tungsten gate electrodes.

III. Stress Simulation

A. Process simulation

Devices were generated with the process simulator Sentaurus process [17]. Beginning with a blank p-doped silicon first all steps of the replacement gate process were computed for all devices on examination. After source / drain implantation and dummy gate removal the devices were provided with a SiO_2 or a Gd_2O_3 layer respectively.

The first batch of process simulations were performed without consideration of thermal mismatch of silicon and silicon nitride.

After the application of stress models and material parameters, a second simulation cycle was conducted. Thermal expansion coefficients α_{ref} and thermal expansion coefficient rates α_{rate} were set for silicon, silicon nitride and silicon oxide respectively. The total thermal expansion coefficient is then described by

$$\alpha = \alpha_{ref} + \alpha_{rate} \cdot \left(T - T_{ref}\right) \qquad (1)$$

Parameters were extracted with Sentaurus process simulator from experimental results described in [14] and [16].

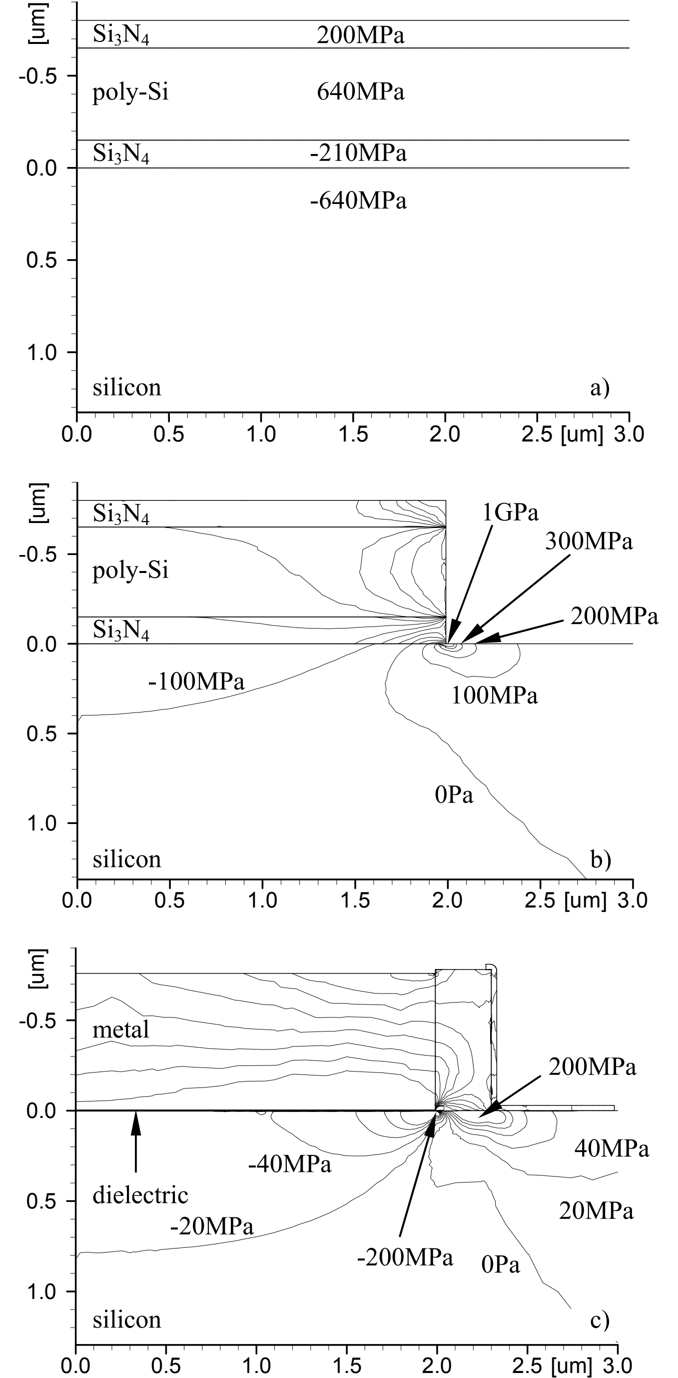

Fig. 2. Computed mechanical stress in channel direction during replacement gate process: a) maximum stresses after deposition of nitride layers, b) after dummy gate formation and, c) after dummy gate removal and deposition of proper gate stack. Negative values indicate compressive stresses, positive values indicate tensile stresses. All stresses are given in Pascal [Pa].

Fig. 2 shows process-simulated contours of mechanical stress in channel direction during the replacement gate manufacturing process of n-MOSFET devices. As one can see, a compressive stress of about -100MPa exists in the subsequent channel region at room temperature. At material edges much higher stresses of up to 1GPa can be observed. After dummy gate removal and formation of the proper gate stack compressive stresses drop down to -20MPa in the mid of channel and -200MPa at the source/drain edges.

B. Device simulation

Device simulation of the process simulated structures was performed with Sentaurus device simulator [18] and prepared with Inspect [19]. First the structure was simulated without any stresses by turning of the models of mechanical stress. It acts as reference with almost ideal sub-threshold and output behavior as can be seen in Fig. 3 for devices with 5nm silicon oxide gate dielectric and Fig. 4 for devices with high-k dielectric. After implementation of the stress models, the impact of the compressive stress of about 20 to 50 MPa shows only a very small shift in the sub-threshold behavior. Output characteristic is also affected only in minor degree.

After manual alteration of the device simulation stress parameters, structures with 150MPa, 500MPa and 1GPa compressive stress in the channel region were simulated. Also a device with tensile stress in the channel region of 150MPa was simulated. Fig. 5 presents the output characteristics for V_G-V_T = 1.5V and stresses from 150MPa tensile to 1GPa compressive.

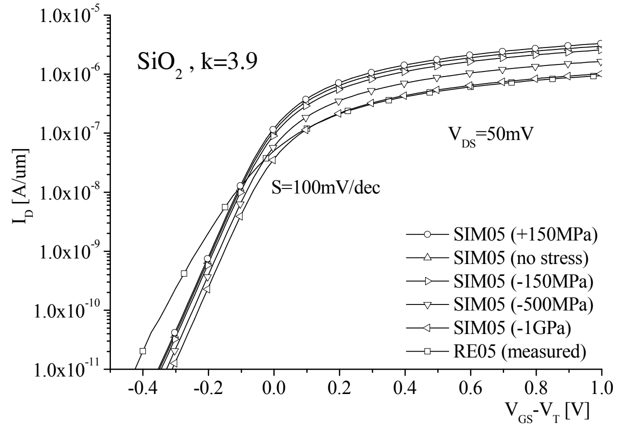

Fig. 3. Comparison of sub-threshold characteristics gained by electrical measurement and device simulation: Devices with 5nm SiO_2.

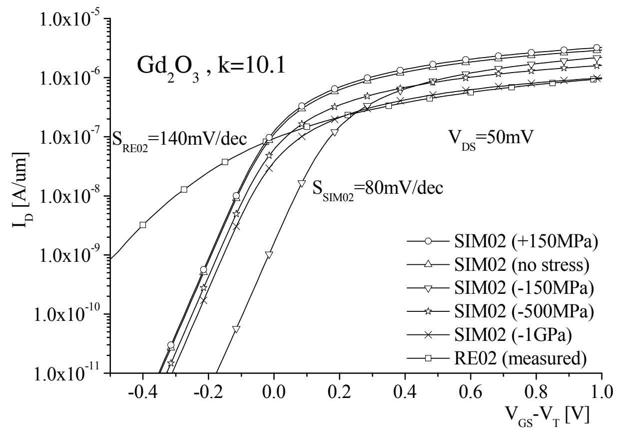

Fig. 4. Comparison of sub-threshold characteristics gained by electrical measurement and device simulation: Devices with 13.5nm high-k dielectric (EOT = 5nm).

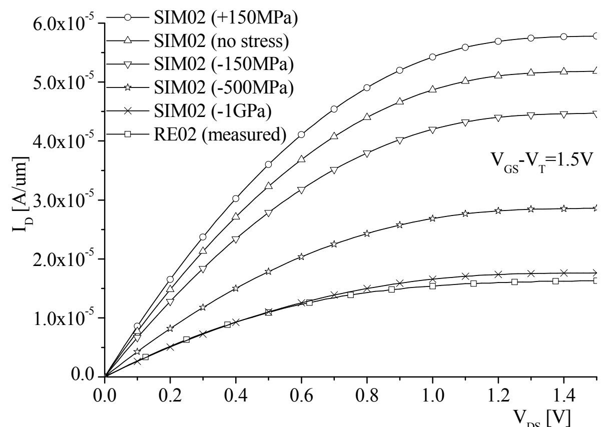

Fig. 5 Comparison of output characteristics gained by electrical measurement and device simulation: Devices with 13.5nm high-k dielectric (EOT = 5nm).

IV. RESULTS

Best transistor performance is observed, when 150MPa tensile stress is applied to the channel region. This conforms with theory where tensile stresses lead to better electron mobility. The consequences of increasing compressive stress appear in decreased electron mobility as can be clearly seen in Fig. 3 and Fig. 4. The simulated characteristics of the structure with 1GPa compressive stress in the channel region coincide very well with the characteristics of the electrically-measured structure. Indeed mechanical stress in the channel region is not considered to be greater than 40MPa, as was proven by process simulation depicted in Fig. 2. This sustains the fact that mechanical stress can not be one of the basic factors which directly influence device performance.

However mechanical stress does influence the generation of point defects in silicon during the manufacturing process. Fig. 2a shows a maximum compressive stress of 640MPa in the channel region, Fig. 2b even demonstrates a stress of up to 1GPa at edges. This stresses may lead to an accumulation of point defects which decrease charge carrier mobility in the channel. [20] and [21] describe correlation between stress and device failures as a result of defects at similar stress ranges.

V. Conclusion

Stress simulations show that compressive mechanical stress in the channel region is indeed one degrading factor for the transistors performance. But from the results it can be also seen, that this not one of the main impacts which influences channel mobility. Increased defect and interface state densities due to mechanical stress during the manufacturing process contribute to lower charge carrier mobility. On the other hand the stresses introduced by the nitride layers could be also used to improve transistor performance.

References

[1] H. J. Osten, J. P. Liu, P. Gaworzewski, E. Bugiel, P. Zaumseil, *High-k Gate Dielectrics with Ultra-low Leakage Current Based on Praseodymium Oxide*. Tech. Dig., pp. 653-656, IEDM 2000.

[2] U. Schwalke (Invited Paper), *Gate dielectrics: process integration issues and electrical properties*. Journal of Telecommunications and Technology, Vol.1, p. 7, 2005.

[3] U. Schwalke, K. Boye, K. Haberle, R. Heller, G. Hess, G. Müller, T. Ruland, G. Tzschöckel, J. Osten, A. Fissel, H.-J. Müssig, *Process Integration of Crystalline Pr2O3 High-k Gate Dielectrics*. Proceedings of the 32nd European Solid-State Device Research Conference, ESSDERC, p. 407, Sept. 2002.

[4] H. D. B. Gottlob, M. C. Lemme, T. Mollenhauer, T. Wahlbrink, J. K. Efavi, H. Kurz, Y. Stefanov, K. Haberle, R. Komaragiri, T. Ruland, F. Zaunert, U. Schwalke, *Introduction of Crystalline High-K Gate Dielectrics in a CMOS Process*. SiO2, Advanced Dielectrics & Related Devices, Chamonix Mont-Blanc, France, on June 21-23, 2004.

[5] U. Schwalke, Y. Stefanov, R. Komaragiri, T. Ruland, *Electrical Characterisation of Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs*. Proceedings of 33rd European Solid State Device Research Conference (ESSDERC), pp. 247-250, 2003.

[6] Y. Stefanov, R. Komaragiri, U. Schwalke, *Device Level and Nanoscale Electrical Characterization of Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs*. SEMATECH International Workshop on Electrical Characterization and Reliability for High-K Devices, Austin, Texas, USA, Nov. 4-5, 2004.

[7] Y. Stefanov, G. Hess, G. Tzschöckel, U. Schwalke, *Global and Local Charge Trapping Effects in Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs*. The Electrochemical Society International Semiconductor Technology Conference (ECS-ISTC) Shanghai China, September, 15 - 17, 2004.

[8] Y. Stefanov et al., *Nanoscale Electrical Characterization of Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs with Conductive Atomic Force Microscopy*. Seeing at the Nanoscale III, Santa Barbara, California, USA, August 13-16, 2005.

[9] R. Komaragiri, F. Zaunert, U. Schwalke, *Gate Engineering for High-k Dielectric and Ultra-Thin Gate Oxide CMOS Technologies*. Workshop on Semiconductor Advances for Future Electronics (SAFE 2004), Veldhoven, The Netherlands, 24th-25th of November 2004.

[10] R. Endres, Y. Stefanov and U. Schwalke, *Electrical Characterization of Crystalline Gd2O3 Gate Dielectric MOSFETs Fabricated by Damascene Metal Gate Technology*. Workshop on Dielectrics in Microelectronics (WoDiM), Catania, Italy, June 26 – 28, 2006.

[11] H. D. B. Gottlob, T. Echtermeyer, T. Mollenhauer, M. Schmidt, J. Efavi, T. Wahlbrink, M. C. Lemme, H. Kurz, R. Endres, Y. Stefanov, U. Schwalke, M. Czernohorsky, E. Bugiel, A. Fissel, H. J. Osten, *Approaches to CMOS integration of epitaxial gadolinium oxide high-K dielectrics*. European Solid State Device Research Conference (ESSDERC), Montreux, Switzerland, Sept. 18 – 22, 2006.

[12] Mikael Cassé, Laurent Thevenod, Bernard Guillaumot, Lucie Tosti, Francois Martin, Jérôme Mitard, Olivier Weber, Francois Andrieu, Thomas Ernst, Gilles Reimbold, Thierry Billon, Mireille Mouis, Fabien Boulanger, *Carrier Transport in HfO2/Metal Gate MOSFETs: Physical Insight Into Critical Parameters*, IEEE Transactions on Electron Device. Vol. 53, No. 4, 759-768, April 2006.

[13] Florian Zaunert et al., *Evaluation of MOSFETs with crystalline high-k gate-dielectrics: device simulation and experimental data*. Journal of Telecommunications and information technology, 2007, pp. 78-85.

[14] Shiliang Wu, *Characterization and applications of PECVD insulator layers concerning electrical, optical and mechanical properties*. Diploma thesis D208, Institute for semiconductor technology, 1999.

[15] U. Schwalke, M. Kerber, K. Koller, H. Jacobs, *EXTIGATE: the ultimate process architecture for submicron CMOS technologies*, IEEE Transactions on Electron Devices 44 (11), p. 2070-2077, 1997.

[16] W. E. Beadle, J. C. C. Tsai and R. D. Plummer, *Quick reference guide manual for silicon integrated circuit technology*. John Wiley & sons, 1985.

[17] *Sentaurus Process User Guide Version Z-2007.03*, Synopsys, March 2007.

[18] *Sentaurus Device User Guide Version Z-2007.03*, Synopsys, March 2007.

[19] *Inspect Version Y-2006.06*, Synopsys, June 2006.

[20] K. V. Loiko , I. V. Peidous, T. E. Harrington and W. R. Frensley, *Stress-induced redistribution of point defects in silicon device structures*. Solid state phenomena Vols. 82-84 (2000), pp. 225-230.

[21] H. W. van Zeijl, S. Mijalcovic, L. K. Nanver, *Electrical detection and simulation of stress in silicon nitride spacer technology*. Journal of materials science: Materials in electronics 12 (2001), pp. 339-341.

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