Single-Crystalline Si CMOS TFT circuit Fabricated Inside a Location-Controlled Grain by μ-Czochralski process

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Abstract— We report the behavior of single grain CMOS TFT inverter and ring oscillator fabricated inside a location-controlled grain. The location of grain was controlled precisely by μ-Czochralski process. The single grain CMOS inverter at V_{DD} = 0.5V showed full swings between ON and OFF state. 31-stage ring oscillator oscillates with a frequency of 53.4 MHz with the supply voltage of 10 V. The propagation delay is estimated to be 0.6ns/stage, which is faster than that of poly-Si TFT counterpart. This μ-Czochralski technology provides a great step towards realization of systems-on-glass in large area electronics and also 3D integration of ICs.

Keywords— **μ-Czochralski process; Single grain, Location-control; TFT circuit;**

I. INTRODUCTION

Excimer-laser crystallization of a-Si is an attractive technique for realizing the poly-Si TFT on glass [1]. The performance of poly-Si TFTs, however, is limited by grain boundaries (GBs), which creates the potential barrier that hinders the carrier motion in poly-Si TFTs. The performance can be enhanced by controlling the location of GBs and avoiding the electrically active GBs from the channel of TFTs. In one dimension, the location of grain can be controlled by lateral solidification [2]. However best situation is that GBs are completely eliminated from channel area i.e. single grain TFTs, For realizing single grain TFTs, it is essential to control the location of grain in two dimensions. The μ-Czochralski (grain-filter) process [3] provides a precise way to control position of grain in excimer-laser crystallization. TFTs fabricated by μ-Czochralski process inside a location-controlled grain (c-Si TFTs) showed a very high performance. This high performance c-Si TFTs will allow us to integrate system circuits with flat panel display, i.e., system on glass. The n-channel c-Si TFTs fabricated inside a location-controlled grain by μ-Czochralski process showed a field-effect electron mobility μ_{FEe}, subthreshold slope S and off-current of 597 cm^2/Vs, 0.2 V/dec. and ~10^{-13}A respectively, [4] while, p-channel counterpart showed a field-effect hole mobility μ_{FEh}, S and off-current of 250 cm^2/Vs, 0.29 V/dec. and ~10^{-13}A respectively [5]. Using coplanar top gate TFT process with self-aligned geometry, we fabricated complementary metal-oxide-semiconductor (CMOS) circuits with inverters and ring oscillators inside a location-controlled grain by μ-Czochralski process. The objective of this paper is to realize CMOS inverter inside a location-controlled grain, i.e., single-grain CMOS inverter, using the c-Si TFTs fabricated inside a location-controlled grain by μ-Czochralski process.

II. EXPERIMENT

The TFTs used in this experiment were fabricated with μ-Czochralski process [3]. The schematic diagram of single grain CMOS inverter is shown in Fig. 1. The planar view of the inverter is shown in fig.2.

Thermally oxidized c-Si wafers were patterned into a grid of deep cavity with the by plasma etching. Subsequently, a silicon dioxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 ^{0}C. The diameter of the larger cavity was decreased to a final value of below 100 nm. Next, 250 nm thick a-Si was deposited by LPCVD using silane at 545 ^{0}C. The samples were crystallized with XeCl excimer-laser (λ = 308 nm, pulse duration = 56 ns) with

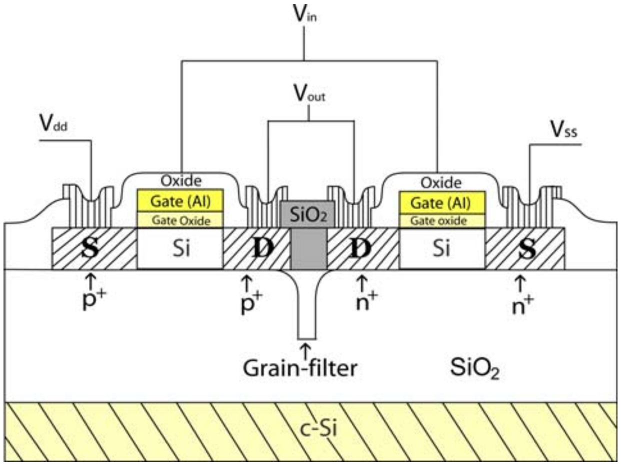


Figure 1. Schematic diagram of single grain CMOS inverter fabricated by μ-Czochralski process

various energy densities at a temperature of 450 ^{0} C.

After the formation of location-controlled grain, oxygen plasma treatment was carried out to passivate the traps states and dangling bonds in bulk silicon. Subsequently, the crystallized Si film was patterned into islands by reactive ion etching. The channel region of both TFTs is designed so that single grain covers the entire channel area of both TFTs, as shown in fig.2. Then, 89 nm ECR-PECVD SiO_2 was deposited as a gate insulator at room temperature and annealed in water vapor at 333 ^{0} C [6]. The gate electrode was then formed with sputtered Al at room temperature. The source and drain were implanted with by phosphorus and boron for n-channel c-Si TFT and p-channel TFT respectively, by covering either side of source drain with photoresist.

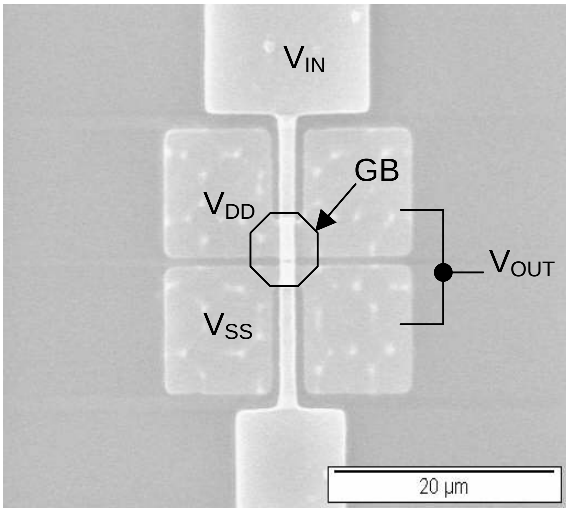


Figure 2. SEM view of single grain CMOS TFT inverter

The activation of the dopants was carried out by excimer-laser at room temperature. To minimize the resistance of gate electrode, caused by Al_2O_3, the contacts with silicon and gate electrode was defined by separate mask. No hydrogenation was carried out later. To determine the delay of one stage, chain of single grain CMOS inverter, i.e. ring oscillator of different stage was also fabricated. The channel dimensions of both TFTs were measured by SEM. The channel width for p-channel c-Si TFT was 2.754 μm and for n-channel c-Si TFT was 1.43 μm, whereas, there was constant channel length of 1.24 μm for both types of TFTs.

III. RESULTS AND DISCUSSION

Figure 3 shows the transfer characteristics of p- and n-channel TFTs of the single-grain CMOS TFT inverter fabricated by μ-Czochralski process. The field effect mobility the p- and n-channel c-Si TFTs were 500 $cm^2/V.s$ and 235 $cm^2/V.s$ respectively, While the subthreshold slope was 0.25 and 0.26 V/dec. respectively. However these characteristics are limited by the fabrication process parameters.

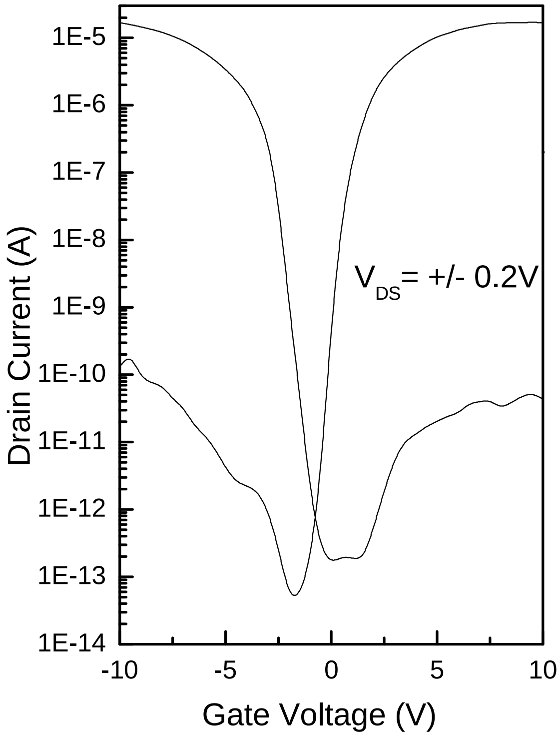


Figure 3. Transfer characteristics of the TFTs fabricated inside a single grain.

Figure 4 shows the static output characteristics of the single-grain CMOS TFT inverter fabricated inside a location-controlled grain. The supply voltage was set from 0.5V to 2V. This inverter shows a full rail-to-rail swing and full range abrupt voltage transfer characteristics. The drain current through the inverter shows negligible current outside the switching range thanks to the low leakage current of the c-Si TFTs. the threshold voltage of the inverter V_M is estimated as;

$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + r}$$

Where

$$r = \sqrt{\frac{k_p}{k_n}} \quad \text{and} \quad k = \frac{\mu\varepsilon}{t_{ox}}$$

V_{DD}, V_{Tp}, and V_{Tn} are the power supply, threshold voltage of p-channel TFT and threshold voltage of n-channel TFT respectively. The threshold voltage of inverter V_M was plotted in Fig.4. According to the threshold equation, V_M is proportional to the V_{DD}.

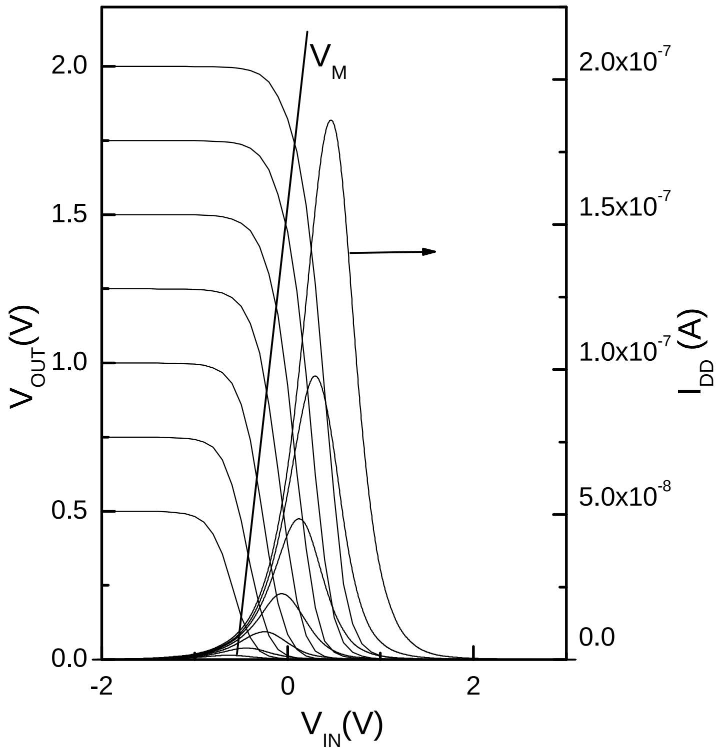
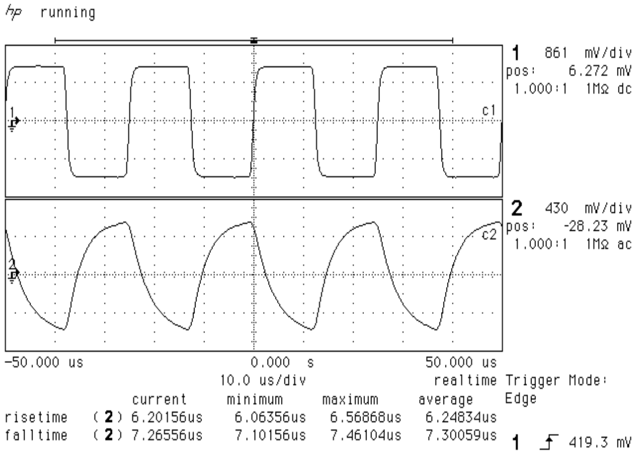


Figure 4. Static output characteristics of the single grain CMOS TFT inverter

Figure 5 shows the dynamic characteristics of the single-grain CMOS TFT inverter. The CMOS TFT inverter was operated with 40 KHz input pulses with a supply voltage V_{DD} of 10V.



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-50.000 us                  0.000  s              50.000 us
                           10.0 us/div              realtime Trigger Mode:
                  current      minimum     maximum     average    Edge
risetime    ( 2 ) 6.20156us    6.06356us   6.56868us   6.24834us
falltime    ( 2 ) 7.26556us    7.10156us   7.46104us   7.30059us  1  ⨍ 419.3 mV
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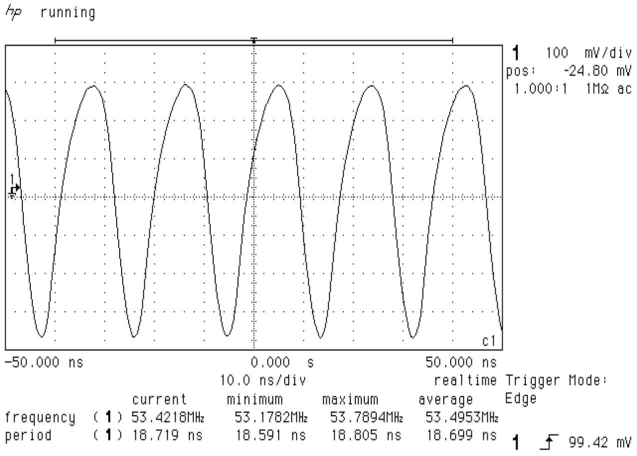
Figure 5. Dynamic characteristics of single grain CMOS TFT inverter at bottom and input pulse on top.

Whereas, the rise and fall time of output waveform of inverter was estimated to be 6.2μs and 7.3μs, respectively. We have fabricated also 31 stages ring oscillator having the chain of the single-grain CMOS TFT inverters with the same channel dimensions. As shown in Fig. 5, the ring oscillator oscillated with a frequency of 53.4 MHz with a power supply voltage V_{DD} of 10V. The propagation delay is estimated to be 0.6 ns/stage, which is faster than that of conventional poly-Si TFT counterpart [7].



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-50.000 ns                  0.000  s              50.000 ns
                           10.0 ns/div              realtime Trigger Mode:
                  current      minimum     maximum     average    Edge
frequency   ( 1 ) 53.4218MHz   53.1782MHz  53.7894MHz  53.4953MHz
period      ( 1 ) 18.719 ns    18.591 ns   18.805 ns   18.699 ns  1  ⨍ 99.42 mV
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Figure 6. 31-stage single grain CMOS TFT ring oscillator TFT 53MHz with supply voltage of 10 V.

IV. CONCLUSION

Single grain CMOS TFT inverter was fabricated for the first time inside a location-controlled grain by μ-Czochralski process with excimer-laser. Single grain CMOS TFT inverter shows a full swing between ON and OFF state at a low voltage. The propagation delay per one stage in the ring oscillator was 0.6 ns with a supply voltage of 10 V, which is faster than its conventional poly-Si circuit counterparts. In summary, single-grain CMOS inverter and ring oscillator have been realized using c-Si TFTs with a low-temperature process. This result provides a great step towards realization of systems-on-glass in large area electronics and also 3D integration of ICs.

V. ACKNOWLEDGEMENT

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