

Energy Band Offset Extraction – A Comparative Study –

J.-L.P.J. van der Steen, R.J.E. Hueting and J. Schmitz
MESA⁺ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands
email: j.l.p.j.vandersteen@utwente.nl

Abstract—Structural quantum confinement in thin silicon double-gate MOSFETs has been quantified using the temperature dependence of the subthreshold current. The results were compared with the shifts in threshold voltage. Data was obtained from simulations after initial verification with experimental data. This study demonstrates that with the temperature dependence of the subthreshold current, shifts in the valence and conduction band edge can be extracted separately from changes in mobility and density of states, making this method more accurate than the commonly used threshold voltage method.

I. INTRODUCTION

Multiple gate devices such as FinFETs and Double Gate (DG) structures are commonly recognized as promising candidates for the next generation CMOS technology [1], [2]. The main merit advocated to these novel devices is the enhanced electrostatic control through the combination of multiple gates and an ultra thin semiconductor body (UTB). As the device dimensions enter the deca-nanometer range, quantum mechanical effects can no longer be neglected. Particularly the reduction of the UTB results in separation of the energy levels within the conduction and valence band, commonly referred to as *structural* carrier confinement [3]. This type of confinement is solely determined by the device geometry, with the silicon body thickness t_{Si} as key parameter.

Besides a change in effective band gap (E_g), through the offsets of (mainly) the first subbands, also other fundamental semiconductor properties such as the effective Densities of States (DOS) and mobility (μ) start to deviate from their respective bulk values [4], [5]. The effect of quantum confinement on the electrical device characteristics is generally quantified using the shift in threshold voltage (V_{th}) as a metric [4], [6]–[8]. Hence, changes in the band alignment contribute to a shift in V_{th} since, in case of band gap widening, a higher gate bias is required to obtain the same level of inversion. However, it is likely that device properties such as the gate oxide thickness, mobility and the series resistance will be incorporated in the threshold voltage: these parameters determine the current in the strong inversion regime, thus having impact on the threshold voltage. Note that, while the *theoretical* V_{th} is well-defined, several definitions of the *experimental* V_{th} exist, e.g. V_{GS} corresponding to a fixed current level, or the linearly extrapolated intersection of I_{DS} with the V_{GS} axis, starting from the maximum transconductance. In the following, we adhere to the latter.

Recently, another approach to electrically assess the impact of structural quantum confinement was reported [9], demonstrating that the temperature dependence of the subthreshold current can be exploited to observe changes in the band alignment, mobility and DOS.

In this work, the results obtained from the temperature dependence of the subthreshold current, hereafter denoted with $I_{\text{DS}}(T)$, are compared with the conventional V_{th} method for both NMOS and PMOS devices. This study clearly points out that changes in band edge, mobility and DOS can be extracted more accurately from temperature dependent subthreshold current measurements, compared to shifts in threshold voltage. Conclusive data is obtained from simulations, after verification with existing experiments. This work has also been presented in [10].

II. VERIFICATION OF SIMULATIONS

The simulations have been performed with Synopsys Sentaurus [11]. Quantum confinement is accounted for by employing the Density Gradient model, which applies a quantum correction to the classical charge distribution and has proven to be adequate in reproducing the effect of quantum confinement on the device characteristics [12]. For the mobility, the Philips Unified Mobility model with Lombardi transversal field dependence was used [13], [14].

First, the simulations are verified with existing experimental data, obtained from [9]. The measured devices are long-channel (100) Silicon-on-Insulator (SOI) MOSFETs [15] with the backside of the wafer as back-gate contact, hereafter denoted with SOIDG. A schematic is depicted in Fig. 1(a); t_{Si} ranges from 27 down to 5 nm, the channel length is 25 μm , and the oxide and BOX thicknesses are 25 nm and 400 nm (t_{ox} and t_{BOX} resp.). Fig. 2 shows the measured and simulated subthreshold curves for the thickest SOIDG devices. Good agreement is observed both in weak and strong inversion. The curves have been fitted solely by adjusting the workfunction ϕ_{m} of the gate (i.e. N^+ poly, for which $\phi_{\text{m}} \approx \chi_{\text{s}}$, the Si electron affinity). The third set of curves shows the simulated data for a fully symmetric device, having the same t_{Si} but with t_{ox} 2 nm [e.g. see Fig. 1(b)]. When operated in DG mode, the subthreshold curves of the SOIDG and symmetric device coincide, as the subthreshold current does not depend on t_{ox} and t_{BOX} [16]. Hence, the existing subthreshold current measurement data is fully comparable with the symmetric case, implying that statements on SOIDG for which $t_{\text{BOX}} \gg t_{\text{ox}}$

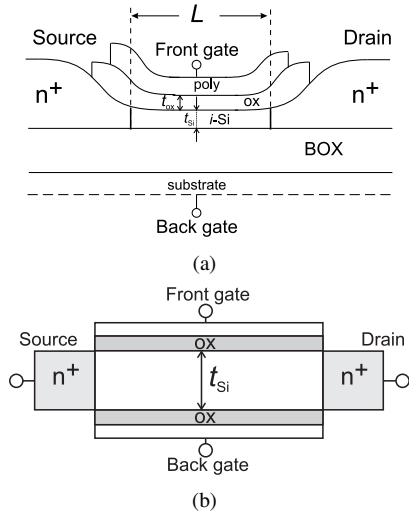


Fig. 1. (a) Asymmetric SOI DG device. (b) Symmetric device.

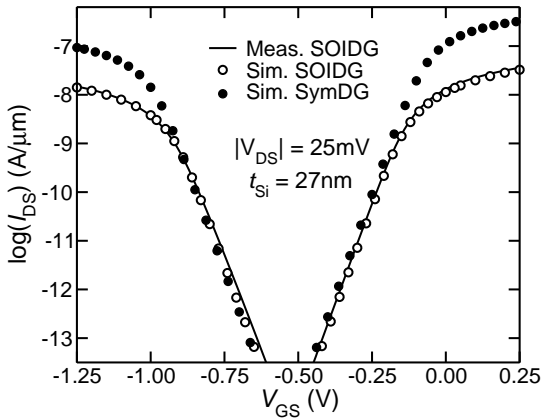


Fig. 2. Measured (solid line) and simulated data (symbols) on asymmetric and fully symmetric device (T 300 K).

in subthreshold also hold for symmetric devices [17]. Figs. 3 and 4 show the simulated subthreshold curves for SOIDG PMOS and NMOS respectively, for different temperatures, along with the measured data. The temperature ranges from 300 K to 450 K and we verified that the subthreshold slope varies linearly with temperature, indicating that no significant side effects occur. The increase in current at low gate bias and the highest temperature originates from thermal generation of carriers. Note that the previously mentioned difference in gate and channel work function can directly be extracted from the slope of $\ln(I_{DS})$ versus the inverse temperature. Good correspondence between measured and simulated data is observed, demonstrating that the simulations can be used with confidence for further investigations.

III. RESULTS AND DISCUSSION

The simulations presented in the following have been performed on symmetric devices, with t_{ox} 2 nm and t_{Si} in the range 3–27 nm, unless stated otherwise; $|V_{DS}| = 25$ mV. The strength of structural confinement in thin silicon layers

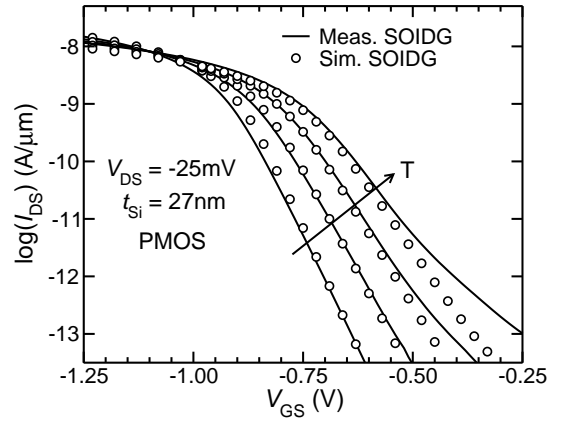


Fig. 3. Simulated and measured subthreshold curves for T 250–450K.

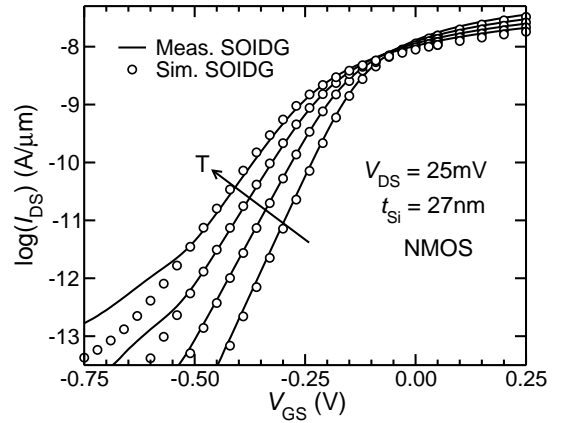


Fig. 4. Simulated and measured subthreshold curves for T 250–450K.

is governed by t_{Si} . As pointed out in [9], this dependence can be exploited to extract the shift in energy band alignment, mobility and DOS, using the temperature dependence of the subthreshold current. In short, we observe, for a given V_{DS} and V_{GS} , the ratio of the subthreshold current (η_{rat}) in two UTB devices with different t_{Si} , as given by

$$\eta_{rat} = \frac{I_{ref}}{I_{thin}} \propto \frac{\mu_{ref} \cdot g(t_{Si,ref})}{\mu_{thin} \cdot g(t_{Si,thin})} \cdot \exp\left(\frac{\Delta E_x}{kT}\right) \quad (1)$$

in which the subscripts ‘ref’ and ‘thin’ refer to the quantities corresponding to the device with the thick and thin silicon layer respectively; $g(t_{Si})$ is the DOS which, in case of quantum confinement, depends on t_{Si} . The difference in energy band edge of the thinnest layer and the reference device (ΔE_x) is equal to $E_{x,thin} - E_{x,ref}$, with subscript ‘x’ denoting the valence or conduction band edge. Note that Eq. (1) is valid for any combination of t_{Si} ’s, provided that the volume inversion condition holds [18]. In the following, the reference device has $t_{Si} = 27$ nm, i.e. sufficiently thick for quantum confinement to be negligible. Thus, the extracted band edge shift in the thinnest layer is referenced to the bulk silicon band edge.

Fig. 5 plots the experimental and simulated η_{rat} for a set of PMOS SOIDG devices with t_{Si} of 19, 9 and 5 nm. The simulations confirm the experimentally observed trend in

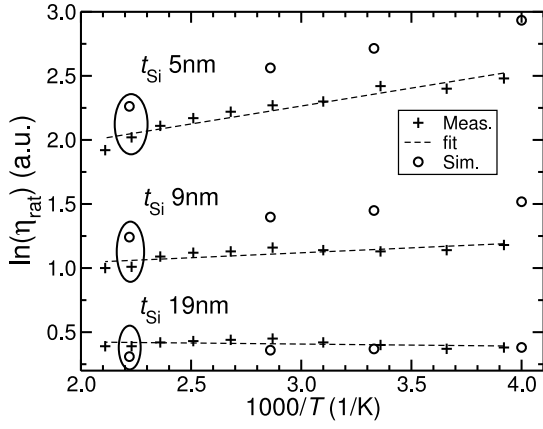


Fig. 5. Simulated (open symbols) and measured current ratio for PMOS; the dashed lines are trendlines through the measured data obtained from [9].

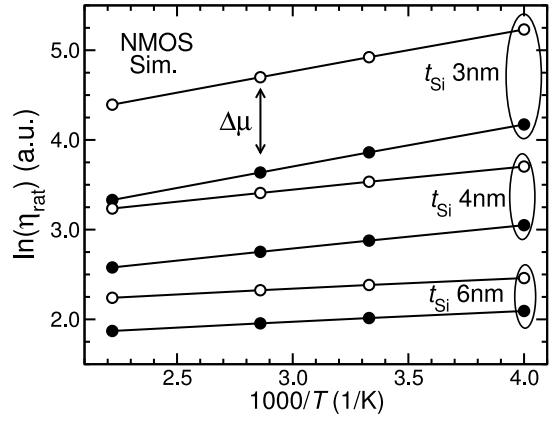


Fig. 7. Simulated current ratio for fixed mobility (filled symbols) and for decreasing mobility with decreasing t_{Si} (open symbols).

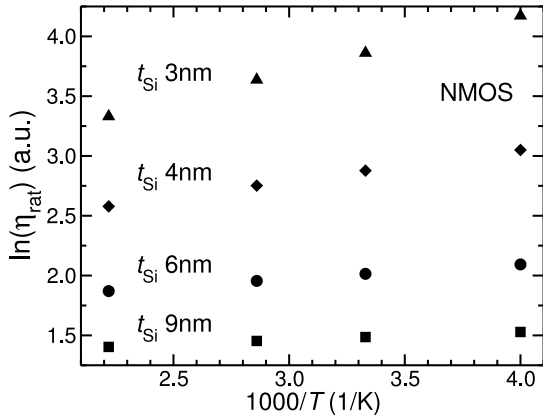


Fig. 6. Simulated current ratio for several values of t_{Si} .

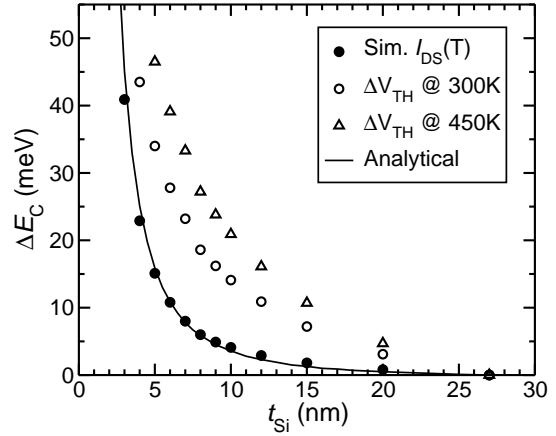


Fig. 8. Extracted conduction band offset.

that the slope of η_{rat} increases with decreasing t_{Si} , which corresponds to a positive shift in valence band edge (i.e. a wider band gap). The procedure is repeated for NMOS devices, shown in Fig. 6. Again, the slope increases for decreasing t_{Si} , as does the offset in η_{rat} . The latter generally represents a change in (combination of) mobility and DOS. However, in this case, the observed change in offset is solely due to a reduction in the DOS, since in these simulations only bulk mobility models are employed which exhibit no direct t_{Si} dependence. Further we stress that, in the subthreshold regime, the electric field normal to the gates is low. Hence, closer inspection confirms that the mobility is essentially constant throughout the entire channel, irrespective of t_{Si} .

At this regard, it is illustrative to investigate the impact of a change in mobility on η_{rat} : Hereto, the mobility was manually reduced by 15% (t_{Si} 9 nm) to 65% (t_{Si} 3 nm) relative to the mobility in the reference device. The resulting η_{rat} is shown in Fig. 7, demonstrating that the offset in η_{rat} is modified in direct proportion to the mobility reduction, whereas the slope remains unchanged.

The band offsets extracted from the slope of η_{rat} are depicted in Figs. 8 and 9 for NMOS and PMOS resp., along with the extracted shift in threshold voltage (ΔV_{th}) for different

temperatures and the SOIDG PMOS $I_{DS}(T)$ data from [9]. All values are referenced to the thickest device (t_{Si} 27 nm) which, by definition, exhibits no band shift (bulk band gap). For reference, the lowest energy in each band is shown as well, calculated with the (100) quantization effective masses [19], [20].

The figures clearly show that, although ΔV_{th} shows the same trend i.e. increasing V_{th} for decreasing t_{Si} , the extracted values are significantly higher than their respective $I_{DS}(T)$ counterparts. This can be explained by noting that quantum confinement alters both the band gap and the density of states: splitting of the bulk conduction and valence band into subbands, gives 1) a wider band gap through the offset of (mainly) the first subband, and 2) a reduction of the available states due to the additional gaps separating the subbands. In the $I_{DS}(T)$ method, shifts in the band edges are extracted from the *slope* of the current ratio, whereas changes in the DOS and mobility can be derived from the *offset* in the current ratio; hence, $I_{DS}(T)$ measurements allow for an investigation of band edge shifts separately from the mobility and DOS. In contrast, ΔV_{th} consists of a combined change in band gap, mobility and DOS, thus amplifying the apparent impact of

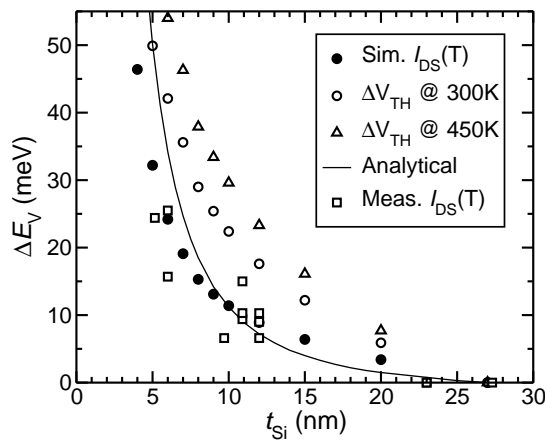


Fig. 9. Extracted valence band offset.

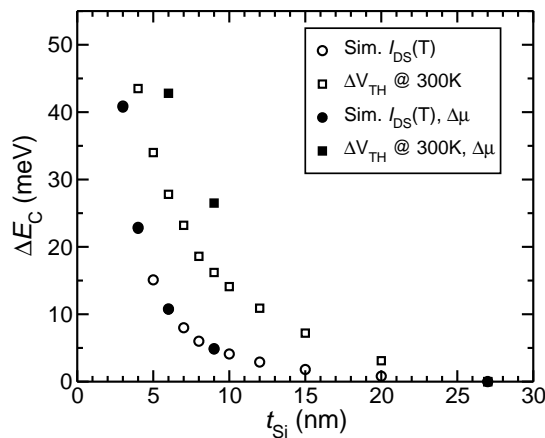


Fig. 10. Extracted conduction band offset (see also Fig. 8) for fixed mobility (open symbols) and modified mobility.

quantum confinement. Further, it is interesting to note that the threshold voltage exhibits a strong temperature dependence. While the latter is exploited in the $I_{DS}(T)$ measurements, it shows up as an additional source of error when determining the band edge shifts based on ΔV_{th} .

The values obtained with the $I_{DS}(T)$ method closely reproduce the analytically calculated lowest energy in each band, particularly for the NMOS. The slight discrepancy for the valence band offset is attributed to the approximation involved in the Density Gradient model.

The effect of a change in mobility on the extracted ΔE_C and ΔV_{th} can be observed in Fig. 10, which shows the conduction band offset and the threshold voltage shift with and without modified mobility. The figure clearly illustrates that the values obtained with the $I_{DS}(T)$ method remain unchanged, while the extracted ΔV_{th} is sensitive to a change in mobility.

IV. CONCLUSION

In this work, shifts in valence and conduction band edge have been extracted using temperature dependent subthreshold current measurements. The results have been compared with shifts in threshold voltage, showing that with the $I_{DS}(T)$

method shifts in the band edges can be observed separately from changes in mobility and DOS, which cannot be accomplished with the ΔV_{th} method.

ACKNOWLEDGMENT

The authors would like to thank NXP Semiconductors, Eindhoven, The Netherlands, for financially supporting this work.

REFERENCES

- [1] D. Hisamoto, W. Lee, J. Kedzicki, E. Anderson, H. Takeuchi, K. Asano, T. King, J. Bokor, and C. Hu, "A Folded-channel MOSFET for Deep-sub-tenth Micron Era," *Proc. IEDM*, pp. 1032–1034, 1998.
- [2] B. Yu, "FinFET Scaling to 10 nm Gate Length," *Proc. IEDM*, 2002.
- [3] L. Ge and J. Fossum, "Analytical Modeling of Quantization and Volume Inversion in Thin Si-Film DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 2, pp. 287–294, February 2002.
- [4] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental Study on Carrier Transport Mechanism in Ultrathin-body SOI n- and p-MOSFETs with SOI Thickness less than 5 nm," *Proc. IEDM*, 2002.
- [5] K. Uchida, J. Koga, and S. Takagi, "Experimental Study on Carrier Transport Mechanisms in Double- and Single-Gate Ultrathin-Body MOSFETs," *Proc. IEDM*, 2003.
- [6] Y. Omura, K. Kurihara, Y. Takahashi, T. Ishiyama, Y. Nakajima, and K. Izumi, "50-nm Channel nMOSFET/SIMOX with an Ultrathin 2- or 6-nm Thick Silicon Layer and Their Significant Features of Operations," *IEEE Electron Device Lett.*, vol. 18, no. 5, pp. 190–193, May 1997.
- [7] H. Majima, H. Ishikuro, and T. Hiramoto, "Experimental Evidence for Quantum Mechanical Narrow Channel Effect in Ultra-Narrow MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 8, pp. 396–398, August 2000.
- [8] G. Tsutsui, M. Saitoh, T. Nagumo, and T. Hiramoto, "Impact of SOI thickness Fluctuation on Threshold Voltage Variation in Ultra-Thin Body SOI MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 4, no. 3, pp. 369–373, May 2005.
- [9] J.-L.P.J. van der Steen, R.J.E. Hueting, G.D.J. Smit, T. Hoang, J. Holleman, and J. Schmitz, "Valence Band Offset Measurements on Thin Silicon-On-Insulator MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 9, September 2007.
- [10] J.-L.P.J. van der Steen, R.J.E. Hueting, and J. Schmitz, "Extracting Energy Band Offsets on Thin Silicon-On-Insulator MOSFETs," *Proc. ESSDERC*, pp. 242–245, 2008.
- [11] Synopsys, "Sentaurus TCAD, v. Z-2007.03."
- [12] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum Device-Simulation with the Density-Gradient Model on Unstructured Grids," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 279–284, February 2001.
- [13] D.B.M. Klaassen, "A Unified Mobility Model for Device Simulation – I. Model Equations and Concentration Dependence," *Solid-State Electronics*, vol. 35, no. 7, pp. 953–959, July 1992.
- [14] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzì, "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices," *IEEE Trans. Computer-Aided Design*, vol. 7, no. 11, pp. 1164–1171, November 1988.
- [15] T. Hoang, P. LeMinh, J. Holleman, and J. Schmitz, "Strong efficiency improvement of SOI-LEDs through carrier confinement," *IEEE Electron Device Lett.*, May 2007.
- [16] Y. Taur, "An Analytical Solution to a Double-Gate MOSFET with Undoped Body," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 245–247, May 2000.
- [17] V. Trivedi and J. Fossum, "Quantum-Mechanical Effects on the Threshold Voltage of Undoped Double-Gate MOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 579–582, August 2005.
- [18] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-Gate Silicon-on-Insulator Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance," *IEEE Electron Device Lett.*, vol. 8, no. 9, pp. 410–412, September 1987.
- [19] F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev. B*, vol. 5, no. 12, pp. 4891–4899, June 1972.
- [20] C. Moglestue, "Self-consistent calculation of electron and hole inversion layers at silicon-silicon dioxide interfaces," *J. Appl. Phys.*, vol. 59, pp. 3175–3183, May 1986.