A Gilbert cell mixer with a digitally controlled performance space

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Abstract— **In today's world, new wireless communication standards evolve fast, putting a significant burden on set makers and RF IC design houses to have integrated and cheap solutions quickly on the market place. Hence there is a strong need for flexible circuit topologies that can support a range of applications via adjustability and configurability. However, this concept makes only sense if the reuse count (how many times the circuit is used while having a minimum amount of design effort) of the flexible circuits justifies the investment. This in turn, is strongly related to the performance space (the set of specifications that can be covered with one circuit, which is a sub-set of the total design space) that can be covered by the adjustable circuit. In order to assess this performance space, the Gilbert cell is considered as an example. The Gilbert cell is the most common switching mixer topology, and it is used as a basis for a digitally controlled Gilbert cell. Hence, design equations of the Gilbert cell are determined and a full design procedure is developed. DC limitations and design parameter limitations of the Gilbert cell are considered. The design space of the Gilbert cell for CMOS 0.25um technology, is determined. Following assessment of its limitations and its design space, a digitally controlled Gilbert cell is derived starting from the basic Gilbert cell. Some general solutions how the digitally controlled Gilbert might be used as a sheared component in multi-standard terminals, are mentioned. Advantages and drawbacks of these solutions in comparison with the fixed solutions are discussed.**

Keywords— **Mixer, Gilbert cell, digitally controlled performance space, adjustability, configurability.**

I. NTRODUCTION

In today's world economy, the ability to process and exchange information on the move is becoming less of a luxury and more vital for its existence. Mobility while accessing the Internet and increased flexibility are motivating the development of new wireless technologies. Each wireless technology is supported by many standards. For example, the Second Generation (2G) technology is adequate for voice communication in cellular telephony and its data communication is limited. Among the others Global System for Mobile communication (GSM) standard and Code Division Multiple Access (CDMA) are 2G technology.

Further, Third Generation (3G) technology is introduced as a successor to 2G. It allows data rates several times higher than 2G technology. Wideband Code Division Multiple Access (WCDMA)is representative from this technology. Due to the delay of 3G cellular networks, "3G-like", [1], services are offered. In particular General Packet Radio Service (GPRS) and Enhanced Data rates for Global Evolution (EDGE) provide wireless data services at speeds higher than 2G technology's standards but has limited potential in comparison with 3G technology's standards. They are also called "2.5G" technology.

In addition to the cellular technologies the Wireless Local Area Networks (WLAN) market and services are growing, as well. The goal of this wireless technology is to be cheap and to provide high data rates on short distances or so-called "hot-spots". WLAN systems can be deployed on various places such as hotels and coffee shops. WLAN technology is supported by various IEEE (Institute of Electrical and Electronics Engineers) standards (IEEE 802.11a/b/g). Bluetooth is a standard that provides connectivity on very short range and it is used for wireless headsets, wireless mouses and keyboards. Zigbee is a new standard for very cheap radios on a short distances with very low bit rate. It is used for home and building automation, industrial monitoring and control.

In the future the appearance of Four Generation (4G), [2], technology can be expected. This system should integrate WLAN, Bluetooth, cellular networks, radio and TV broadcasting and satellite communications. It should provide full mobility and connectivity for users; and free roaming from standard to standard or from service to service. The coexistence of all wireless technologies into one system requires multi-mode, multi-band and multi-standard mobile terminals. In recent publications multi-standard front-ends use duplicate circuit blocks, or even entire radio front-ends foe each standard. Although this approach is simple to implement it is not optimal in cost of chip area, especially when the number of standards is increasing. Hence, the demands for multi-standard mobile handsets have motivated the development of analog front-ends with adaptive building blocks.

Therefore, this paper investigates DC limitations, design parameter limitations, design space of the Gilbert cell, and presents an example of the Gilbert cell mixer with a digitally controlled performance space as a solution of an adjustable topology.

The organization of the paper is as follows. The subject of Section 2 is the optimization procedure for the Gilbert cell, design parameter limitations and circuit performance. Section 3 focuses on a general solution of the Gilbert cell with a digitally controlled space. In Section 4 a concrete example of the Gilbert cell with digitally controlled space is presented. The design space is investigated by parametric simulation sweeps on this topology . Section 5 is reserved for the conclusion.

II. THE GILBERT CELL

The Gilbert cell (double balanced switching mixer), see fig. 1, is the most common mixer. In this section a care is taken to determine DC limitations and design parameter limitations of the Gilbert cell. An optimisation procedure of the Gilbert cell was introduced in [3]. The first step in the design procedure is to adjust the biasing voltages (V_{rfdc}, V_{lodc}), the *W/L* ratio of the transistors and the load resistor value (*R*) such that all transistors are in saturation. Assume the DC bias current (I_{bias}) is constant. Thus, the voltage V_1 is determined by V_{rfdc} and the *W/L* ratio of the transistors M_1 and M_2. A sufficient high V_1 value can be achieved by a larger *W/L* ratio or by a larger V_{rfdc} voltage. As *W/L* the overdrive voltage (V_{gs}-V_t) of the transistors M_1 and M_2 is decreasing and as *W* is increasing, parasitics are also increased. This will lower the mixer operation at high frequencies and the mixer linearity. However, the transconductance of the transistors M_1 and M_2 (g_m) will be higher, which increases the conversion gain and reduces the noise. On the other hand, V_{rfdc} also influences the V_1 value. Thus, as V_{rfdc} increases, V_1 reaches higher values. Further, for a given I_{bias}, V_2 can approach a higher value by increasing the *W/L* ratio of the transistors M_3, M_4, M_5 and M_6. This increases parasitics at higher frequencies and lowers mixer performance. Also V_{lodc} has impact on V_2, by means that V_2 increases with higher V_{lodc}. If the I_{bias} is constant the V_3 level depends on V_{dd} and *R*. In the case all design parameters and biasing voltages are constant, V_1, V_2 and V_3 will reach higher values by decreasing I_{bias}. However, g_m is reduced and Noise Figure (*NF)* is increased.

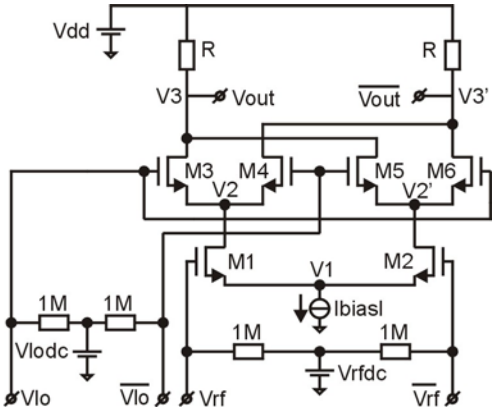


Figure 1: The Gilbert cell

Once all transistors are adjusted in saturation region, the optimisation of the mixer specification such as conversion gain, *NF* and linearity have to be done. Assuming a perfect square wave for local oscillator (LO) voltage, the voltage gain can be approximated as:

$$Gain \approx g_m R\left(\frac{2}{\pi}\right)\frac{1}{2\pi f C_{gs} R_s} \tag{1}$$

R_s is the impedance of the signal source, and C_{gs} is gate-source capacitance of the transistors M_1 and M_2. *NF* of the Gilbert cell, neglecting the flicker (*1/f*) noise, can be approximated by:

$$NF = 10\log\left(1+\frac{\pi^2}{4}*\frac{\gamma}{g_m R_s}+\frac{\pi^2}{2g_m^2 R R_s}\right) \tag{2}$$

γ is equal to 2/3 for long channel transistors and bigger than 2/3 for submicron MOSFETs [4]. A more detailed noise analysis can be found in [5].

The total intermodulation in the Gilbert cell is approximately equal to the sum of the intermodulation values that the transconductance and the switching stage would generate if the other stage were ideal. More detail analysis can be found in [6]. IIP_3 can be approximated as:

$$IIP_3 \approx 4\sqrt{\frac{2}{3}\left(V_{gs}-V_t\right)} \tag{3}$$

(V_{gs}-V_t) is the overdrive voltage and V_t is the threshold voltage of the transistors M_1 and M_2.

Based on the previous expressions and simulation results, the most important conclusions about design parameter limitations and circuit performance can be drawn. For a given I_{bias} the minimal size of transistors M_1 and M_2 is limited by DC voltages that push transistors in the triode region. The maximal size of the transistors is limited by DC voltages that push transistors in moderate inversion. Higher I_{bias} improves g_m, that improves the voltage gain and *IIP3*, reduces *NF*, but increases power consumption. Increasing the *W/L* ratio of the transistors M_1 and M_2 improves g_m, but this increase chip area, reduce overdrive voltage and reduce *IIP3*, and increased *W* introduce more parasitics,. Load resistor (*R*) is determined in such a way that all transistor are in saturation. Higher *R* improves the voltage gain. For a given bias condition there is a value of *R* for which the voltage gain is maximal. Lower *R* improves the input-referred linearity, and for a given biasing condition there is a value of *R* after which *IIP3* does not improve any more.

III. A GILBERT CELL WITH A DIGITALLY CONTROLLED PERFORMANCE SPACE

A Gilbert cell with a digitally controlled performance space (see fig 2) is based on the Gilbert cell that is introduced in previous section. The switching stage is the same stage as in the Gilbert cell. It is a cross-coupled differential pair that consists of the transistors M_3, M_4, M_5 and M_6. The load resistors and the transconductance stage in the digitally controlled Gilbert cell are programmable. To facilitate the digital control the nMOS transistors M_{sw1}, M_{sw2}, … M_{swN} and $M_{\overline{sw1}}$, $M_{\overline{sw2}}$, …, $M_{\overline{swN}}$; and pMOS transistors M_{R1}, M_{R2}, … M_{RN} and $M_{\overline{R1}}$, $M_{\overline{R2}}$, …, $M_{\overline{RN}}$ operate as switches biased in the triode region. The transistors M_{11}, M_{12}, …, M_{1N} and M_{21}, M_{22}, … M_{2N} build the *N* differential pairs of the transconductance stage. So, the transconductance stage consists of *N* differential pairs that could be switch *ON* and *OFF*. With a different combination of the switches different transistor sizes can be achieved. Each combination of the differential pairs can be biased by one of different current sources I_{bias1}, I_{bias2}, … I_{biasN}. Hence, there are 2^N combinations of (*differential pair*$_i$, $I_{bias,l}$), where i=1,   ,N, l=1,   ,N. For each group of (*differential pair*$_m$, $I_{bias.n}$), m=1,   ,N; there is a pair of load resistors R_{G1} and R_{L1}, R_{G2} and R_{L2}, …, R_{GN} and R_{LN}. R_{Gi} is a load resistance that gives the maximum conversion gain for a certain group (*differential pair*$_m$, $I_{bias,n}$), m=1,   ,N; and R_{Li} is load resistance that gives the maximum linearity for the same group (*differential pair*$_m$, $I_{bias,n}$), m=1,   ,N. The biasing voltages (V_{rfdc}, V_{lodc}) differ for a different combination of (*differential pair*$_m$, $I_{bias,n}$, R_{Gn} and R_{Ln}), where m, n =1, …, N. In such a way different set of specification can be achieved.

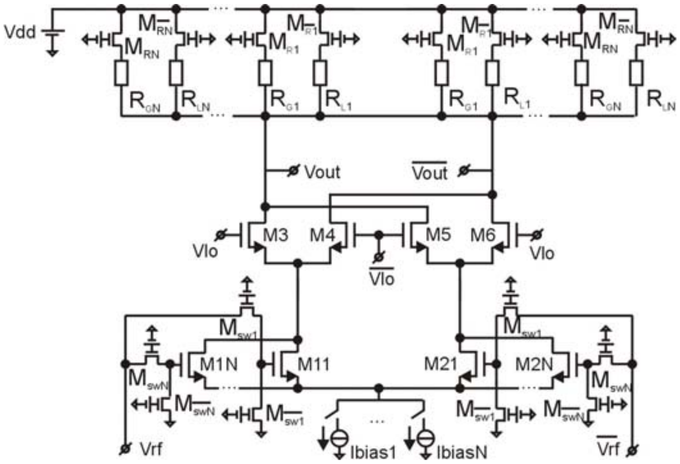


Figure 2: The Gilbert cell with digitally controlled performance space

The optimization procedure of the digitally controlled Gilbert cell is similar as for the Gilbert cell. For a desired *NF* a certain combination of (*differential pair*$_i$, $I_{bias,l}$), i=1, ..., N, l=1, ..., N, is chosen. Further, for each combination of (*differential pair*$_i$, $I_{bias,l}$) the biasing voltages (V_{rfdc}, V_{lodc}) and the load resistor value (*R*) are adjusted in such a way that a maximum voltage gain is achieved. In this way the value of $R_{G,l}$ is determined. Then, the value of $R_{L,l}$ for which the maximum *IIP3* is achieved, is determined.

Theoretically the number *N* can be unlimited. In practice it is limited and it is a tradeoff between the degradation of mixer performance and a desirable resolution of the adjustability. In order to estimate the performance degradation the impact of the MOSFET switches on the mixer performance has to be considered.

The circuit model of the single ended Gilbert cell with a digitally controlled space is shown in fig.3. Assuming a perfect square wave for local oscillator (*LO*) voltage, the voltage gain of this topology can be calculated as:

$$G = \left(\frac{2}{\pi}\right)\frac{Z_y}{Z_y + R_s} * \left(\sum_{i=1}^{N} \frac{Z_{\overline{sw,i}} // Z_{in,M1i}}{Z_{\overline{sw,i}} // Z_{in,M1i} + Z_{sw,i}} * g_{m,i} * i\right) * \left(\frac{(R_{G,i} + Z_{R,i})(R_{L,i} + Z_{\overline{R,i}})}{(R_{G,i} + Z_{R,i}) + (R_{L,i} + Z_{\overline{R,i}})}\right) // \left(\frac{(R_{G,i+1} + Z_{R,i+1})(R_{L,i+1} + Z_{\overline{R,i+1}})}{(R_{G,i+1} + Z_{R,i+1}) + (R_{L,i+1} + Z_{\overline{R,i+1}})}\right)_{i=1}^{N-1} \tag{4}$$

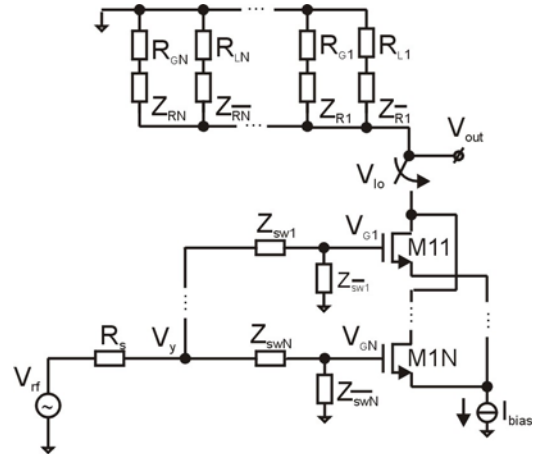


Figure 3: The single ended Gilbert cell with a digitally controlled design space

where

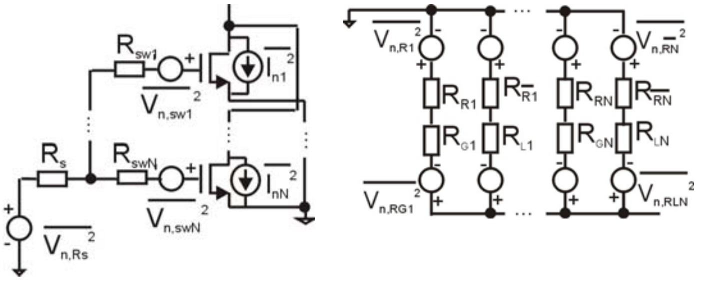
$$Z_y = \left(Z_{sw,i} + Z_{\overline{sw,i}} \,//\, Z_{in,M1i} \right) // \\ // \left(Z_{sw,i+1} + Z_{\overline{sw,i+1}} \,//\, Z_{in,M1i+1} \right)_{i=1}^{N-1}$$

i is 0 and 1 when $M_{sw,i}$ and *OFF* or *ON*, respectively. $g_{m,i}$ is the transconductance and $Z_{in,M1i}$ is input impedance of $M_{1,i}$, $Z_{sw,i}$ and $Z_{\overline{sw,i}}$ are the impedances of $M_{sw,i}$ and $M_{\overline{sw,i}}$, respectively, $Z_{R,i}$ and $Z_{\overline{R,i}}$ are the impedances of $M_{R,i}$ and $M_{\overline{R,i}}$.

The noise model of the load resistors and transconductance stage of the single ended Gilbert cell with digitally controlled space when all switches are *ON* is shown in fig.4. The *NF* of this topology, neglecting the flicker (*1/f*) noise, can be approximated by:

$$NF = 10\log(1 + \frac{\pi^2}{4} * \frac{4KT\gamma}{4KTR_s * \sum_{i=1}^{N} g_{m,i} * i} + \\ + \frac{4KT * (R_{sw,i} \overset{L}{\underset{i=1}{//}} R_{sw,i+1})}{4KTR_s} + \sum_{l=1}^{N} \frac{2 * 4KT\left(R_{G,i} + R_{R,i}\right)}{G^2 * 4KTR_s} * l \\ + \sum_{l=1}^{N} \frac{2 * 4KT\left(R_{L,i} + R_{\overline{R,i}}\right)}{G^2 * 4KTR_s} * \bar{l} \qquad (5)$$

$R_{sw,i}$ is the resistance of the transistor $M_{sw,i}$ when it is *ON*, $R_{R,i}$ and $R_{\overline{R,i}}$ are the resistance of the transistors $M_{R,i}$ and $M_{\overline{R,i}}$, respectively, when they are *ON*, i is 0 and 1 when $M_{sw,i}$ is *OFF* and *ON*, respectively. l is 0 when $M_{R,i}$ is *OFF* and $M_{\overline{R,i}}$ is *ON*, $\bar{l}$ is 0 when $M_{\overline{R,i}}$ is *OFF* and $M_{R,i}$ is *ON*. L is the number of switches that are *ON*. When all switches are *ON* L is equal to N.



(a) (b)

Figure 4: Noise model: (a) a programmable transconductance stage, (b) a programmable stage with load resistors

The total intermodulation in the digitally controlled Gilbert cell can be approximated in the same way as the total intermodulation in the Gilbert cell. IIP_3 can be approximated as:

$$IIP_3 \approx 4\sqrt{\frac{2}{3}\left(V_{gs} - V_t\right)} \qquad (6)$$

(V_{gs}-V_t) is the overdrive voltage in the transconductance stage and V_t is the threshold voltage of the transistors $M_{1,i}$.

Based on the previous expressions and simulation results, the most important conclusions about the impact of the MOSFET switches on the mixer performance can be drawn. A higher voltage gain is achieved by decreasing the value of $R_{sw,i}$ and increasing $Z_{\overline{sw,i}}$. An increased *W/L* ratio of the transistor $M_{sw,i}$ decreases $R_{sw,i}$ when the transistor in *ON*, but increased *W* introduces more parasitics and increases chip area. A lower *W* and *L* ratio of the transistor $M_{\overline{sw,i}}$ decreases $Z_{\overline{sw,i}}$ when the transistor is *OFF*, but smaller *W/L* ratio increases $R_{\overline{sw,i}}$ when the transistor is *ON*. However, the high value of $R_{\overline{sw,i}}$ does not influence the voltage gain and *NF* since it is not in the signal path. Lower value of $R_{sw,i}$ decreases *NF*. Lower values of $R_{R,i}$ and $R_{\overline{R,i}}$ reduce *NF*. By increasing *W/L* ratio of the transistors $M_{R,i}$ and $M_{\overline{R,i}}$, respectively $R_{R,i}$ and $R_{\overline{R,i}}$ decrease when the transistors are *ON*. Increased *W* increases parasitic capacitance when the transistors are *OFF*. The signal at the load resistors is low frequency signal, so, parasitic capacitance degrade negligibly the signal. The impact of switches on the linearity can be neglected.

IV. A COMPARISON BETWEEN THE GILBERT CELL AND THE GILBERT CELL WITH DIGITALLY CONTROLLED PERFORMANCE SPACE

In order to make comparison these two topologies are simulated, by using the circuit simulator SpectreRF in CMOS 0.25um technology. For this specific case the transconductance stage of digitally controlled Gilbert cell consists of 3 differential pairs where M_{11} has $W/L=50/0.25$; M_{12} and M_{13} have $W/L=100/0.25$. M_{12} and M_{13} could be switch *ON* and *OFF*. The combination of transistor sizes, I_{bias} and load resistors used in this example are presented in Table 1. The sizes of switches are: $M_{sw,i}$ has $W/L=100/0.25$, $M_{\overline{sw,i}}$ has $W/L=10/0.25$, and $M_{R,i}$ and $M_{\overline{R,i}}$ have $W/L=100/0.25$. The fixed Gilbert cell is simulated separately for each combination.

Table 1: The combinations for the digitally controlled Gilbert cell

transistor sizes	*50um*	*100um*	*250um*
$I_{bias}=1mA$	$R_{G1}=2.5K$ $R_{L1}=2K$	$R_{G1}=2.5K$ $R_{L1}=2K$	$R_{G1}=2.5K$ $R_{L1}=2K$
$I_{bias}=5mA$	$R_{G1}=550$ $R_{L1}=350$	$R_{G1}=550$ $R_{L1}=350$	$R_{G1}=550$ $R_{L1}=350$
$I_{bias}=10mA$	$R_{G1}=180$ $R_{L1}=100$	$R_{G1}=250$ $R_{L1}=100$	$R_{G1}=250$ $R_{L1}=100$

A criteria for choosing this configuration is to reach more extreme points in the design space of the Gilbert cell while introduce as less as possible parasitics. Taking the formulas (4), (5) and (6) for N=3 the voltage gain, *NF* and *IIP3* can be calculated for this specific example.

Higher value of I_{bias} improves very slightly *NF* while the power dissipation is very high. Further decrease of the transistor size brings the transistors out of the region of operation for I_{bias}=10mA. Further increase of the transistor sizes improves slightly the voltage gain and *NF* while parasitics degrades circuit performances at higher frequencies. Higher value of R_{Gi} does not improve the voltage gain any more and lower value of R_{Li} improves slightly *IIP3*.

The obtained ranges for the voltage gain, *NF* and *IIP3* of the Gilbert cell and the digitally controlled Gilbert cell are given in Table 2. Although some values within these ranges are not applicable they represent extreme points in the design space of the Gilbert cell. For any other combination of I_{bias} (1mA< I_{bias} <10mA), transistor sizes and load resistors circuit performance are within the obtained ranges.

Table 2: Simulation results at 2.5GHz

	Gain [dB]	*NF [dB]*	*IIP3 [dBm]*
Gilbert cell	*Max =16* *Min =-2*	*Max =14* *Min=7*	*Max=12* *Min =-8*
Digitally controlled Gilbert cell	*Max =15* *Min=-1.2*	*Max =16* *Min=9*	*Max =11* *Min=-7*

From the analytical analysis and the obtained simulation results the following can be concluded. The number N in the digitally controlled Gilbert cell can represent a number of different standards for witch the topology is designed. So, it is possible to share the topology when different standards are not operating simultaneously. Moreover, this solution is very flexible because there are more different combination possible of gain, *NF*, *IIP3* and power consumption, since transistor sizes, I_{bias} and load resistors can be chosen independently and in any combination. This might increase the reuse count. If the fixed Gilbert cell were used the multi-standard solution is possible either by duplicating the Gilbert cell N times, or designing the circuit for a standard that has the most stringent specifications. Although these two approaches are easy to implement they are not optimal. The first approach is not optimal in chip area. In the second approach the circuit consumes more power than necessary when operating under more relaxed condition (for standards with more relaxed specifications). In the case that some standards have very close specification, they can be grouped. Then N can represent a number of different groups, and the Gilbert cell with a digitally controlled space for each group is designed for a standard with the most stringent specifications. For example Zigbee and Bluetooth might be one group, standards from 2G cellular technology might be another group, and standards from 3G cellular technology might be third group, and so on. In such a way a huge range of standards can be covered with one adjustable topology. Moreover, incoming standards can fit in certain groups and products are ready very quickly on the market.

The price paid for programmability and adjustability is degradation of the circuit performance due to the parasitic capacitances especially when the number N is higher and the frequencies are higher.

V. CONCLUSIONS

The Gilbert cell was analyzed and evaluated, and was used as a basis for a Gilbert topology with a digitally controlled space with N stages. An analysis of the digitally controlled Gilbert cell was done. For N = 3 the following ranges for the voltage gain, *NF* and *IIP3* in CMOS 0.25um technology were obtained from 15dB to –1.2dB, from 16dB to 9dB, and from 11dBm to –7dBm, respectively, for the power dissipation in the range from 2.5mW to 25mW. It was shown that a wide range of standards could be covered with a digitally controlled Gilbert cell. A great flexibility at a relatively low (1 or 2dB) degradation of performance compared to a full custom design, was achieved. Moreover, incoming standards can easily fit in predesigned digitally controlled topologies, and hence, products are ready very quickly on the market. The price paid for programmability and adjustability is degradation of the circuit performance due to the parasitic capacitances especially when the number *N* is higher and the frequencies are higher.

REFERENCES

[1] A.K.Salkintzis, C.Fors and R.Pazhyannur, "WLAN-GPRS Integration for Next-Generation Mobile Data Networks", IEEE Wireless Communications, October 2002.

[2] U.Varshney and R.Jain, "Issues in Emerging 4G Wireless Networks", COMMUNICATIONS, 2001.

[3] V.Vidojkovic, *et.al.*, "Mixer Topology Selection for a Multi – Standard High Image – Reject Front – End", ISCAS, vol. 2, no. 2, pp. 300-303, 2003.

[4] B.Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001.

[5] H.Daragi *and* A.Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model", *IEEE Journal of Solid State Circuits*, vol. 35, no. 1, pp. 15-25, January 2000.

[6] M.T.Terrovitis and R.G.Meyer, " Intermodulation Distortion in Current – Commutating CMOS Mixers", *IEEE* Journal of Solid-State Circuits, vol. 35, no. 10, October 2000.