

# A Low Power Chopper Current-Feedback Instrumentation Amplifier with noise PSD of $17\text{nV}/\sqrt{\text{Hz}}$

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**Abstract**—This paper presents the design of a chopped fully-differential current-feedback instrumentation amplifier (CFIA). The current-feedback topology facilitates ground sensing and the use of independent input and output common-mode voltages. The amplifier is intended for the readout of a high-precision thermistor bridge. The required temperature sensing resolution is  $1\mu\text{K}$  ( $3\sigma$ ) in a  $3\text{mHz} - 50\text{mHz}$  bandwidth, which translates to an input referred noise density of  $31\text{nV}/\sqrt{\text{Hz}}$ . Since these frequencies are very low, the input stages of the amplifier are chopped to suppress their  $1/f$  noise. Moreover, to achieve optimum power efficiency at low noise, the first stage is designed to dissipate the most power (75%). Simulations show that the amplifier’s input-referred noise density is  $17\text{nV}/\sqrt{\text{Hz}}$  at a supply current of  $226\mu\text{A}$ . The amplifier has been implemented in  $0.7\mu\text{m}$  CMOS technology. Measurement results agree well with the simulation results.

**Index Terms**—Current-feedback, ground sensing, chopping, power efficiency.

## I. INTRODUCTION

In wafer-steppers, due to the extremely rigorous requirements on mechanical accuracy, temperature must be precisely controlled. Over a small ( $0.8\text{K}$ ) temperature range, a resolution of  $1\mu\text{K}$  ( $3\sigma$ ), or equivalently 20bit, is required. This resolution must be maintained at very low frequencies (long time periods) ranging from  $3\text{mHz}$  to  $50\text{mHz}$ . Such high precision sensing can be achieved by the use of negative temperature coefficient (NTC) thermistors in a dual bridge configuration<sup>[1]</sup>.

The block diagram of the thermistor read-out system is depicted in Fig. 1. It consists of a preamp, a low pass filter and a commercially available  $\Sigma\Delta$  ADC (LTC2484). The preamp amplifies the bridge output and therefore, relaxes the dynamic range required of the ADC. In order not to compromise the noise performance of the bridge, the preamp must have very low noise and low drift.

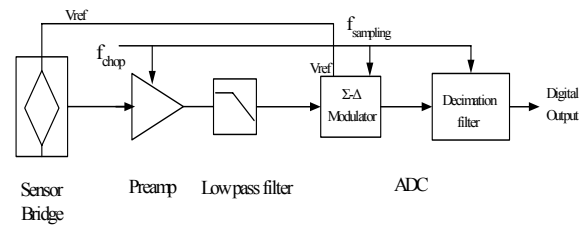


Fig. 1. Block diagram of the interface electronics for high-precision thermistor bridge

This paper describes the design of a power-efficient fully differential preamp. The gain of the preamp is chosen to be  $45\text{dB}$  in the wafer-stepper’s application due to the mapping from  $1^\circ\text{C}$  to  $5\text{V}$ . The other parts of the temperature control system in the wafer-stepper are all based on this scaling factor. The bandwidth of the preamp will be limited by the low pass filter and the ADC’s decimation filter of  $3\text{Hz}$ , which has an over-sampling ratio of 60 over the application bandwidth  $50\text{mHz}$ . The requirement for very low noise at very low frequencies makes this design quite challenging.

The first challenge involves the required resolution. The sensitivity of the bridge is such that the required temperature sensing resolution translates into an input-referred noise density of  $31\text{nV}/\sqrt{\text{Hz}}$ . The noise of the thermistor bridge is  $16\text{nV}/\sqrt{\text{Hz}}$ , and so the preamp’s noise density was chosen to be at the same level. Furthermore, the application requires that the preamp’s  $1/f$  noise corner frequency must be below  $3\text{mHz}$ , i.e. the preamp should have very low drift. This also means that the preamp must have high CMRR and PSRR.

A second challenge involves self-heating. Since the preamp is located close to the thermistor bridge, its power consumption should be only a few milliwatts to minimize self-heating errors. Moreover, to reduce the effect of self-heating in the thermistor bridge itself, its DC excitation voltage should be as low as possible. As a result, its

common-mode output voltage will be low, and so the preamp's common-mode input range should include ground.

A third challenge is the need to isolate the input and output common-mode voltages. This allows for flexibility, as the input common-mode range of the ADC is 0-5V, while, as discussed above, that of the bridge should preferably be close to ground. The resulting preamp specifications are listed in Table I.

TABLE I. Key preamp requirements

Specifications	Value
Supply Voltage	5V
Gain	45dB
Bandwidth	0-3 Hz
Gain tolerance	0.5%
Input referred noise	17 nV/ $\sqrt{\text{Hz}}$
1/f corner frequency	3 mHz
Offset	5 $\mu\text{V}$
CMRR	>130 dB
Input Common-Mode	0-3 V
Output Common-Mode	2.5 V
Supply current	<300 $\mu\text{A}$

This paper is organized as follows. In section II, the choice for the preamp's topology and the choice of a chopping strategy are described. In section III, the preamp's circuit design is presented. In section IV, simulation results are given. The paper ends with some conclusions.

## II. ARCHITECTURE OF THE PROPOSED PREAMP

### A. Choice of Preamp Topology

There are two basic approaches to the design of an instrumentation amplifier: resistive feedback or current feedback.

A traditional instrumentation amplifier using resistive feedback is shown in Fig. 2. The main disadvantage of this topology is that its common-mode input range does not extend to ground. Second, to accommodate differences in the input and output common-mode voltages, a resistor  $R_3$  is required at the common-mode node. A DC current then flows through the feedback resistors to adjust the output common-mode voltages. For a given output common-mode voltage, the required current (and excess noise) increases as the input common-mode voltage decreases. Third, the feedback resistors need to be well trimmed to obtain high CMRR. Fourth, it is not power efficient, as it requires two high gain operational amplifiers.

An instrumentation amplifier that uses current mode feedback is depicted in Fig. 3. The input voltage signal is

transferred into current by the input stage  $G_{m1}$ , while the feedback voltage signal is converted to current by the feedback stage  $G_{m2}$ . Due to feedback, the output of  $G_{m1}$  will be compensated by the output of  $G_{m2}$ . A current-feedback instrumentation amplifier (CFIA) has the advantage that both current-source isolation and null-balancing techniques are used to achieve a good CMRR. Secondly, the input and output common-mode voltages are independent. Thirdly, it is power efficient because the input stages share a common summing and output stages.

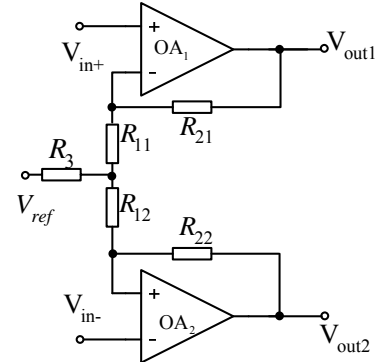


Fig. 2. Bridge instrumentation amplifier realized by two operation amplifiers

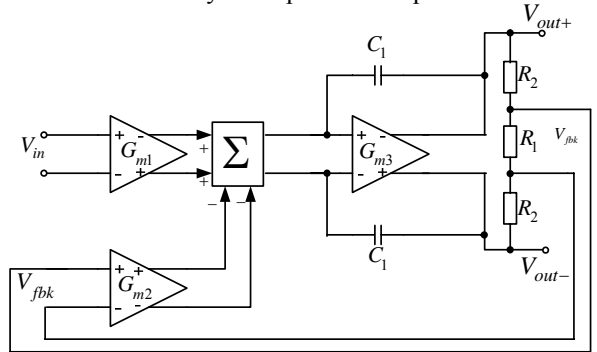


Fig. 3. Current-feedback instrumentation amplifier

To achieve good gain accuracy, the two  $G_m$  stages need to be accurately matched. The input common-mode voltage varies from 0V to 3V, which can be handled by PMOS differential pairs. So with good layout, it should be possible to achieve 0.5% gain accuracy with the CFIA topology.

### B. Chopping Strategy

The noise requirement in this application is quite demanding. To achieve an input-referred noise density of 17nV/ $\sqrt{\text{Hz}}$  down to 3mHz and low drift over time and temperature, techniques such as auto-zeroing and chopping can be adopted to suppress the 1/f noise. Due to noise aliasing, auto-zeroing will cause the noise at low frequencies to exceed the thermal noise floor of the input stage. Furthermore, auto-zeroing is not suitable for

continuous-time operation<sup>[5]</sup>. Chopping maintains the thermal noise of the input stage, but shifts its offset and  $1/f$  noise to the chopping frequency. Filtering is required to

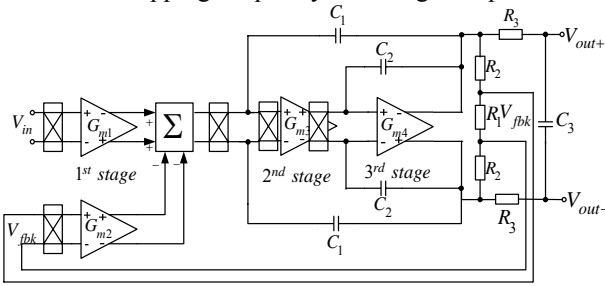


Fig. 4. Block diagram of the chopped CFIA

reduce the ripple at the chopping frequency<sup>[5][6]</sup>. For low-noise and low bandwidth applications, chopping is the best choice because of its superior noise performance.

The topology of a chopped CFIA is depicted in Fig. 4. A class-AB output stage was chosen to save power and improve output driving capability. However, the large signals present in the class-AB stage mean that it cannot be accurately chopped. Simulations show that the preceding (chopped) stages must then have a gain of at least 190dB in order to sufficiently suppress the class-AB stage's input referred  $1/f$  noise. Such a high gain can only be obtained with a two-stage amplifier.

Thus, we choose a three-stage CFIA topology, in which the first and the second stages are chopped to suppress their  $1/f$  noise. Stability is obtained by the use of Nested-Miller frequency compensation. The feedback compensation capacitors of the class-AB stage then help to filter out ripple present at the chopping frequency. The remaining ripple can then be filtered out by an off-chip RC filter.

The chopping clock with perfect 50% duty cycle is essential to suppress very low-frequency  $1/f$  noise. The rise and fall times of the clock should also be small enough to ensure that the switches's own  $1/f$  noise can be neglected.

### C. Optimum Power Efficiency

To achieve the optimum power efficiency, most of the power should be dissipated in the first stage. In this design, the first stage consumes 75% of the power. Meanwhile, the first stage provides high gain (140dB) to suppress the noise and nonlinearity from the following stages.

## III. CIRCUIT IMPLEMENTATION

The first stage amplifier is depicted in Fig. 5. For simplicity, the common-mode feedback loop is not shown. PMOS input transistors and a folded-cascode topology are chosen to achieve ground sensing.

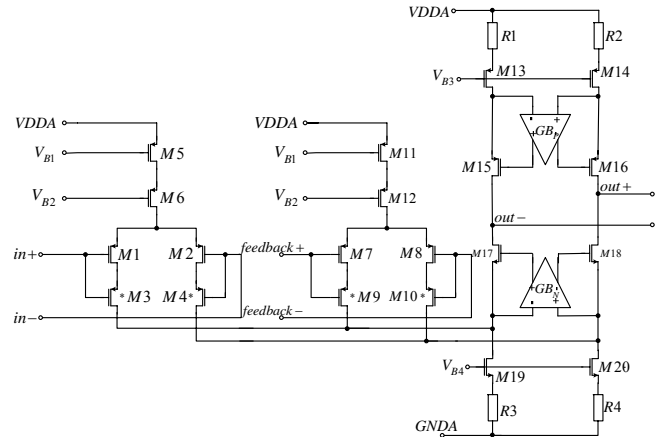


Fig. 5. The first stage amplifier

To achieve better matching of the input and feedback  $G_m$  stages, bias currents, transconductance and drain-source voltages of the input transistors should be the same. In this way, the nonlinearity of the two  $G_m$  stages can be well-compensated. However, different input and output common-mode voltages will lead to different drain-source voltages. Two cascoded low-threshold transistors M3 and M4 are utilized to regulate the drain-source voltages of the input transistors. The current sources are also cascoded to reduce channel-length modulation.

A gain-boosting structure is employed to obtain 140dB DC gain in the first stage amplifier. To reduce the noise contributed from the current source in the folded-cascode topology, degenerated current sources are utilized.

## IV. SIMULATION RESULTS

The simulation results of the input referred noise spectrum without chopping is depicted in Fig. 6. Without chopping,  $1/f$  noise below 10kHz is clearly visible.

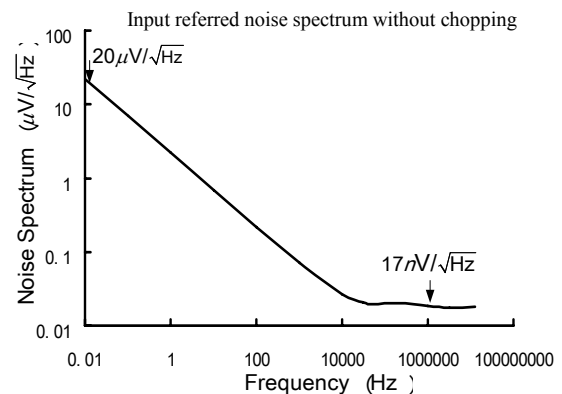


Fig. 6. Simulated input referred noise spectrum without chopping

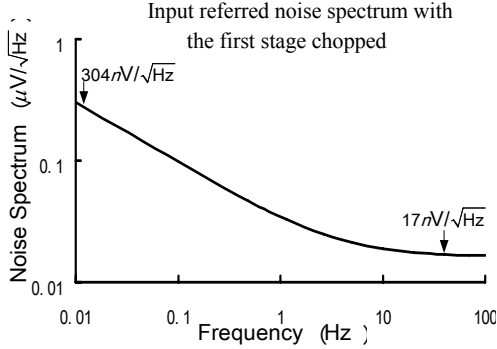


Fig. 7. Simulated input referred noise spectrum when only the first stage amplifier is chopped

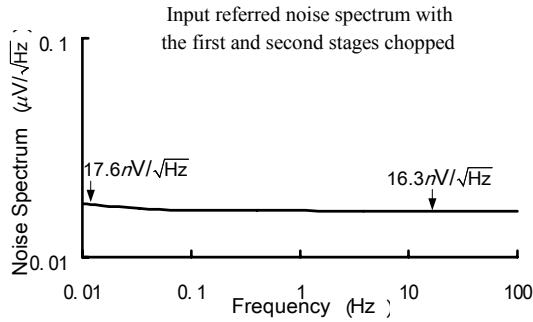


Fig. 8. Simulated input referred noise spectrum when both the first and second stages are chopped

The periodic steady-state (PSS) and periodic noise analysis (PNOISE) capabilities of Spectre RF are used to simulate the noise spectrum with chopping. Fig. 7 shows the noise spectrum when only the first stage is chopped. Fig. 8 depicts the noise spectrum when both the first and second stages are chopped. The simulation results are summarized in Table II.

TABLE II Simulation Performance of the CFIA

Supply voltage	5V
Gain	45 dB
Gain tolerance	0.5%
Input offset voltage	5µV
Input noise density	17nV/√Hz
PSRR	120dB
CMRR	130dB
Unity-Gain-Bandwidth	800kHz
Rail-to-Rail Output	0-5 V
Input Common Mode Voltage Range	0-3 V
Output Common Mode Voltage	2.5 V
Supply current	226 µA

The noise efficiency factor<sup>[3]</sup> (1) is used to benchmark the expected noise efficiency of this work, as shown in Table III.

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (1)$$

where  $V_{ni,rms}$  is the input referred rms noise voltage,  $I_{tot}$  is the total amplifier supply current,  $U_T$  is the thermal voltage  $kT/q$  and  $BW$  is the amplifier bandwidth.

TABLE III Figure of merit comparison with state-of-the-art

	Supply current	Input Noise Density	Input referred noise	NEF
Instrumentation Amplifier with two OPA333 <sup>[2]</sup>	34µA	76 nV/√Hz	0.253µVrms (0.1-10Hz)	18.4
This work	226µA	17 nV/√Hz	30nVrms (0.003-3Hz)	10.2
[7]	1.2µA	94 nV/√Hz	0.93µVrms (100Hz)	4.9

This work achieves good noise efficiency comparable with a state-of-the-art ultra low-power instrumentation amplifier.

## V. CONCLUSION

A chopped low noise current-feedback instrumentation amplifier is presented in this paper. It achieves input referred noise density of 17nV/√Hz down to 10mHz with a quiescent current of 226µA. It is capable of ground sensing and handling different input and output common-mode voltages. This instrumentation amplifier architecture can be applied successfully to interface bridge-based sensors. Measurement results agree well with simulations.

## REFERENCES

- [1] G. C. Meijer, "Thermal sensors", Institute of Physics publishing, 1994.
- [2] R. Burt, J. Zhang, "A Micropower Chopper-Stabilized Operational Amplifier using a SC Notch Filter with Synchronous Integration inside the Continuous-Time Signal Path", *IEEE J. Solid-State Circuits*, Vol. 41, pp. 2729-2736, Dec. 2006.
- [3] M. S. Steyaert, et. al., "A micropower low-noise monolithic instrumentation amplifier for medical purposes", *IEEE J. Solid-State Circuits*, Vol. 22, pp. 1163-1168, Dec. 1987.
- [4] R. Yazicioglu et. al., "A 60µW 60nV/√Hz Readout Front-End for Portable Biopotential Acquisition Systems", *IEEE J. Solid-State Circuits*, Vol. 42, pp.1100-1110, May. 2007.
- [5] A. T. K. Tang, "A 3µV offset Operation Amplifier with 20nV/√Hz Input Noise PSD at DC Employing both Chopping and Autozeroing", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 386-387, Feb.2002.
- [6] J. F. Witte, et. al., "A CMOS Chopper Offset-stabilized Opamp", *IEEE J. Solid-State Circuits*, Vol. 42, pp. 1529-1535, July. 2007.
- [7] T. Denison et. al., "A 2.2µW 94nV/√Hz Chopper-Stabilized instrumentation amplifier for EEG Detection in Chronic Implants", *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp. 162-163, 2007.