

A RF-Resonator Packaged in Vacuum Using Substrate Transfer and Thin film processes

M. Duemling, J. Mueller, R. Dekker and H. Pohlmann

Abstract— A new packaging process for single crystalline silicon MEMS devices that allows an easy integration of the resonator into a BIMOS process will be presented. The resonator is defined via trench etching into a SOI wafer and a spacer technology followed by a standard metallisation process. After processing the front side the wafer is glued to a glass substrate (substrate transfer technology). From the backside trenches are etched into the buried oxide layer through the silicon. Afterwards the MEMS device will be released in hydrofluoric acid. Finally the cavity is sealed with a PECVD layer. This paper will present first frequency measurements of the MEMS resonator and a feasibility study to integrate the resonator into a BIMOS process.

Index Terms— MEMS, packaging, substrate transfer

I. INTRODUCTION

ELECTROMECHANICAL silicon resonators are considered as a possible replacement for SAW and FBAR resonators in filter applications [1]. While in recent years the frequency and quality factor of the silicon resonators were continually improved [2], the packaging is still challenging since the devices have to be packaged in vacuum to obtain a high quality filter.

In current packaging technologies RF-resonators are either packaged in complex and expensive vacuum housing or the structure is protected on a wafer level, which is done commonly by wafer bonding. The drawback of this process is that the wafer-bonding process requires exact placement of the two wafers across the whole wafer what is difficult due to layer stress related wafer bow and warpage of the processed wafers. To obtain a strong and reliable bond, the overall wafer thickness variation has to be in the order of a few nanometers. To overcome this disadvantage separate lids can be soldered on each device [3]. This individual packaging of each die makes this process expensive. Alternatively the MEMS-structure is protected by a sacrificial layer (e.g. oxide) followed by a thick capping layer. The sacrificial layer is etched through holes in the capping layer to release the structures. An additional PECVD layer finally seals the system [4]. This process usually requires thick films and therefore high temperature processes are necessary. To overcome the

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disadvantages of the common packaging technologies, we recently introduced a novel packaging process combining thin film technologies and substrate transfer [5, 6]. In this process a polysilicon RF-MEMS Resonator (see figure 1) is manufactured between two oxide sacrificial layers and then sealed with an LPCVD nitride layer. After gluing the wafer to a glass substrate, holes are etched from the backside. The resonator is released and subsequent the cavities are sealed

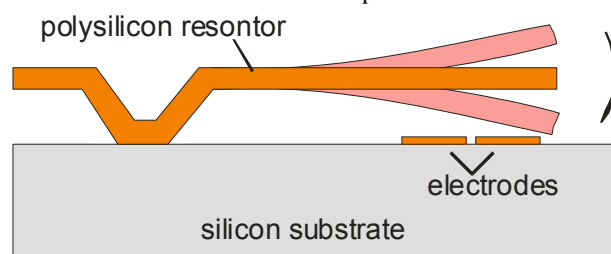


Fig 1. Schematic drawing of a polysilicon RF-resonator with vertical excitation in the caption.

with a PECVD oxide. The combination of these two processes reduces process temperatures and film thicknesses significantly. The required alignment accuracy of the two wafers of a few hundred micrometers can be achieved easily with an optical flat aligner. A drawback of this method is the restriction of the resonator material to polysilicon. The thickness of the resonator is therefore limited. Recent enhancements of this process allow the fabrication of the resonator in single crystalline silicon. Having a free choice of the resonator thickness, single crystalline silicon has also better mechanical properties, less intrinsic losses and better hysteresis properties compared to polysilicon.

The resonator is realized in single crystalline silicon using a SOI-Wafer with an active silicon layer of 10 μm . The resonator is defined via trench etching the top silicon layer. The gap between the electrode and the resonator is defined with a spacer technology, allowing distances smaller than 100nm. An advantage of the small gap is that a resonator drive voltage compatible with commercial IC processes can be used. After the deposition of a nitride layer a CMOS-compatible two layer metallization follows. Subsequently the silicon wafer is glued to a glass substrate and grinded back to approximately 30 μm . From the backside, deep trenches are etched into the silicon down to the buried oxide layer. These trenches serve as etch holes for releasing the structure in hydrofluoric acid. A final PECVD process seals the trenches. Figure 2 and 3 show cross-sections of the final device.

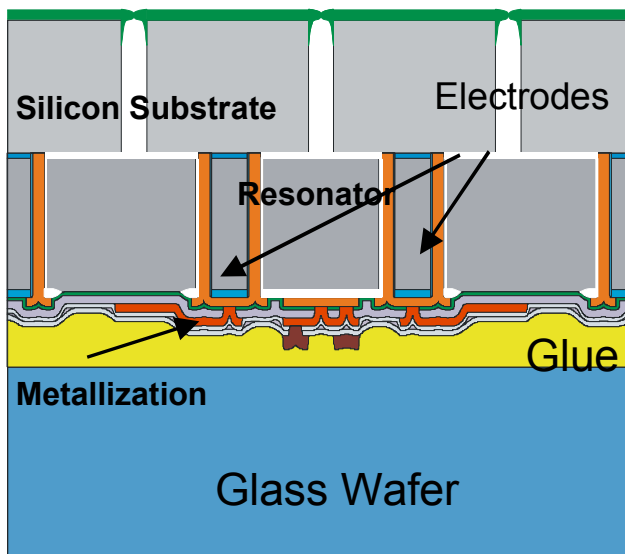


Fig. 2 Drawing of the cross section of the packaged resonator

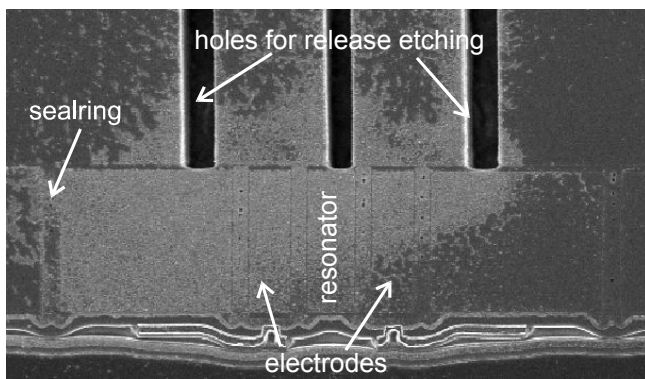


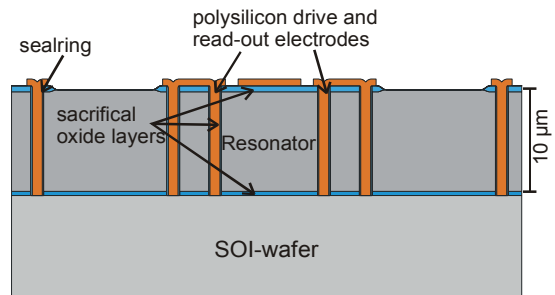
Fig.3 SEM-cross section of a beam resonator

After a detailed process description, the results of a feasibility study of the integration of these devices in a CMOS process will be given. Finally the first measurement of an unpackaged resonator will be presented.

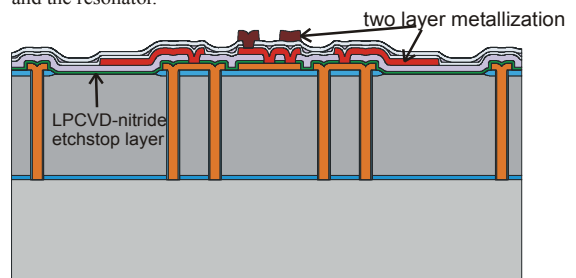
II. PROCESSING

The resonators are fabricated on a SOI-Wafer with a 400 nm thick buried oxide layer and a 205 nm thick active silicon layer. The oxide layer acts as lower sacrificial layer, the silicon layer as starting layer for the 10 μm thick, boron doped silicon epitaxy. The silicon epitaxy defines the resonator thickness and was chosen after considering technological aspects as well as process cost: From a technological point of view a thicker layer and therefore a heavier resonator is of advantage. A resonator with a larger mass is more frequency stable since it is less affected by process variations and contaminations. A thick silicon layer has also the advantages of larger electrode areas, resulting in a larger signal. On the other hand a thicker silicon layer implies longer deposition and etching times, making the process more expensive.

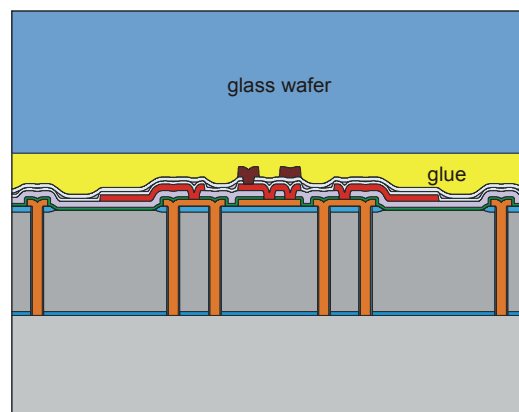
The basic process steps are shown in figure 4. After the LOCOS oxidation that also acts as upper sacrificial layer, the resonator and the electrodes are defined with an anisotropic



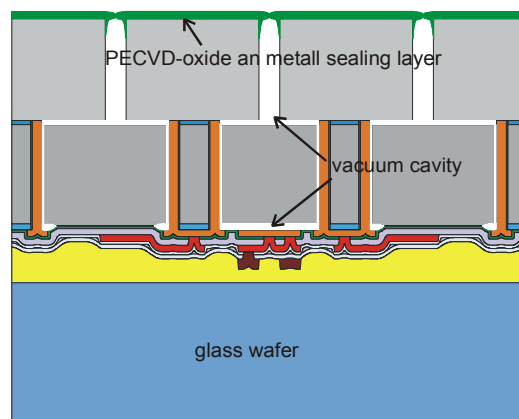
On an SOI-Wafer with an active silicon layer of 10 μm , the resonator is defined via trench etching. An TEOS-spacer process is used to obtain a narrow gap between the electrodes and the resonator.



After the deposition of an LPCVD nitride etch stop layer a two layer metallization process is used to electrical contact the resonator.



After the deposition of a passivation layer the silicon wafer is glued to a glass wafer. The silicon is then grinded back to a remaining thickness of approx. 30 μm



In the final step holes are etched from the backside into the wafer. The resonator itself is released in hydrofluoric acid via these holes. The cavity is sealed with a combination of PECVD-Oxide and metal deposits.

Fig. 4 Schematic fabrication process of an encapsulated RF-resonator

high rate silicon etch process (Bosch process) and the etching of the buried oxide layer. Two parallel trenches both 1.2 μm wide are etched for each electrode. Instead of being limited to 1 μm wide, 10 μm deep flexible polysilicon electrodes, this technique consistently obtains stable and reliable electrodes that are several micrometers wide (figure 5 and 6). A 180 nm thick LPCVD TEOS-layer defines the distance between the electrodes and the resonator. Since the TEOS deposition process has a sidewall step coverage of less than 60 %, the resulting TEOS thickness at the walls of the trenches is approximately 100 nm, defining the resonator electrode gap. A following antistrophic oxide etch process removes the TEOS from the bottom of the trench. The trench is then filled with polysilicon. To archive uniform doping of the polysilicon in the trench a 200 nm thick polysilicon layer is deposited first followed by a doping process in a furnace under phosphine

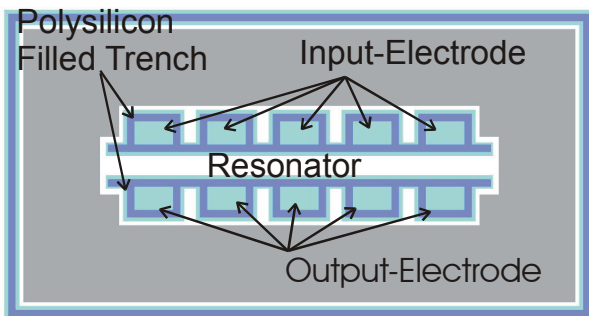


Fig. 5 CAD-drawing of a beam resonator

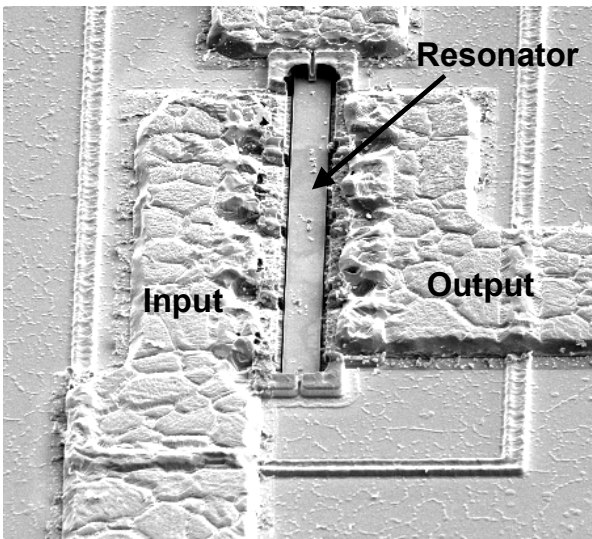


Fig. 6 SEM picture of a beam resonator.

atmosphere. A second 460 nm polysilicon deposition step with an additional doping step follows to completely fill the trench. The mechanical contact between the polysilicon and substrate at the bottom of the trench is necessary for the stability of the electrode and for the vacuum package. To obtain good access to the upper sacrificial layer (LOCOS) during the final release etch from the substrate backside the polysilicon is removed from some trenches. The etching channels are then filled with

LPCVD-TEOS. The resonator is then sealed with a 250 nm thick low stress silicon rich LPCVD-nitride layer [7]. To complete the device a two-layer metallization process with BPSG and SOG planarization is used. After a final PECVD-nitride and PECVD-TEOS passivation, the wafer is glued to a glass substrate using a solvent free UV-curable glue [8]

Followed by the transfer process the silicon wafer is grinded down to approximately 60 μm , 50 μm substrate and the 10 μm epitaxy layer remain. The crystal damage caused by the grinding process is removed with a spin etching process that thins the substrate further down to 30 μm . To get access to the resonator for releasing it, 1 μm wide etching channels are etched into the substrate from the backside. After the release in concentrated hydrofluoric acid, the device is dried in a critical point dryer to prevent stiction between the electrode and the resonator. The risk of stiction during operation can be significantly reduced by the deposition of an antistiction layer (i.e. DDMS monolayer) [9]. A combination of PECVD and

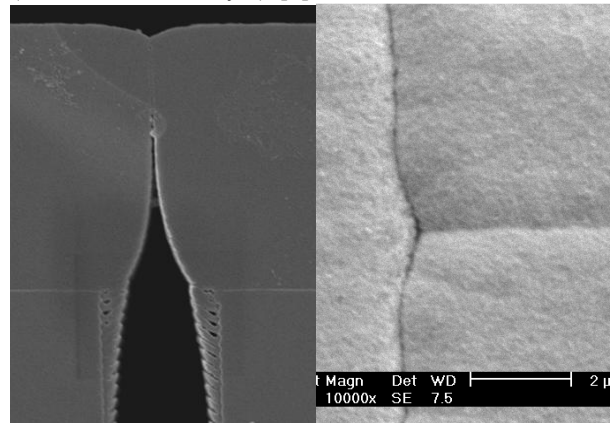


Fig. 7 Sealed backside trench

metal deposition seals the resonator. The pressure in the resonator cavity is defined by the pressure during the deposition process (figure 7). The final step is to open the bondpad from the backside through the silicon substrate

III. CMOS-INTEGRATION

The fabrication process of the RF-resonators was developed to be integrated into an existing CMOS or BIMOS process easily. Thus drive and read out electronics can be placed along with the resonator on one chip. The integration reduces parasitic inductance and capacitance, the device is therefore more sensitive to low signal levels.

The resonator will be integrated in a BIMOS process. The process has an NPN bipolar transistor with cut-off-frequency of 3 GHz and a maximum operation voltage of 20 V as well as a high voltage transistor (EPMOS) that operates up to 40 V. Therefore it is possible to build an oscillator or filter at a frequency up to several 100 MHz. Furthermore the process has a 2.5 μm CMOS technology implemented, allowing to include a simple logic circuit.

Since the process temperature of the fabrication steps for manufacturing the resonator does not exceed 950 °C, the additional thermal budget can be neglected compared to the 4 hours 1150°C emitter-drive-in.

To investigate the effects of the resonator integration to the electrical device performance, transistors on a SOI-Wafer as well as a standard wafer with and without the additional temperature steps were compared.

The SOI substrate and the additional temperature budget did not have any significant influence on the bipolar NPN-transistor. The CMOS transistors on the SOI-wafers show a decreased DC-current gain by 7.0% and a smaller saturation current by 9.6%. The DC current gain of the EPMOS high voltage transistors is reduced by 4.0 % and the saturation current is 6.4% smaller.

All the derivations were well within the process limits of the process. It is therefore possible to integrate the resonator in the BIMOS process and use the standard design library for modeling the electrical circuitry.

IV. RESULTS

A 50 μm long and 3.5 μm wide resonator was designed to proof the concept of the process flow. For the test structure the standard two layer metallization was replaced by a one-layer 5 μm thick aluminum layer. The resonator was released in concentrated hydrofluoric acid before packaging. The measurements were performed in a custom build vacuum chamber equipped with Picoprobe microwave probes. A HP 8753C network analyzer with additional external DC-power supply was used to record the frequency response of the resonator. For the measurement a DC external potential of 100 V and a AC signal of 20 dBm was applied to the resonator. The resonator had a resonance frequency of 11.35 MHz and a Q-factor up to 300 in vacuum (figure 8). The relatively low Q-factor is due the unfavorable ratio between the length and the width of the resonator resulting in high losses at the anchors, since kinetic energy is radiated as thermoelastic losses into the substrate [10]. Nevertheless this design was chosen since good analytical models are available, simplifying the process characterization and the investigation of the temperature dependent drift of the resonance frequency.

V. CONCLUSIONS

A process has been presented that allows the vacuum packaging of single crystalline resonators. It has been shown that the SOI wafer and the additional temperature budget needed for the resonator fabrication has only minor influence on the performance of the electrical parameter of the devices of a BIMOS process. Also the frequency response of a unpacked resonator has been presented.

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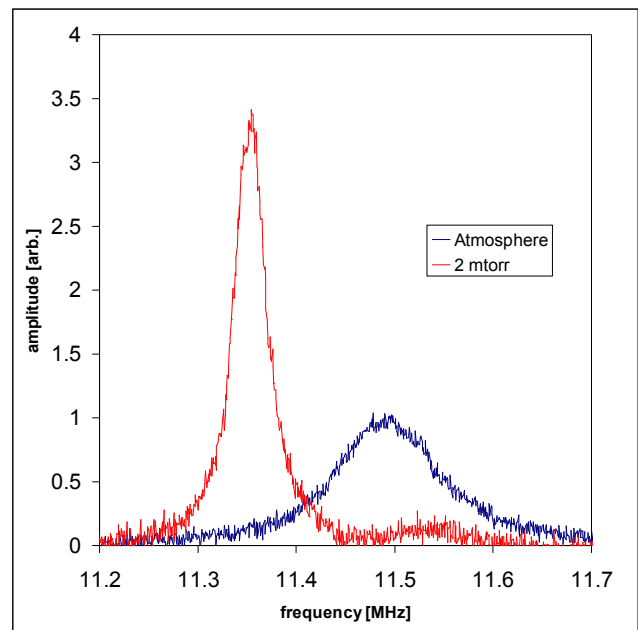


Fig. 8 Frequency response of an 11.35 MHz beam resonator.

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