

Design of an RF Power Harvester in a Silicon-on-Glass Technology

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Abstract—This paper presents a RF power harvester implemented in a silicon-on-glass technology for batteryless tags in short-range wireless communication systems. The power harvester consists of a voltage boosting network and a rectifier circuit. P-type Schottky diodes are used in the rectifiers to increase RF-to-DC conversion efficiency. For a given required output voltage and current, the harvester can be optimized for minimum required RF input power by carefully selecting design parameters such as number of rectifier stages and diode area. Simulation results shows that the harvester can generate 1V DC supply voltage with 2 μ A DC-output current from -16.5 dBm received RF signal at the 50 Ω antenna interface.

Index Terms—RFID, integrated circuit, rectifiers, wireless sensor networks

I. INTRODUCTION

REMOTELY powered wireless systems, such as RF identification (RFID), wireless sensor networks, have enjoyed rapid growth in recent years. They find their applications in logistics control, environment sensing, medical monitoring and ambient intelligence. Fig. 1 shows the block diagram of a typical remote tag in these systems. The RF power harvester which generates the DC power supply for the tag from the received RF signal is an essential component. The efficiency of the harvester will determine the maximum operation distance of the batteryless tag, when powered by a certain power level.

The threshold voltage of the diodes in the rectifiers limits the minimum required input power at the harvester input to obtain a certain DC output voltage. Previous research proposed a voltage boosting network to overcome the threshold voltage limits [1][2]. However, these networks require large size inductors, which are very lossy when implemented in CMOS technologies. Therefore, a silicon-on-glass technology with high-quality passive components and low-threshold Schottky diodes are ideal for implementing RF power harvester [3][4].

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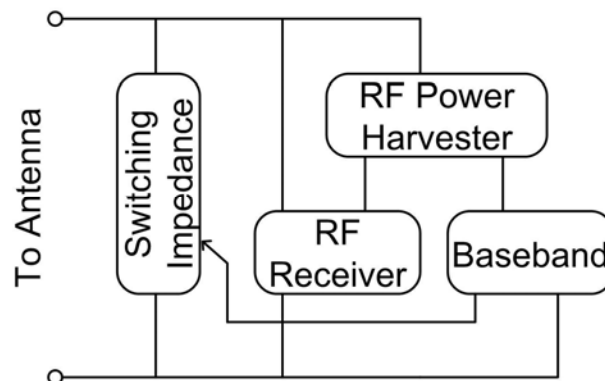


Fig. 1. the block diagram of a typical batteryless tag in remotely powered wireless systems.

There have been different frequency ranges proposed for remotely powered systems, ranging from 125 KHz to 5.8 GHz [5]. Since the power of RF signals at higher frequency decays much quicker than low frequency signals, the ISM band at 868.3 MHz offers a good compromise between operation distance and tag antenna size. The work presented in this paper focuses on the design of a power harvester at 868.3 MHz in a silicon-on-glass technology.

The rest of the paper is organized as follows. The design considerations and selections of design parameters of the power harvester is discussed in detail in Section II. Section III gives the simulation results and layout implementation of the power harvester. Section IV concludes the work.

II. DESIGN OF RF POWER HARVESTER

A. Rectifier

Fig. 2 shows a typical n-stage rectifier with load and its equivalent impedance representation. The load impedance R_{chip} is determined by the desired output DC voltage and the required DC current of 1V and 2 μ A respectively. At its operation point, the rectifier's equivalent input impedance can be represented by a capacitor in parallel with a resistor. In such a rectifier, the parameters available for designers are typically the type of diode, the diode dimensions and the number of stages.

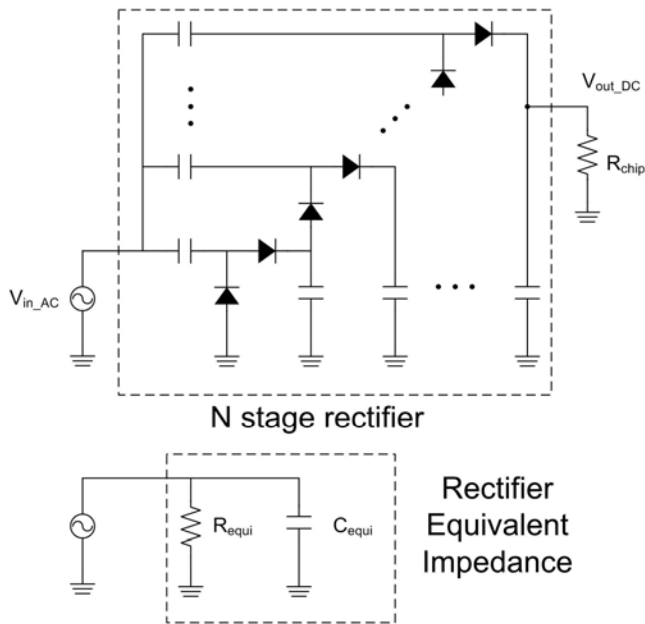


Fig. 2. the schematic of a typical rectifier and its equivalent input impedance representation.

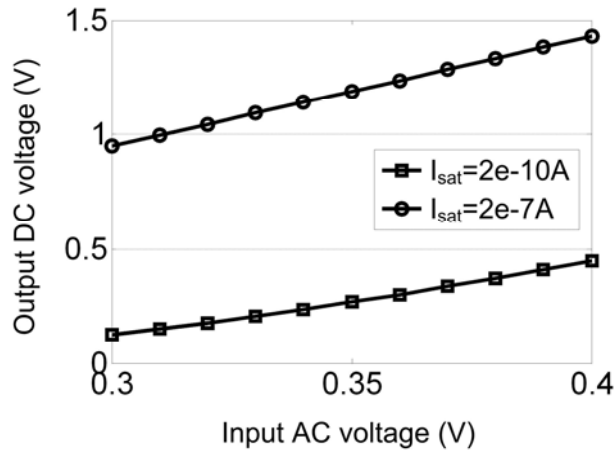


Fig. 3. the DC output voltage as function of the input AC voltage for 3-stage rectifiers employing n-type and p-type diodes. P-type Schottky has a saturation current of $2 \cdot 10^{-7}A$ while the n-type Schottky's saturation current is $2 \cdot 10^{-10}A$. The diode area is $16\mu m$ by $16\mu m$.

First, the diode's parameter that influences the performance most is the saturation current. With the same area, diodes with higher saturation current can provide higher forward current, which results in higher current driving ability of the power harvester. Although higher saturation current leads also to higher reverse leakage, this is normally a minor effect compared to the beneficial much larger forward current, because the reverse DC bias is small especially when the number of stages is large. Fig. 3 shows a comparison of two rectifiers with different Schottky diodes. The smaller junction built-in potential of P-type Schottky diodes gives them higher saturation current compared to n-type Schottky diodes with the same doping level. This makes p-type Schottky diodes a preferred choice in the power harvester design.

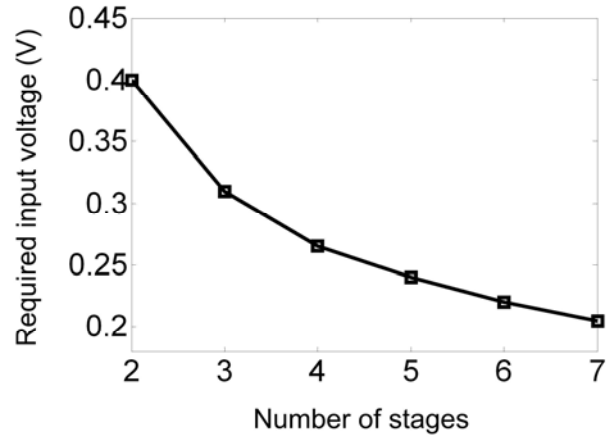


Fig. 4. the minimum required input voltage versus the number of rectifier stages to obtain $2\mu W$ at 1V. The diode area is $16\mu m$ by $16\mu m$.

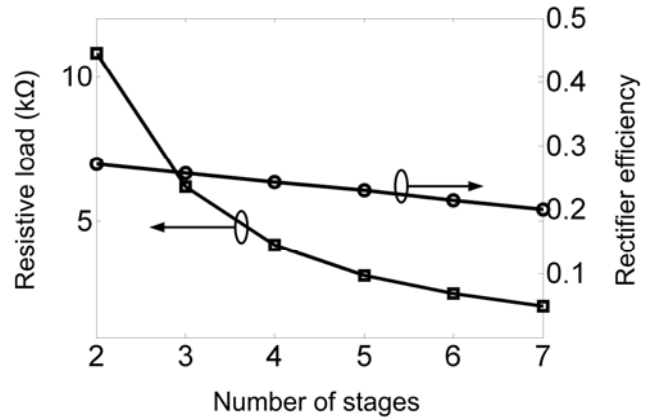


Fig. 5. the equivalent parallel resistance and rectifier efficiency at different number of rectifier stages. The condition is to obtain 1V DC voltage and $2\mu W$ at the rectifier output. The diode area is $16\mu m$ by $16\mu m$.

Second, the number of rectifier stages influences the minimum required voltage at the input in order to obtain a certain output. Fig. 4 plots the minimum required AC voltage at the rectifier input to obtain 1V DC and $2\mu A$. Adding more stages can relax the requirement on AC voltage swing, but introduces more losses as well. That is the reason why the curve starts to flatten out with the increase of stages. If we define the rectifier efficiency by

$$Eff_{Rectifier} = \frac{P_{DC}}{P_{in_{Rectifier}}} \quad (1)$$

where P_{DC} is the output DC power and $P_{in_{Rectifier}}$ is the AC input power to the rectifier. Fig.5 shows the rectifier efficiency versus the number of stages, with a fixed input voltage. The efficiency drops as the number of stages increase. In Fig.5, the equivalent parallel resistance value at different number of stages is also plotted. Adding more stages could reduce the impedance level of the rectifier and making impedance matching much more feasible. Therefore, the number of stages has to be designed together with the voltage boosting network to reach an optimum state for the complete harvester.

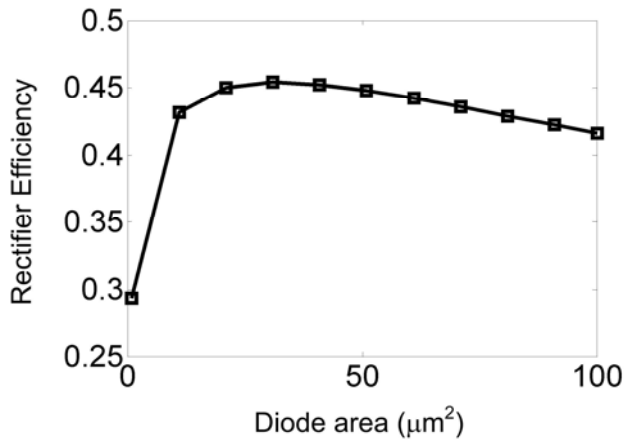


Fig. 6. the rectifier efficiency versus diode area, with a 0.4V input AC voltage.

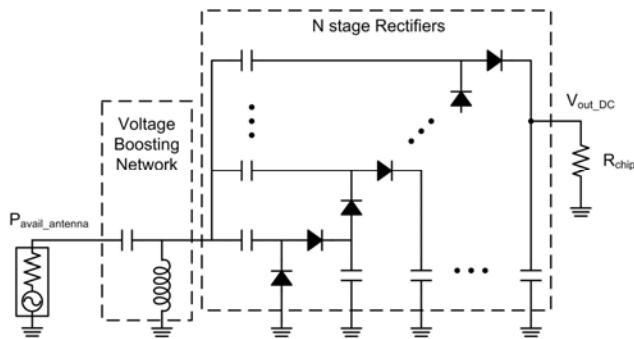


Fig. 7. schematic of the RF power harvester including the voltage boosting network and the n-stage rectifier.

Third, the area of the diodes in the rectifier has its optimal value as well. If the diode is too small, it cannot provide sufficient forward current. If it is too large, the loss through its parasitic capacitance becomes the limiting factor. Fig. 6 shows the rectifier efficiency at different diode sizes with a fixed input voltage. In addition, the area of the diode will influence the input impedance of the rectifier and consequently, influence the design of the matching network for maximum harvester efficiency. Therefore, the area of the diode should be determined in combination with the matching condition for the voltage boosting network.

B. Voltage Boosting Network

The function of the voltage boosting network is to provide a high enough AC voltage swing at the rectifier input in order to obtain the required DC voltage from the available RF power at the antenna.

As shown in Fig. 7, a LC-network using high quality passive components from the silicon-on-glass technology was employed in this design.

C. Design Parameter Selection

As discussed previously, the number of rectifier stages and the size of the diodes must be designed in conjunction with the voltage boosting network. For any number of stages, the

TABLE I
MINIMUM REQUIRED RF POWER TO OBTAIN 1V AND $2\mu\text{W}$

	$10\mu\text{m} \times 10\mu\text{m}$	$12\mu\text{m} \times 12\mu\text{m}$
N=2	-14.7dBm	-13.7dBm
N=3	-15.1dBm	-14.2dBm
N=4	-15.2dBm	-14.4dBm
N=5	-15.2dBm	-14.3dBm
N=6	-15.1dBm	-14.2dBm
N=7	-14.9dBm	-14.1dBm

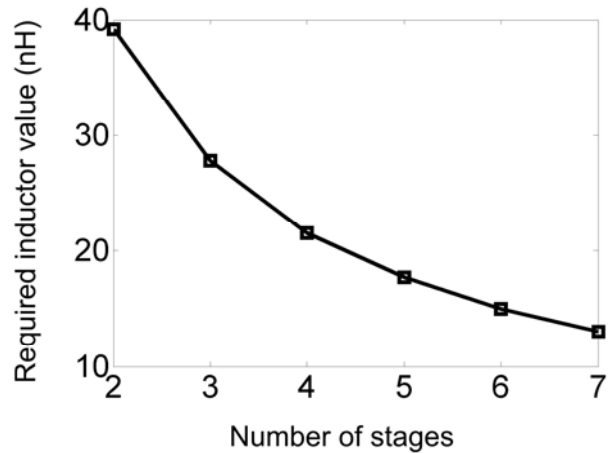


Fig. 8. the required inductor values in the voltage boosting network to achieve minimum required RF power level for obtaining 1V DC voltage and $2\mu\text{W}$ DC power, versus the number of rectifier stages. The diode size is $10\mu\text{m}$ by $10\mu\text{m}$.

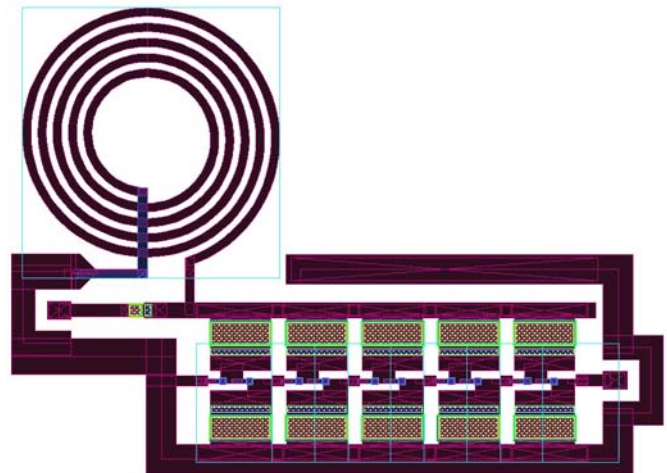


Fig. 9. the layout of the RF power harvester

optimal diode size and the corresponding inductor and capacitor values in the voltage boosting network, to obtain a certain DC voltage and current (for this design 1V and $2\mu\text{A}$), with minimum available RF power can be found by simulation. Table 1 shows the minimum required RF power at the 50Ω antenna interface versus the number of stages at two different diode area. The required inductor values for different stages are plotted in Fig. 8. A rectifier with 5 stages and diode size $10\mu\text{m}$ by $10\mu\text{m}$ requires the lowest RF input power and a reasonable size inductor. Please note that this simulation is done under the assumption that the quality factor of the inductor is 20.

TABLE II
RF POWER HARVESTER PERFORMANCE SUMMARY

Technology	Silicon-on-Glass
Operating frequency	868MHz
Sensitivity for 1V DC voltage and 2 μ W	-16.5dBm
Harvester efficiency	8.93%
Chip dimensions	1500 μ m x 2000 μ m

III. IMPLEMENTATION AND SIMULATION RESULTS

The circuit is implemented in an in-house silicon-on-glass technology. The technology provides 1 thick Cu metal layers and two aluminum layers.

Fig. 9 shows the layout of the complete RF power harvester. The size of the complete chip is 1500 μ m by 2000 μ m.

The simulated result shows that 1V and 2 μ A can be achieved with -16.5dBm RF signal at the antenna interface. This improvement compared to the previous simulation in Table II is due to the higher implemented inductor quality factor, which is 32 from post layout simulation instead of 20 as used in the previous simulations. Table II summarizes the simulated performance.

IV. CONCLUSION

An RF power harvester is implemented in a silicon-on-glass technology with p-type Schottky diode. Thanks to careful circuit parameter selection and the high-quality passives in the technology, the harvester can provide 1V DC supply voltage at 2 μ A output current from a -16.5dBm received RF signal at 50 Ω antenna interface. With this result, it has been demonstrated that the silicon-on-glass technology is a promising candidate for implementing high-efficiency RF power harvesters.

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