

# Profile Engineering of Decreasing Arsenic Doping in Silicon RPCVD

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**Abstract**—Investigation of different techniques for creating decreasing arsenic doped profiles in Si RPCVD is presented. Techniques that do not require As removal from the surface, such as taking advantage of the temperature dependence of the As incorporation rate and counter-doping with B are considered. Furthermore, As removal techniques are considered, e.g. desorption upon baking and chemical removal. Each technique is discussed with respect to effectiveness and technological applicability.

**Index Terms**—Arsenic doping, Reduced pressure chemical vapor deposition, Silicon epitaxy, Surface segregation

## I. INTRODUCTION

PRECISE engineering of doping profiles can greatly improve the performance of Si based devices, especially for microwave and RF applications. For example, in bipolar technology tailoring the collector with a non-uniform doping profile can enhance high-frequency behaviour [1], and for varactor diode-based circuit topologies high-Q “distortion-free” tunable capacitive elements for RF adaptivity have recently been presented [2].

In-situ doping during CVD epitaxy was shown to provide a high degree of versatility and accuracy in fabricating profiles. For example in [3] we showed that by investigating the surface segregation of As during low-temperature epi growth, the dependencies of parameters important for the growth and segregation kinetics on the As surface coverage and the arsine partial pressure could be obtained. Knowledge of these dependencies was employed in simultaneous As deposition and Si epi growth to obtain highly-controllable monotonically increasing doping profiles by appropriate variation of the arsine partial pressure.

On the other hand, the growth of decreasing arsenic doped profiles, particularly those with sharp transitions from high to low doping, are complicated by the surface segregation of As. Terminating only the deposition of As will result in an

exponentially decreasing doping profile with a characteristic length unacceptable for a majority of applications. A sharp drop in doping can be obtained only by removing As from the surface [3].

In this paper we evaluate different techniques for creating decreasing doping profiles by discussing their benefits and shortcomings. Special attention is devoted to removing As from the sample surface before continuing with Si epitaxy. Our research was motivated by the demand for low doping in the surface layer for varactors, but abrupt doping control is attractive for many other device applications.

This paper is organized as follows: chapter II introduces the As surface segregation in Si RPCVD; chapters III and IV discuss various techniques for creating decreasing doping profiles, with chapter IV considering specifically techniques in which As surface layer is being removed; and chapter V presents the conclusions.

## II. ARSENIC SURFACE SEGREGATION

### A. Segregation Process Model

Growth of an arsenic doped Si RPCVD epi layer is dominated by the effects of As surface segregation [4][5]. Arsenic atoms deposited from the gas phase do not remain incorporated at the point of deposition, but instead continue segregating to the surface during Si epi growth. However, a small fraction of As atoms does remain in the incorporated state which results in an As doped Si epi layer. The number of incorporated atoms and consequently the doping level  $N_d(x)$  is proportional to the As surface coverage  $\theta$  as [3]

$$N_d(x) = i_R N_{Si} \theta, \quad (1)$$

where  $\theta$  is expressed as a fraction of a full monolayer,  $N_{Si} = 5 \cdot 10^{22} \text{ cm}^{-3}$  is the concentration of Si atoms in the lattice and  $i_R$  is the constant of proportionality called the incorporation rate.

Silicon epi growth and As deposition are described by [3]

$$dx = g_R dt \quad (2)$$

and

$$d\theta = d_R P_{As} dt, \quad (3)$$

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where  $x$  denotes epi thickness,  $g_R$  and  $d_R$  are growth and deposition rates, respectively, and  $P_{As}$  is the gas partial pressure of arsine ( $AsH_3$ ) in the deposition chamber. When Si epi growth and As deposition are being used simultaneously, the number of atoms on the surface obeys the continuity equation [3]

$$d(N_{ML}\theta) = -N_d(x)dx + N_{ML}d_R(\theta)P_{As}(t)dt, \quad (4)$$

where  $N_{ML} = 6.8 \cdot 10^{14} \text{ cm}^{-2}$  is a surface density corresponding to a full monolayer on (100) surface, and  $dx$  and  $dt$  are related by (2).

### B. Profile Growth

With the knowledge of important parameters and their functional dependencies on the As surface coverage and arsine partial pressure, the previous model can be used to determine the necessary  $P_{As}(t)$  dependence that results in the desired doping profile. However, certain restrictions to the range of possible doping profiles apply. Probably the most pronounced is the problem of creating decreasing doping profiles.

Our experiments were performed on the ASM's epsilon one epi reactor.

## III. CREATING DECREASING DOPING PROFILES WITHOUT REDUCING ARSENIC SURFACE COVERAGE

### A. Arsenic Equilibrium Incorporation

During the Si epi growth and As deposition, the As surface coverage that determines the doping level is being reduced due to As incorporation and increased due to deposition, as can be seen from (4). When As deposition is slower than incorporation, surface coverage decreases with time, which consequently leads to decreasing (in the growth direction) doping profiles.

However, the rate at which the doping level is decreasing in this case has an upper boundary corresponding to the case of no As deposition. Solving (1)-(4) for  $P_{As} = 0$  results in exponentially decreasing profiles

$$N_d(x) = N_d(0) e^{-\frac{i N_{Si} x}{N_{As}}}, \quad (5)$$

an example of which is shown in Fig.1 [3]. Characteristic lengths of these profiles are determined by the incorporation rate, e.g. at 800 °C the characteristic length is approximately 1360 nm [3]. For many applications this is unacceptably long, and other techniques must be utilized.

### B. Reducing As Incorporation

Arsenic incorporation rate is a parameter strongly dependent on temperature. Increase in temperature leads to more effective segregation due to increased energy of atomic vibrations, and this is observed as a lower incorporation rate.

Already at 800 °C, the As incorporation rate is more than ten times lower than at 700 °C [3][6] which means that a drop in the doping level by a decade can be achieved by increasing the growth temperature from 700 °C to 800 °C. Temperature range within which the As incorporation rate can be tuned has an upper boundary of less than 900 °C, as higher temperatures cause significant diffusion, and the lower boundary is determined by the lowest temperature at which a stable and reproducible Si epi can be grown. If the temperature is to be continuously changed during growth, the temperature dependence of the growth rate needs to be taken into account.

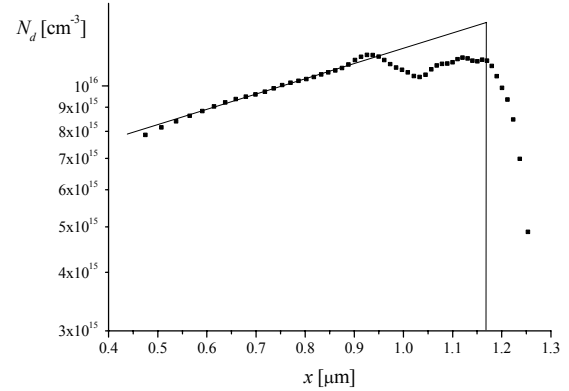


Fig. 1. An example of an exponentially decreasing As doping profile due to As incorporation from the surface layer. A sub-monolayer of As was deposited at approximately  $x = 1.16 \mu\text{m}$  and a layer of Si was grown at 800 °C over it. [3]

### C. Enhancing As Incorporation

As opposed to the approach presented in the previous section, enhancing As incorporation can also be utilized in certain cases. Enhanced incorporation will result in higher doping, but also, as can be seen from (5), in a more sharply decreasing doping profile (and ultimately, low doping levels). For certain applications such an incorporated As peak preceding the doping drop may be exactly desired, or its existence may be irrelevant.

Methods for enhancing As incorporation are reducing the temperature of growth and introducing a catalyzer. We have observed the most effective enhancement with germanium as a catalyzer. Introducing Ge will also lead to its incorporation, but its influence is generally not significant.

### D. Compensating the As Profile with a P-Type Dopant

Regarding the electrical characteristics of devices, equivalent doping level essentially amounts to the difference between p- and n-type doping levels. Therefore, an effective drop in the doping level can in principle be achieved by compensating the As doping with p-type doping.

Our attempts were focused on achieving the compensation with boron, as it is the most commonly used p-type dopant. We have observed that a strong mutual enhancement of the incorporation exists between As and B. Furthermore, As and B appear to have a tendency to incorporate in similar amounts, but not necessarily exactly equal. However, due to the mutual

incorporation enhancement, the process is beyond control. Changes in the partial pressures of precursors have little effect on the growth and incorporation, which makes the process unattractive for profile engineering. However, the phenomena related to parallel As and B doping are not entirely understood, and further research is needed.

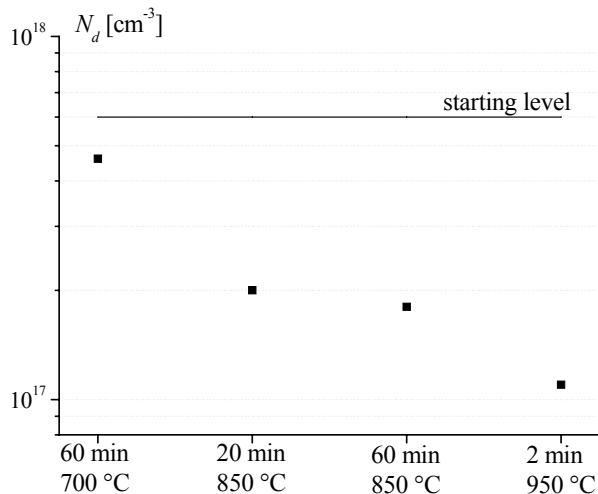


Fig. 2. Reduction in doping levels after baking the sample at different temperatures. A high sensitivity to the baking temperature and a saturation with the baking time is observed.

#### IV. CREATING DECREASING DOPING PROFILES BY REDUCING ARSENIC SURFACE COVERAGE

##### A. Arsenic Bake-off

With the As surface coverage being responsible for the doping of the grown Si epi layer (1), an obvious method to create a decreasing doping profile is to reduce the As surface coverage. The simplest of the techniques is to bake the wafer at an elevated temperature in the reactor chamber while continuously purging the chamber with an inert gas, and thereby allow desorption to reduce the coverage.

At lower temperatures, desorption is weak and the coverage cannot be considerably reduced within reasonable time. As it is shown in Fig.2, baking the wafer for one hour at 700 °C creates only a minor decrease in coverage. Baking at 850 °C reduces the coverage more substantially, but the dependence on the baking time is very weak (Fig.2). This indicates that the binding energy of As atoms to the Si surface is not uniform, as the uniform binding energy would result in the surface coverage exponentially decreasing with time, which is evidently not the case.

Baking at 950 °C further decreases the doping level, but the improvement compared to 850 °C is not as significant as expected. At 950 °C the diffusion of the As profile is not negligible. This both adversely affects the shape of the profile, and creates further segregation from deeper layers. An example of a successfully employed bake-off and enhanced incorporation due to the presence of Ge is shown in Fig.3 [4].

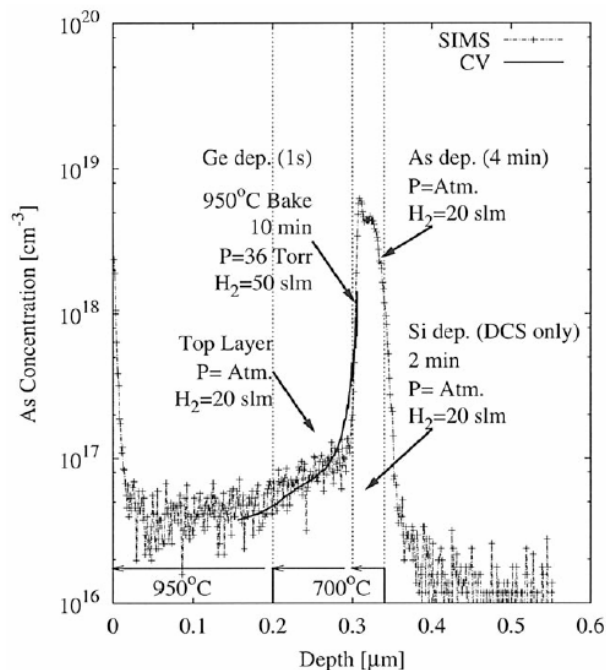


Fig. 3. An example of a successfully grown As doping profile including a moderately sharp drop in doping. The drop was achieved by two means: Ge was introduced to enhance As incorporation, and the sample was baked at 950 °C for 10 min to reduce the As surface coverage by desorption. [4]

##### B. Chemical Removal Inside the Reactor

The etchant typically used to clean the reaction chamber is the HCl gas. Introducing it at the point when As removal is desired would most likely etch clean the wafer. However, this process also damages the wafer surface and we have not succeeded in continuing the growth of high-quality Si epi after the etching has been done. Further experiments that would possibly overcome this technological problem could prove this technique viable.

##### C. Chemical Removal Outside the Reactor

A conceptually simple method for removing the As coverage layer is to chemically clean the wafer surface outside the epi reactor, and then continue the growth.

Two main problems are related to this method. First, it is evidently not suitable for creating decreasing profiles with a finite steep slope, but instead can be used to create only discrete drops in the doping level. It is not possible to controllably chemically remove only a fraction of the coverage, but an equivalent result can be achieved by cleaning the surface completely and then re-depositing the desired amount.

Second, it is technologically challenging to grow a high-quality Si epi without a pre-baking step at temperatures equal or higher to 900 °C. However, such a high-temperature pre-baking step causes As diffusion and a deformation of the previously grown doping profile. Essential to achieving high-quality Si epi without the high-temperature pre-baking step are cleaning and drying steps immediately prior to epi growth. These steps should ideally result in a perfectly smooth surface with no contaminating particles and no native oxide.

The exact arsenic removal and pre-epi cleaning sequence we have employed is standard wet (HNO<sub>3</sub>) cleaning with dilute HF as last step. Dilute HF (0.55%/4 min.) provides hydrophobic, hydrogen-terminated surface. The following drying step is essential in achieving a free contaminated surface, stable for some time: and we have thus employed Marangoni drying with IPA. By this method, we have been able to remove completely the As surface coverage and continue the Si epi growth with pre-baking at 700 °C.

## V. CONCLUSIONS

Techniques for creating decreasing doping profiles have been discussed. Their respective advantages and possibilities have been analyzed together with the difficulties involved. Taking advantage of the temperature dependence of the incorporation rate was found to be the most promising technique for creating moderately varying continuous profiles, while chemical removal of As surface coverage was found to be the most effective technique for creating large and sharp discrete drops in doping.

## ACKNOWLEDGMENT

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