

A new current calibration scheme suitable for generic DAC architectures

G.I. Radulov¹, J.A. Hegt¹, P.J. Quinn²,
and A.H.M. van Roermund¹

¹Mixed-signal Microelectronics group, Eindhoven University
of Technology, Eindhoven, The Netherlands,
web: www.msm.ele.tue.nl, e-mail: g.radulov@tue.nl

²Mixed Signal Design Group, Xilinx, Dublin, Ireland

Abstract — This paper presents a new start-up calibration method and algorithm for current-steering D/A converters. The method extends the ideas presented in [1] and the proposed current cell allows its application on generic DAC architectures, i.e. binary, thermometer, segmented. With respect to the thermometer type implementations, the binary implementations are area efficient and the calibration may even further reduce their size. Unlike the thermometer converters, which use identical currents, the binary converters are problematic for calibration at the level of current sources due to the different weights of their current sources.

A new transistor level architecture for scaled current cells is proposed. It uses a set of parallel calibrated unit elements to construct a signal current source. When after the calibration, these are assembled back, the accuracy of the current sources is improved. Moreover, the method is independent from the architecture of the converter. Therefore, for all current-steering DAC architectures, an optimal area solution through optimising the calibration strength exists.

Further, the paper analyses the start-up calibration requirements for generic DAC architectures. It offers a tool to estimate the calibration strength for an optimal area solution. An example of a 12-bit self-calibrated DAC, a high-level model and simulations verify the presented and analysed method. A general discussion on the advantages and constraints of the new calibration method is offered and conclusions are drawn.

Keywords— calibration; binary, thermometer, segmented current-steering DACs; area optimisation.

I. INTRODUCTION

For several decades, the D/A research efforts of both the academia and the industry are dominated by current-steering approaches. Nowadays, these converters may achieve up to 16-bits of static linearity for a price that is still paid for by large silicon areas. To save silicon area, two orthogonal approaches are

used: binary architectures [2] and self-calibration.

A popular self-calibration method adjusts the currents of the elements that generate the output current. However, this method is not directly applicable to generic architectures (binary, segmented, thermometer), because their current sources might not be identical and hence the reuse of the calibration apparatus is difficult. For example, in the most popular segmented approach, calibration of current sources is limited only to the identical thermometer current sources.

Thus, a new architecture for the current cells that allows reuse of the calibration apparatus will add another degree of freedom to optimise silicon area by optimising the calibration strength. For example, this will lead to even smaller high-resolution binary current steering D/A converters, while the advantages of the calibration method at current sources level are preserved. Moreover, such a current cell will make the DAC area optimization (through calibration) independent from the DAC architecture optimization (for optimal dynamic performance, relaxed DNL, etc.).

Section II of this paper gives an overview on DAC calibration and its problems and requirements. Section III presents a new self-calibration method, suitable for generic DAC architectures. It offers an analysis on the estimation of the calibration strength for an optimal area solution. Section IV presents an example of a 12-bit self-calibrated DAC that justifies the new calibration method. Section V considers the advantages and the constraints of the new method and the presented analysis. Section VI draws conclusions.

II. OVERVIEW OF DAC CALIBRATION

DAC calibration offers two important benefits: reduction of the silicon area and automatic detection and correction of production tolerances.

To save silicon area, the intrinsic accuracy of the DAC, and hence its static linearity, is designed lower than its resolution. After manufacturing, additional smart on-chip circuits and automated operations improve the accuracy of the DAC. During this process any production tolerances will also be corrected, which improves the chip yield. Generally, these operations build on two sub-processes: *self-test* and *self-calibration*. Firstly, information is acquired about the deviation of the actual targeted value from the reference. Secondly, calibration activities minimise that deviation. Both sub-processes of *self-test* and *self-calibration* are often interleaved and simply referred to as calibration.

The DAC accuracy can be improved either directly, at the output of the DAC [3], or via improvement of the accuracy of the current sources, [4], [5]. While the former approach is independent of the DAC architecture but deteriorates the DAC output response, see [1], improving the accuracy of the signal current sources requires a calibration apparatus that is custom-made to the DAC architecture but features a smaller negative impact on the intrinsic DAC performance. Thus, to preserve the dynamic performance, the second approach demands more resources to correct at the level of the current sources.

These DAC designs use segmentation and only the accuracy of the thermometer current sources is to be improved, see [4], [5], [6]. The contribution of the thermometer current sources to the output current is greater, because they generate the current for the more-significant bits. Furthermore, the thermometer current sources are identical, so a shared calibration circuitry and logic may be used. These practical reasons on one hand couple the choice of the segmentation level with the calibration apparatus and on the other hand make it difficult to implement self-calibration to the current sources in a fully binary design. Moreover, the choice of the calibration strength, which sets the area requirements, is not independent from the DAC architecture, since imperatively only the thermometer current sources are corrected. This does not allow a degree of freedom that balances the non-calibrated and the calibrated parts of the system.

To be motivated, the extra silicon area of the calibration circuitry should not exceed the area that is saved thanks to the reduced accuracy of the intrinsic DAC core. Other important problems and requirements include the introduction of additional errors, the impact and influence of the calibration circuitry and

activities on the normal operation of the DAC and vice versa.

Due to these difficulties, many designers avoid calibration. Thus, research is needed towards simple calibration schemes and methods that have a minimised negative impact on the normal operation of the DAC, correct their own errors at system level, and are technology independent. Furthermore, these have to be generic enough to allow a direct implementation on the three main DAC architectures: binary, thermometer, and segmented.

This paper presents a new start-up¹ self-calibration scheme that allows calibration of non-identical current sources by way of a shared calibration circuitry. It shows that based on this new current cell the optimization of the DAC architecture regarding the dynamic performance and relaxed DNL is decoupled from the area optimization via calibration.

III. NEW METHOD AND ARCHITECTURE FOR SELF-TESTING SELF-CALIBRATING CURRENT-STEERING D/A CONVERTERS WITH A GENERIC ARCHITECTURE

A. A new self-test self-calibration scheme for scaled current sources

To minimise silicon cost, the proposed self-test scheme uses a 1-bit ADC (a current comparator) as a measurement device. The single bit of information can be sufficient for calibration, providing a smart digital algorithm that extends its usefulness, similarly to the Successive Approximation ADCs [4] or the Successive Increment approach of Tiilikainen [7]. The overhead of digital circuitry is preferred over an increased number of bits of the ADC because of the two following reasons:

- The digital silicon area is steadily getting cheaper than the analog silicon area, viewed from the prospective of CMOS technology evolution.
- 1-bit ADCs are linear by definition and hence their only non-ideal property is the **input offset**.

The unavoidable comparator input offset I_{offset} is compensated at system level by the proposed calibration scheme. The scheme consists of two parts: phase A (ϕ_A) and phase B (ϕ_B), see Figure 1.

During ϕ_A , a temporary current source I_{temp} is adjusted to the reference current I_{ref} ; the comparator input offset I_{offset} is inherently also recorded; the result of the calibration is stored.

$$\phi_A: \quad I_{\text{temp}} \approx I_{\text{ref}} + I_{\text{offset}} \quad (1)$$

During ϕ_B , the reference current I_{ref} is disconnected

¹ See [1] for a classification of the calibration methods.

from the input of the comparator and the current to be calibrated, named *calibrated unit element (CUE)* I_{cue} , is connected. Consequently, it is adjusted to I_{temp} . I_{offset} affects the self-test process with an opposite sign, so I_{cue} is calibrated to I_{ref} , free of offset:

$$\phi B: \quad I_{cue} \approx I_{temp} - I_{offset} \approx I_{ref}. \quad (2)$$

Therefore, the unavoidable comparator offset I_{offset} , and hence the implementation of the comparator, sets no constraints on the proposed *self-test* scheme.

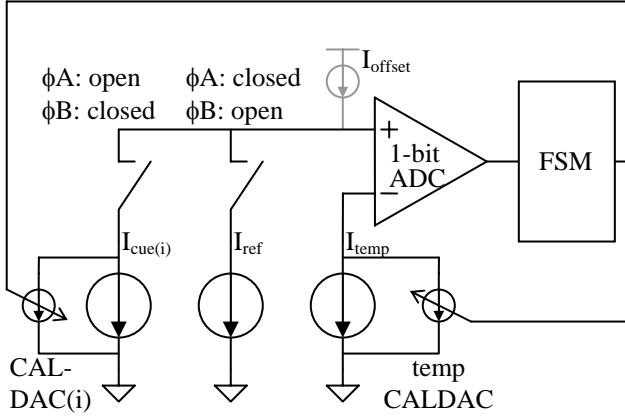


Figure 1. Proposed self-test high-level scheme.

Mini-calibration D/A Converters (CALDACs) implement the *self-calibration* capability. They provide fine currents that correct the deviation of the coarse currents. Thus, every signal current source to be calibrated consists of a main coarse current source and a parallel CALDAC. The transfer characteristic of the CALDAC is discrete. Therefore, the fine currents correct the coarse currents within a random quantization error I_q that is set by the Least-Significant-Bit current I_{lsbc} of the CALDAC. The post-calibration spread of the calibrated currents is due to this quantisation error. The calibration algorithm minimises the post-calibration spread of the calibrated currents through controlling the quantization error in both phases.

The post-calibration spread is minimized in a similar way like the compensation of the comparator input offset I_{offset} . In ϕA , I_{temp} is always adjusted to I_{ref} within a positive I_q , which results in a uniform post-adjustment distribution with spread I_{lsbc} and a mean value $I_{ref} + \frac{1}{2}I_{lsbc}$. In ϕB , I_{cue} is always adjusted to I_{temp} within a negative I_q that results in a triangular post-adjustment distribution with standard deviation $\sigma_{cue} = \frac{I_{lsbc}}{\sqrt{6}}$ and a mean value equal to I_{ref} .

The *self-test* described above and the actual *self-calibration* is applied to nominally identical current sources that are referred to as calibrated unit elements (CUE), I_{cue} , see Figure 2.

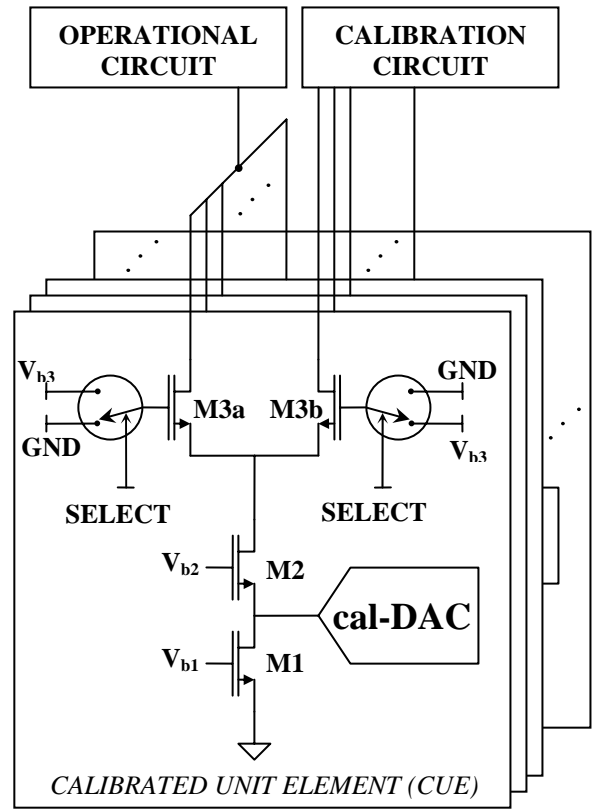


Figure 2. A self-calibrated (binary, thermometer, scaled) current source, composed of parallel calibrated unit elements.

Calibration of identical current sources allows the use of a shared calibration circuitry, in terms of the measurement device, the digital control logic, the temporary current source I_{temp} , and instances of identical CALDACs. These calibrated unit elements (CUEs) construct the scaled binary current sources. For example, the M^{th} -bit binary current source I_M is constructed by 2^L identical I_{cue} . Then, the $(M+1)^{\text{th}}$ -bit binary current source I_{M+1} is constructed by 2^{L+1} identical I_{cue} , etc. Thus, every coarse current source to be calibrated is composed by these calibrated unit elements, as shown in Figure 2. The start-up calibration apparatus individually improves the accuracy of every calibrated unit element. Consequently, the accuracy of the (binary-scaled) signal current sources is improved. Ultimately, the specified static linearity of the binary DAC system is achieved.

NMOS transistor M1 generates the coarse current $I_{cue(i)}$ and the correcting-it fine current is generated by the cal-DAC connected to the drain of M1. The cascode M2 shields the generation of $I_{cue(i)}$ from the calibration and operational circuits and increases the output impedance of the self-calibrated current source $I_{cue(i)}$. The switches M3a and M3b redirect the current to be used either by the D/A converter or by the calibration circuit. To construct the scaled binary current, several CUEs are connected in parallel, but

each of them is calibrated separately.

The non-calibrated current sources have a similar architecture like those that are to be calibrated. There is no CALDAC and the current sources are scaled with respect to the CUE. The non-calibrated current sources and one additional LSB current source are summed in parallel during the calibration ϕ_A to construct the reference current I_{ref} . This approach minimises the DNL error in the DAC transfer characteristic at the transition point between non-calibrated and calibrated bits, see [7].

The non-calibrated current sources and the remaining post-calibration mismatch in the calibrated current sources set the post-calibration static DAC linearity. An optimal, in terms of silicon area, DAC design has a balance between the calibrated and non-calibrated current sources, i.e. between the required intrinsic accuracy and the devoted resources for calibration. This trade-off is discussed in details in the following section.

B. Area driven optimum of the level of calibration

Two design specifications set the calibration strength:

- The post-calibration static accuracy of the DAC, dictated by the required INL.
- The intrinsic (before calibration) accuracy of the DAC, INL_0 .

While the first design specification is often imperative, e.g. $INL < 0.5LSB$, the second specification is a designer choice and it has a great impact on the area of the converter. The second specification also sets the required calibration strength, being from weak to aggressive.

On one hand, an *aggressive calibration* is when the intrinsic DAC accuracy is very poor and it is improved to the specified level. In this case, the majority of current sources are calibrated and the CALDACs have large full-scales, whereas the most aggressive calibration would calibrate all current sources and the CALDACs would have infinite full-scales. On the other hand, a *weak calibration* is when the intrinsic DAC accuracy is close to the specified level. In this case, a minority of current sources are calibrated and the CALDACs have small full-scales, whereas the weakest calibration would mean no need of calibration – the intrinsic accuracy of the DAC is equal to the specified level.

Therefore, an aggressive calibration implies a very small area of the coarse current sources and a large area of the CALDACs. A weak calibration implies a very large area of the coarse current sources and a small area of the CALDACs. For both cases, the area

of the self-test and the control circuitry, e.g. measurement devices, digital logic, etc., is constant, see Table 1.

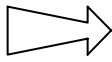

Weak calibration	→	Optimal calibration	←	Aggressive calibration
Large area of the coarse current sources				Small area of the coarse current sources
Small area of the CALDACs				Large area of the CALDACs
Constant area of self-test and control circuitry				

Table 1. Qualitative area comparison between weak and aggressive calibration.

Thus, the area of the coarse current sources and the area of the CALDACs balance the trade-off area of the self-calibrating D/A Converter.

On one hand, as shown in [8], the active silicon area of the coarse current sources is inversely proportional to the 2nd power of their mismatch $\left(\frac{\sigma_I}{I}\right)$.

Furthermore, [9] expresses the statistically expected maximum of the INL for 3 σ confidence level, as a function of the DAC resolution N and the mismatch of the unit elements $\left(\frac{\sigma_u}{I_u}\right)$:

$$INL_{max} = 3\sqrt{2^{N-1}} \left(\frac{\sigma_u}{I_u}\right). \quad (3)$$

To conclude, the active silicon area of the coarse current sources has a square inverse relationship with the intrinsic accuracy of the DAC, INL_0 :

$$(W \times L)_0 = K_1 \frac{1}{(INL_0)^2}, \quad (4)$$

where the constant K_1 depends on the resolution N , the technology constants A_F and A_{VT} , and the $(V_{gs} - V_{th})$ and can be derived from [8], [9]. Therefore, a lower intrinsic accuracy of a DAC (higher INL_0) implies less area for the coarse current sources.

On the other hand, the active silicon area required for the array of CALDACs depends on:

- The number of used CALDACs, i.e. used calibrated unit elements (CUE);
- The area of a single CALDAC.

This results in a function proportional to the 3rd power of INL_0 , as shown next. The number of used CALDACs is 2^{N-B} , with N being the resolution of the DAC and B - the bit implemented as a single CUE. Indeed, 2^{N-B} shows the number of bits that are calibrated. A greater intrinsic INL_0 error requires more calibrated bits, i.e. a smaller B .

To derive the requirements for B, equation (3) is expressed as a function of the accuracy of the non-calibrated unit elements and the CUEs:

$$INL \approx \sqrt{9 \times 2^B (2^{N-1} - 2^B) \left(\frac{\sigma_{cue}}{I_{cue}} \right)^2 + 9 \times 2^B \left(\frac{\sigma_u}{I_u} \right)^2} \quad (5)$$

Thus, the range of static errors, set by the allowed INL, is shared between the calibrated CUEs (the first term under the square root of (5)) and the non-calibrated unit elements (the second term under the square root of (5)). For example, if the error contribution of the non-calibrated current sources is larger, then the error contribution of the CUEs should be smaller, and vice versa. Thus, the error contribution of the non-calibrated current sources may range from 0 (ideally accurate) to full INL, which after minor elaborations of (5) is expressed in:

$$9 \times 2^B \left(\frac{\sigma_u}{I_u} \right)^2 = (1-k) INL^2, \quad (6)$$

where the constant $k \in (0;1)$ indicates the contributions of the non-calibrated current sources and the calibrated current sources to the INL error. $k = 0$ means that the entire INL error is due to the non-calibrated current sources and $k = 1$ means that the entire INL error is due to the calibrated current sources. Expressing 2^B and substituting the relative matching of the unit current sources with an expression derived from (3), the number of the used CALDACs is derived:

$$\frac{2^N}{2^B} = \frac{2}{(1-k)} \times \left(\frac{INL_0}{INL} \right)^2 \quad (7)$$

Furthermore, the area of a single CALDAC is proportional, within a first order approximation², to its full-scale range and inversely proportional to its LSB step, I_{lsbcal} . The latter is set by the required post-calibration INL and it does not depend on the INL_0 . The CALDAC full-scale has to cover the spread of the un-calibrated CUE. This spread is proportionally related to INL_0 via (3) and (5), so:

$$FS_{caldac} = \frac{2 \times I_u}{\sqrt{2^{N-1}} \sqrt{2^B}} \times INL_0 = F(N, B, I_u) \times INL_0 \quad (8)$$

Thus, a larger intrinsic INL_0 means a larger spread of the CUE currents, which requires the CALDACs to provide correction current over a larger range. Since the LSB step of the CALDAC depends only on the required post-calibration accuracy, a larger range of

the CALDAC correction current requires proportionally more silicon area, discarding the error that the CALDACs would normally be binary. Combining (7) and (8), the required active area for the array of CALDACs cubically depends on the intrinsic INL_0 .

$$(W \times L)_{cal} = K_2 \times INL_0^3, \quad (9)$$

where K_2 is a term that does not depend on INL_0 .

Thus, the total trade-off area of the self-calibrating DAC is the sum of (4) and (9):

$$(W \times L)_{DAC} = \left(K_1 \times \frac{1}{INL_0^2} \right) + \left(K_2 \times INL_0^3 \right) \quad (10)$$

Thus, the minimum, $\min\{(W \times L)_{DAC}\}$, is found for:

$$INL_0 = \sqrt[5]{\frac{2K_1}{3K_2}} \quad (11)$$

Figure 3 graphically shows the relations given by (4), (9), and (10) and the minimum given by (11). Interestingly, the minimum (11) is not the crossing point of (4) and (9), since (9) is a faster increasing function than the decreasing function (4).

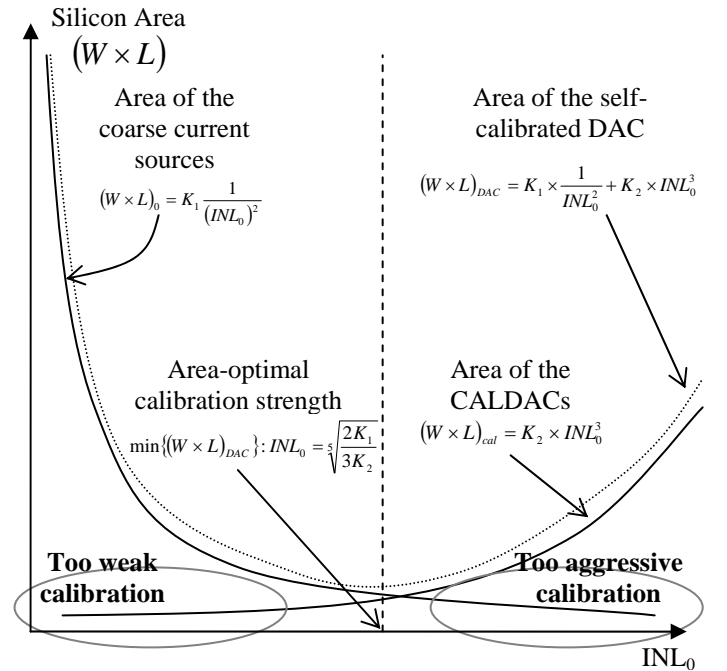


Figure 3. Qualitative graphs of the area requirements for a self-calibrated DAC.

² Only the active area of the CALDAC current sources is taken into account and the area for the memory elements is not taken into account.

IV. EXAMPLE OF A SELF-CALIBRATING 12-BIT BINARY DAC IN AN INDUSTRY STANDARD 0.25 μ m PROCESS

A resolution of 12-bit can be considered as the border between intrinsic and calibrated designs. Not calibrated DACs with higher resolutions and accuracies demand huge area for the signal current sources and hence are unpractical. Calibrated DACs with lower resolutions and accuracies demand small area for the signal current sources, so any extra calibration circuitry would be excessive and hence unpractical. However, for DAC resolutions of 12-bits, there are examples of both approaches: the intrinsic and the self-calibrated. Based on the presented analysis, this section elaborates a practical example to show that for 12-bit D/A converters, calibration is motivated and leads to smaller areas.

Table 2 summarises the process of finding the optimal intrinsic accuracy INL_0 for a 12bit DAC in industry standard 0.25 μ m CMOS process.

Firstly, constant K_1 is derived via calculation of the intrinsic active area for a given INL error, e.g. $INL=0.5LSB$. Secondly, to find constant K_2 , the area of the array of CALDACs should be estimated for a given intrinsic accuracy, e.g. $INL_0=1LSB$. The number of DAC 2^{N-B} is calculated for $INL_0=1LSB$, with assumed equal contribution k of the calibrated and the non-calibrated current sources to the INL error. Next, the full-scale of a CALDAC is calculated based on the spread of the current of the CUE element for the chosen intrinsic $INL_0=1LSB$. Furthermore, to estimate the number of unit-elements of the CALDAC, the LSB step of the CALDAC is calculated based on the target post-calibration $INL=0.5LSB$. Subsequently, the number of the unit-elements of the CALDAC is derived and an estimation of the size of 1 LSB element is assumed. An estimation of the area for the CALDAC memory elements is assumed. The active area of the array of CALDACs is calculated and the constant K_2 is derived. According to the given example, the minimum DAC area would be for intrinsic accuracy error $INL_0=2LSB$ and from (10) it results in 6438 μ m² active area of the coarse current sources and the array of CALDACs, which is compared to almost 10 times greater number of 60'000 μ m² for a 12-bit intrinsic accuracy of the coarse current sources.

Parameter	Symbol	Value
Resolution	N	12 Bit
Technology factor for V_{th}	$A_{V_{th}}$	5.2 $\mu V \times \mu m$
Technology factor for β	A_{β}	1.8 $\mu m \times 10^{-2}$
DAC LSB current	I_u	5 μ A
Active area of the array of current sources for $INL_0=0.5LSB$	$(WL)_0$	59951 μ m ²
Intrinsic area constant	K_1	14988 μm²
Post-calibration INL contribution constant, see (6)	k	0.5
CUE bit for $INL_0=1LSB$	$B_{INL_0=1}$	8
CALDAC Full-scale for $INL_0=1LSB$	FS_{CALDAC}	3.552 μ A
CALDAC LSB step for $INL_0=1LSB$	I_{lsbcal}	255nA
Estimated active area for a single CALDAC LSB element, see [6]	$(WL)_{cal.lsb}$	1 μ m ²
Estimated area for the memory elements of a single CALDAC, [6]	A_{mem}	5 μ m ²
A single CALDAC area for $INL_0=1LSB$	$(WL)_{caldc.1}$ $_{NL_0=1}$	21 μ m ²
Area of the array of CALDACs for $INL_0=1LSB$	$(WL)_{caldacs}$ $_{INL_0=1}$	336 μ m ²
CALDACs area constant	K_2	336μm²
Area optimal intrinsic accuracy INL_0	$\sqrt[5]{\frac{2K_1}{3K_2}}$	2LSB

Table 2. An example of DAC area optimization through calibration.

The presented example suggest that $INL_0=2LSB$ is near the area optimum for a 12-bit binary DAC in an industry standard 0.25 μ m process.

A MATLAB high-level model is built that simulates the presented calibration method for that case. The intrinsic standard deviation of the unit current sources is set to $\sigma_u=74nA$, which corresponds to 10-bit intrinsic accuracy of the DAC. Then, the CALDAC LSB step is calculated to be $I_{lsbcal}<260nA$. The full-scale of a CALDAC is calculated to be 4.1 μ A, rounding its resolution to 4bits. 100 samples were simulated.

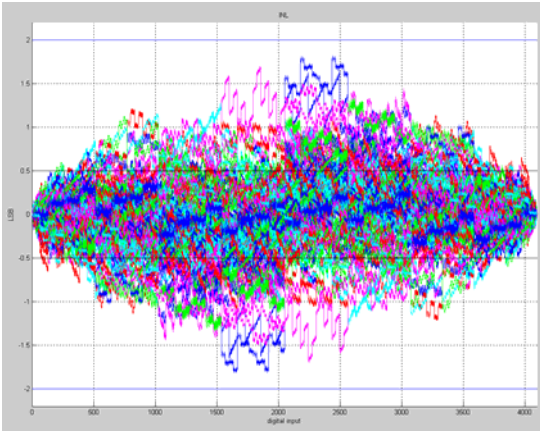


Figure 4. Pre-calibration (intrinsic) INL_0 for 100 DAC samples.

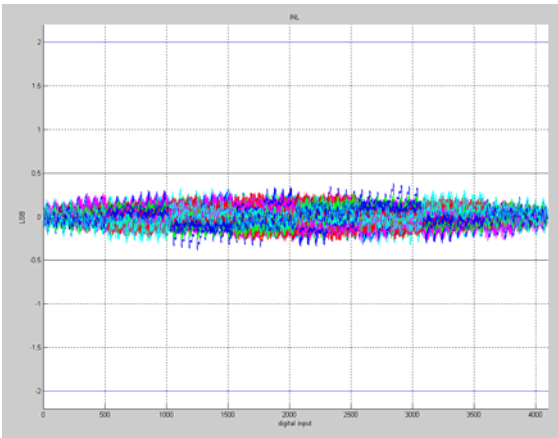


Figure 5. Post-calibration INL_0 for 100 DAC samples.

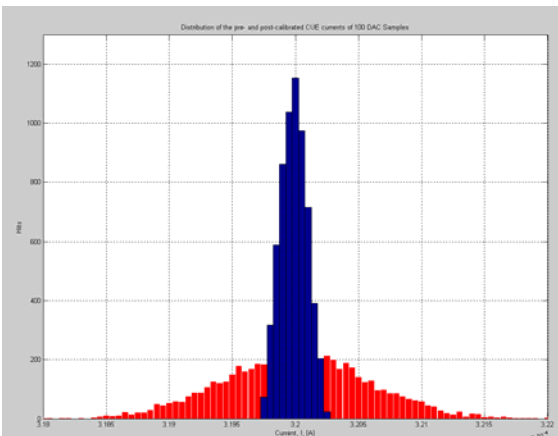


Figure 6. Distribution of the pre- and post-calibrated CUE currents for 100 DAC samples.

V. ADVANTAGES AND CONSTRAINTS

The presented method for scaled current sources calibration can be applied on all DAC architectures, i.e. binary, thermometer, and segmented. Since the segmented DAC architectures include a binary LSB and a thermometer MSB part, it is further considered

as an example of the method implementation.

Depending on the optimal calibration strength with respect to area optimisation, the calibration may appear in three cases, as shown in Figure 7:

- Calibration includes a portion of the binary bits;
- Calibration includes only the thermometer bits;
- Calibration excludes a portion from the thermometer bits.

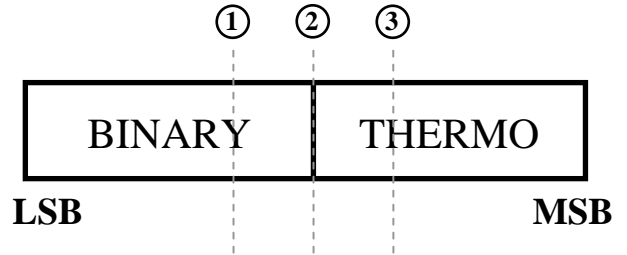


Figure 7. Three cases of the method application on segmented DACs.

Firstly, when the calibration includes a portion of the binary bits, the calibrated binary bits and the thermometer bits are constructed with parallel CUEs. For example, if the 7th bit is the segmented bit, i.e. the last binary bit is the 6th, but the optimal calibration is found to begin from the 5th bit, then the 5th bit is implemented as a CUE, the 6th bit is implemented as 2 CUEs in parallel, and the thermometer current sources are implemented as 4 CUEs in parallel. These are the current sources configurations during the normal operation of the DAC. During the calibration phase, every CUE is calibrated separately.

Secondly, the optimal calibration can be found to include only the thermometer bits. This is the conventional case when the binary bits are not calibrated and only the thermometer bits are calibrated. Then, every thermometer current cell is implemented as a single CUE.

Finally, the optimal calibration can be found to exclude a portion of the thermometer bits. For example, if the 7th bit is the segmented bit, i.e. the last binary bit is the 6th, but the optimal calibration is found to start from the 9th bit, then four thermometer current sources construct 1 CUE. That is to say, the thermometer current sources are calibrated in packs of four in parallel. Thus, a single CALDAC is shared among four thermometer current sources.

Thus, the presented method advances the state-of-the-art techniques with the freedom of setting the calibration strength independently of the DAC architecture. This would lead to smaller and more compact DAC chips, in terms of silicon area. Smaller DACs would reduce the direct manufacturers' costs. More compact DAC chips would reduce the parasitic

capacitances and resistances, e.g. of the interconnection lines, improving the static and dynamic DAC performance!

Furthermore, the presented analysis gives a picture of the trade-off on the calibration strength, in terms of the intrinsic DAC accuracy. It offers a tool for estimation, the accurateness of which is high providing empirical data from realized chips in the target technology. This analysis is a higher level abstraction and it considers only active areas, so a great amount of errors is discarded, e.g. passive inter-transistor area, the CALDACs would be binary, the amount of constant calibration area (measurement devices, control logic), etc. Nevertheless, the designer may descent through the abstraction layers and may include as much data details as needed. However, the principles of the analysis would remain unchanged.

In practice, the presented analysis can be concluded to a simple rule of thumb. The silicon layout area of the calibration circuitry, i.e. CALDACs, measurement devices, digital logic, etc., should be equal to (or slightly less then) the area of the array of the coarse current sources. Such an approach would guarantee that the implementation is close to the theoretically optimal area solution.

Thus, the presented analysis would help designers to quickly estimate a minimal area for a self-calibrated DAC. This would reduce the circuit design cycle allowing a faster market-release of the self-calibrated DAC chip or of the system that includes it!

VI. CONCLUSIONS

The proposed new calibration method is applicable to all DAC architectures. The method is area efficient, as it is based on one shared 1-bit ADC. The calibration scheme is controlled by digital logic, making full use of the single bit of self-test information. The calibration circuitry is reused for all current to be calibrated. The unavoidable input offset of the measurement device is compensated at system level. The post-calibration spread of the calibrated currents is optimised via controlling the quantisation errors of the discrete calibration. The method makes the optimization of the calibration strength independent from the choice of the converter segmentation and hence allows calibration of binary converters. The presented analysis shows that for an area optimal calibration, the array of the coarse current sources and the calibrating-it circuitry should occupy approximately equal areas.

REFERENCES

- [1] G.I.Radulov, P.J.Quinn, J.A.Hegt, and A.H.M. van Roermund, "A self-calibrating current-steering 12-bit DAC based on new 1-bit self-test scheme", IEEE IC Test Workshop, Limerick, Ireland, 13-14 September 2004, pp.49-54.
- [2] Jurgen Deveugele, Michiel Steyaert, "A 10b 250MS/s Binary-Weighted Current-Steering DAC", IEEE Solid-State Circuits Conference 2004, Session 20, Digital-to-Analog Converters, 20.2.
- [3] Yonghua Cong, Randall L. Geiger, "A 1.5V 14-bit 100MS/s Self-Calibrated DAC", 2003 IEEE International Solid-State Circuits Conference, ISSCC.
- [4] W. Schofield, D.Mercer, L. St. Onge, "A 16b 400MS/s DAC with $< -80\text{dBc}$ IMD to 300MHz and $< -160\text{dBm/Hz}$ Noise Power Spectral Density", 2003 IEEE International Solid-State Circuits Conference, ISSCC.
- [5] Alex R. Bugeja, Bang-Sup Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC", IEEE J. Of Solid-State Circuits, Vol. 35, No. 12, Dec. 2000, p.1841.
- [6] G.I.Radulov, "Design of a calibrated 12-bit current-steering Digital-to-Analog Converter", PDEng Thesis, TU/e, Jan. 2004, ISBN 90-444-0362-1.
- [7] Mika P. Tiilikainen, "A 14-bit 1.8-V 20-mW 1-mm^2 CMOS DAC", IEEE J. of Solid-State Circuits, Vol. 36, No. 7, July 2001.
- [8] M.J.M. Pelgrom, et al, "Matching properties of MOS transistors", IEEE J. Solid-State Circuits, vol.24, pp. 1433-1439, Oct. 1989.
- [9] Jose Bastos, "Characterization of MOS Transistor Mismatch for Analog Design", PhD thesis, Universiteit Leuven, ISBN 90-5682-110-5.