

# A CMOS Transimpedance Pre-Amplifier for 40 Gb/s Receiver Design

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*Abstract* — A two-stage transimpedance pre-amplifier is designed for 40 Gb/s applications using 0.13  $\mu\text{m}$  CMOS. Design issues related to transimpedance pre-amplifiers include achieving high gain ( $> 40 \text{ dB}\Omega$ ) and low input-referred noise ( $< 25 \text{ pA/Hz}^{1/2}$ ) over a bandwidth of at least 70% of the 40 Gb/s bit-rate. Phase distortion is of particular importance in high bit-rate receivers where the group delay variation is required to be within 2.5 psec. An input parasitic model of a packaged photo-detector diode is embedded in the post-layout simulation results, which yields the design as a low-power (22.5 mW) alternative to traditionally-based III-V implementations.

*Index Terms* — OC-768, Transimpedance, Pre-Amplifier, CMOS.

## I. INTRODUCTION

Foreseeable consumer demand for broadband services such as 4G wireless systems will flood backend optical networks with an increase in data traffic. These networks will be forced to operate at higher speeds in order to support multimedia tributaries such as 4G handsets. Optical networks will expand in infrastructure, requiring more electro-optical interface equipment at a lesser cost, while next generation optical systems like SONET OC-768 will attempt to stem the influx of traffic at channel data transfer rates in excess of 40 Gb/s. However, improvements introduced by OC-768 will have to scale in tandem with the cost of network exhaustive user devices. In other words, cost-effective Si-based technologies should be further utilized in the realization of high-yield and highly-reliable OC-768 chipsets. This poses a formidable design task for any technology, as fibre system capacity is incriminated by a factor of four every 3-5 years generation (current systems operate at 10 Gb/s while the fibre capacity is in the THz range).

A transimpedance (TIA) pre-amplifier is a circuit that is typically integrated with a photo-detector (as seen in Fig. 1), utilizing high-resistivity and relatively expensive III-V technologies that boast reduced parasitics (i.e., GaAs pHEMT and InP HBT). However, given the improvements of packaging technologies (i.e., flip-chip), the prospect of optoelectronic integration with

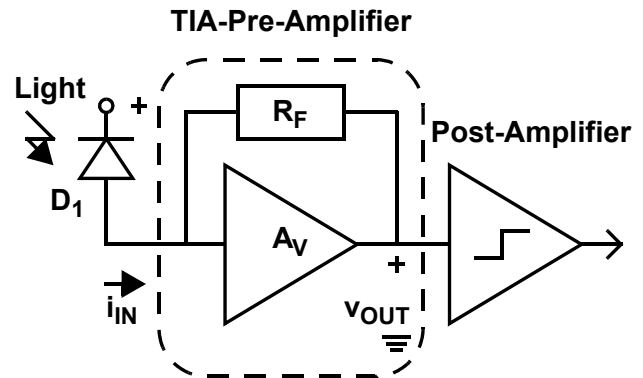


Fig. 1. Simplified optical / electrical front-end highlighting transimpedance pre-amplifier (dashed box).

inexpensive CMOS is encouraging. Unlike III-V technologies, CMOS transistor operation (over low-resistivity substrate) is adversely affected by temperature variation; thus limiting IC designers to low-power implementations for performance reliability (typical TIAs dissipate on the order of hundreds of milli-watts). In spite of this shortcoming, current deep submicron CMOS technologies possess gain-bandwidth products close to 100 GHz, lending itself as a potential candidate for low input impedance 40 Gb/s transimpedance pre-amplifier design.

In this paper, a transimpedance pre-amplifier, implemented in a 0.13  $\mu\text{m}$  CMOS technology is designed for 40Gb/s applications. Positive magnetic coupled coils are used to flatten group delay, transimpedance gain and input-referred noise over a bandwidth adequate for OC-768. Output return loss is better than 10 dB (50  $\Omega$ ) up to 50% of the bit-rate (BR) while DC power is restricted to 15 mA from a 1.5 V supply.

## II. TRANSIMPEDANCE AMPLIFIER DESIGN

The traditional opto-electrical front-end (seen in Fig. 1) shows a p-i-n photo-detector diode used to convert light into electrical current, which precedes the transimpedance pre-amplifier (bounded by dashed box). A post-amplifier typically is used for either adjustable gain

control or limiting the signal swing (as chosen for Fig. 1) in an effort to reduce ISI. The pre-amplifier design and the electrical parasitics related to a packaged photo-detector are considered in this paper. Targeted specifications for this design are derived from [1] and are listed in Table 1.

TABLE 1: DESIGN TARGETS

Specification	Target
Transimpedance	> 42 dBΩ [1]
Bandwidth	> 28 GHz [1]
Noise (Input)	< 25 pA / Hz <sup>1/2</sup> [1]
S <sub>22</sub>	< -10 dB
P <sub>DC</sub> / V <sub>DD</sub>	< 25 mW / 1.5 V

Schematic of the two-stage pre-amplifier is shown in Fig. 2.

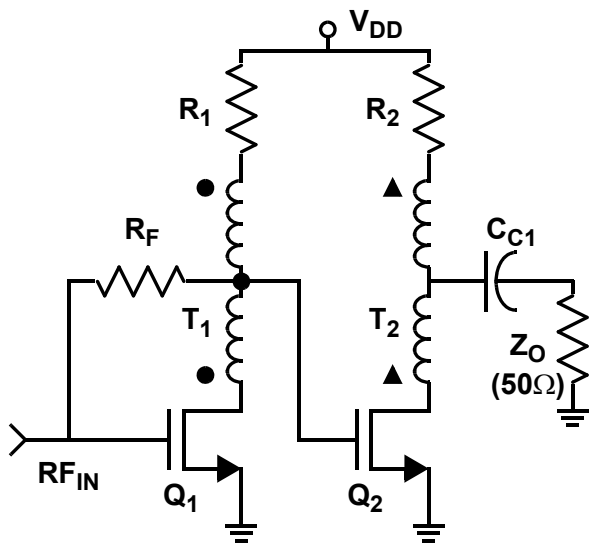


Fig. 2. Schematic of the two-stage transimpedance pre-amplifier.

The first stage is used to stabilize a transimpedance gain around the  $Q_1$ - $R_F$  loop. Transformer  $T_1$  provides broadband signal transfer between the two stages by separating the capacitances inherent to  $Q_1$  from  $R_1$ ,  $R_F$ , and the input capacitance of  $Q_2$ . In a similar fashion,  $T_2$  windings allow broadband signal transfer between the second-stage and the  $50\ \Omega$  output by separating the capacitances of  $Q_2$  (seen at the drain) from  $R_2$  and  $Z_O$  (incl. output bondpad capacitance). The second stage is used as a common-source buffer, improving the isola-

tion between the output and the first-stage. Transformer windings for  $T_1$  and  $T_2$  are magnetically coupled in positive configuration in order to improve the TIA's broadband group delay performance.

The photo-detector / IC interface and its equivalent network used in post-layout simulations is shown in Fig. 3.

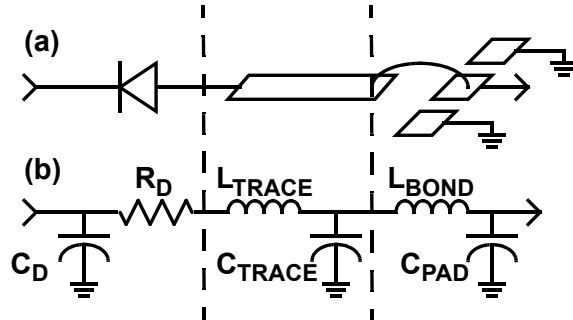


Fig. 3. (a) Input network parasitic to the pre-amplifier (b) Equivalent circuit used in post-layout simulation.

The values used to model the parasitic input network are derived from [2] and are used to consider a more realistic representation.  $L_{BOND}$  has a value of 200 pH and with a  $2\ \Omega$  parasitic resistance, is assumed as a bondwire with length  $\sim 200\ \mu\text{m}$ . Advances in packaging technology can reduce the  $L_{BOND}$  value (e.g. utilizing flip-chip bonding), if desired. However, low-parasitic inductance can also be used to tailor the bandwidth of input-referred noise [1].

### III. SIMULATION RESULTS

The transimpedance gain (shown in Fig. 4) is above the specified target of 42 dBΩ with a -3 dB cut-off frequency of 35 GHz (i.e., 87.5% BR). The moderate gain

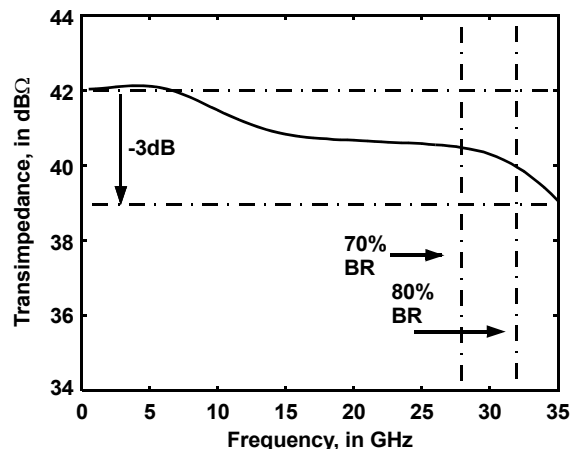


Fig. 4. Simulated transimpedance vs. frequency.

is achieved by modelling the TIA with a low-input impedance (i.e.,  $< 50 \Omega$ ), which is used in reducing the loading-effect of the input bondpad (as seen in Fig. 5).

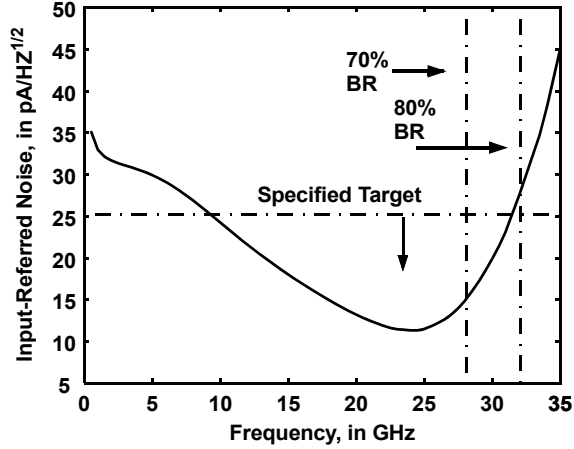


Fig. 5. Simulated input-referred noise vs. frequency.

The specified input-referred noise target of  $25 \text{ pA/Hz}^{1/2}$  is satisfied from 10-32 GHz, which ensures better input-sensitivity (i.e., dynamic range) at these frequencies. Furthermore, at frequencies lower than 10 GHz, the input sensitivity will depend more upon the distortion behavior (i.e., group delay variation)

Phase distortion is of particular importance in pulse-based amplifiers. The linear phase requirement (i.e., group delay  $< 10\%$  of  $1/\text{BR}$ ) inherently becomes more difficult to achieve with each successive generation of TIAs (e.g.,  $10 \text{ Gb/s} \sim 10 \text{ psec}$ ,  $40 \text{ Gb/s} \sim 2.5 \text{ psec}$ ). While each successive generation of semiconductor technology may yield fewer parasitics, and faster devices (i.e., higher  $f_T$ ), linear phase delay (i.e., flat group delay) may not improve concurrently. The positive magnetic-coupled coils used in  $T_1$  and  $T_2$  aid in realizing a flat, broadband group delay variation of  $< 2.5 \text{ psec}$  for the most of the band (up to 28 GHz or 70% BR) as seen in Fig. 6.

The output return loss is of variable importance in TIA pre-amplifier design. While it is imperative that there exist broadband inter-stage matching considerations between pre- and post-amplifiers, the output impedance is not necessarily required to be designed for  $50 \Omega$  system. In this design, a  $50 \Omega$  output impedance was facilitated for on-wafer measuring purposes. The output matching response (seen in Fig. 7) is  $< -10 \text{ dB}$  for a bandwidth up to 50% of the BR. Further improvements in output matching are attainable through the use of a multi-section lumped or a distributed output matching

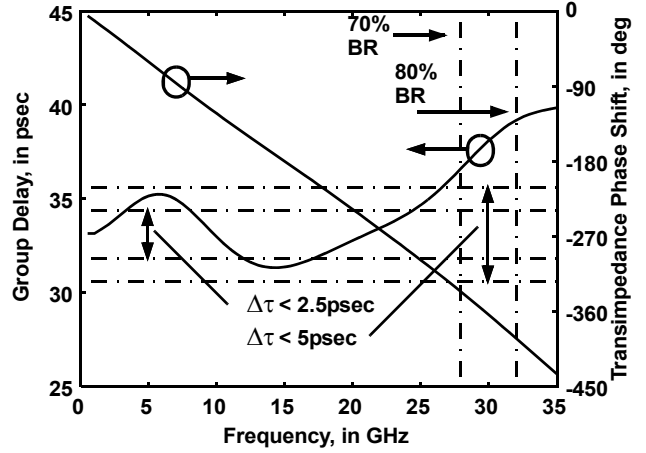


Fig. 6. Group delay with transimpedance phase as reference vs. frequency.

circuit, which may degrade the input-referred noise performance.

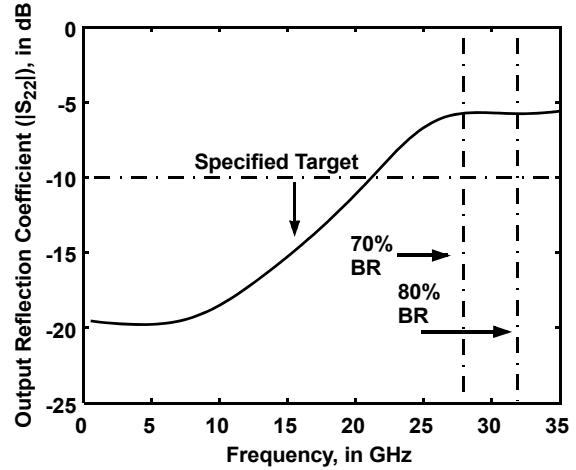


Fig. 7. Output reflection coefficient vs. frequency.

A summary comparing intended TIA pre-amplifiers is listed in Table 2. The measured performance specifica-

TABLE 2: COMPARATIVE SUMMARY

Specification	This Work	[2]	[3]
Technology	0.13 $\mu\text{m}$ CMOS	InP HBT	0.18 $\mu\text{m}$ CMOS
Transimpedance	42 $\text{dB}\Omega$	71.1 $\text{dB}\Omega$	54 $\text{dB}\Omega$
Bandwidth	35 GHz	60 GHz	9.2 GHz
DC Power	22.5 mW	271 mW	137.5 mW
Application	40 Gb/s	40 Gb/s	10 Gb/s

tions of the InP 40 Gb/s TIA [2] are achieved through differential design and under a DC power dissipation of almost 10 times more than in the presented design. However, its superior gain-bandwidth performance lends itself as a candidate for long-haul OC-768 equipment. The CMOS version [3] (intended for 10 Gb/s) better illustrates the technology bottleneck in designing high-performance CMOS TIAs. First, an extra 12 dB in gain is exchanged for approximately 25% of the total bandwidth. Moreover, the gain is improved with multiple amplifying stages and thus, a much greater power consumption (i.e., almost 5-times greater than the presented design) is dissipated. The presented design which also achieves bandwidth extension via inductive peaking, still does not boast as much gain as in [2] and may be more suitable for metro-area network architectures rather than long-haul equipment. However, the much lower DC power consumption of 15 mA drawn from a 1.5 V supply demonstrates that low-cost, low-power TIA design may be an ambition for both future CMOS and 40 Gb/s architectural design.

#### IV. CONCLUSION

In this paper, a low-power 22.5 mW transimpedance pre-amplifier designed in a commercial 0.13  $\mu\text{m}$  CMOS technology ( $f_T \sim 85$  GHz) was presented as an alternative to designs traditionally implemented using expensive III-V technologies. A targeted transimpedance gain of 42 dB $\Omega$  was demonstrated in a post-layout simulation, embedded with expected package parasitics. Positive magnetic - coupled coils are used to broaden the transimpedance bandwidth, minimize group delay variation, and low broadband input-referred noise.

#### ACKNOWLEDGEMENT

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