High Aspect Ratio Copper Electroplating Process for Compact Coplanar Transmission Line Implementation

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***Abstract*—Coplanar waveguide structures with small lateral dimensions have been fabricated using a high aspect ratio copper electroplating process achieving a metal thickness of 15 µm. Measurements show an attenuation of 0.12 dB/mm at 30 GHz for a line with a 15 µm-wide signal path on a glass wafer. This amounts to a twofold reduction of loss compared to a coplanar waveguide with the same signal-line width, but fabricated using a 3 µm-thick Aluminum layer.**

***Index Terms*—CPW, transmission lines, RF passives, micromachining, copper electroplating**

I. Introduction

THE role of RF integrated circuits (RFIC) in the development of modern personal communication systems is undeniably crucial. RFIC technology allows the fabrication of low–cost, miniaturized transmit and receive elements with applications in almost every aspect of daily life. A current issue faced by many RFIC designers, however, is the high area consumption of monolithically integrated passive devices such as inductors and transmission lines.

Transmission lines, which are the biggest passive components in an RFIC are characterized by their length, as well as their overall lateral dimensions. The length of a transmission line depends on the electrical length required by the circuit designer, and on the effective permittivity of the environment, which somehow scales this electrical length to physical length. Those parameters are thus set by design requirements and material constraints and as such, cannot be easily changed. There exists, however, a certain degree of flexibility in choosing the lateral size of a transmission line. In case of a coplanar wave guide (CPW), one can reduce the width of the signal line and the signal-ground spacing without essentially changing the characteristic impedance of the line, which is usually determined by the design environment. This property of a CPW is due to its single plane geometry, which places the ground line on the same plane as the signal line.

Narrowing or scaling down a CPW, however, leads to a significant increase in the insertion loss of the line due to an increase in conductor loss [1,2]. Therefore, most of the conventional CPW designs utilize very wide signal and ground lines [3-5]. In order to be able to build miniaturized CPW lines while maintaining the same or a lower level of loss, one has to compensate the effect of using narrow lines by increasing the thickness of the metal used for the fabrication of the device.

This paper presents CPWs implemented using a high aspect ratio copper electroplating process, achieving a metal thickness as high as 15 µm. Such thick metal layers allow the fabrication of devices with significantly reduced conductor loss. This in return enables the designer to design narrow transmission lines, which is demonstrated in the paper.

II. High Aspect Ratio (HAR) Compact CPWs

A. Structure

High aspect ratio compact CPWs have a slightly different geometry compared to standard CPWs. This difference can be observed in Fig. 1, where the standard CPW line has a relatively thin conductor and electric field is distributed in an elliptic contour. By contrast, a HAR CPW has an additional parallel plate or strip type region. This region can affect the

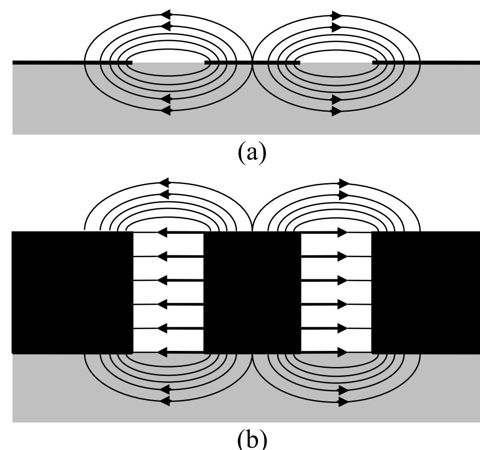

Fig. 1. (a) Standard CPW configuration where electric field has elliptic distribution. (b) HAR CPW where there is an additional parallel plate region.

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line characteristics depending on the spacing between the signal and ground line. Since our structures are narrow structures, this spacing is also small. Therefore this strip type of behavior is more significant compared to wider lines.

B. Theory

The parallel plate or strip region of a compact HAR CPW is not taken into account directly with the usual equations used in conventional (flat) CPW's [1,2]. Those equations calculate the capacitances C_1 and C_2 shown in Fig. 2 using a quasi-static approach and a conformal mapping technique, followed by an empirical thickness approximation.

To extend the conventional CPW model to HAR CPW's, we approximate the strip region as a parallel plate capacitance C_3 (Fig. 2) and to include this capacitance in the calculations. This approach was used to derive preliminary characteristics of the lines. Using this approach enables the designer to make quick calculations to estimate the characteristics of the transmission line without going into detailed simulations.

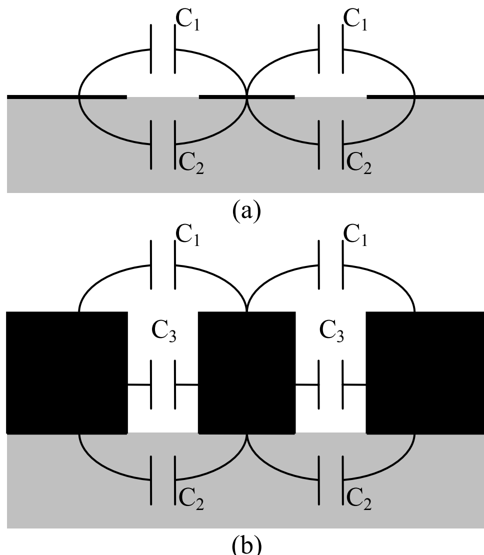

Fig. 2. (a) Standard CPW equations take into account C_1 and C_2 only. (b) In this work C_3 is also calculated as a parallel plate capacitance.

C. Design

Three different coplanar (CPW) lines were designed on a high-resistivity Silicon (HRS) substrate, and on a glass substrate using the high aspect ratio (HAR) process. The CPWs had a signal-line width of 5, 10, and 15 µm. Spacing between signal and ground were 15, 20, and 23.5 µm, respectively, leading to characteristic impedance close to 50 Ω for all the lines on HRS. Lines with the same signal width are designed for the flat Al case with same characteristic impedance.

III. Fabrication

High aspect ratio electroplated copper structure fabrication is a simple one-lithography-step process. The process is cost effective and can be implemented within standard IC fabrication equipment. It is designed as a post processing module to be added after RF IC fabrication depending on the demand.

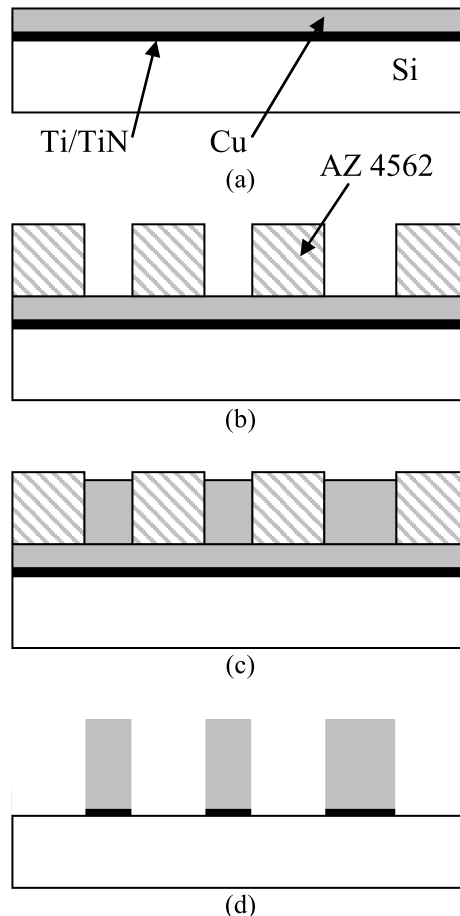

Fig. 3. Fabrication steps for the single mask High aspect ratio copper electroplated structures.

The flow starts with the sputtering of a Copper (Cu) seed layer for electroplating as shown in Fig. 3 (a). However, a thin layer of Ti/TiN is sputtered beneath Cu to prevent diffusion into silicon and to provide good adhesion to the substrate. Then a thick photoresist layer (AZ4562) is spin coated on the wafer at low speed [Fig. 3 (b)]. The low speed used causes wide and high edge bead, which has to be removed for good exposure resolution. It is also important that baking process should be longer to ensure complete baking. Then the wafer is exposed and developed. After development the wall profile is not a 90° straight wall. It is curved and tilted as seen in the SEM picture in Fig. 4. After the preparation of the photoresist mold, Copper is deposited using electroplating [Fig. 3 (c)]. Then photoresist is cleaned from the surface with acetone. The Cu seed layer on the open surfaces is cleaned with copper etching solution, and Ti/TiN is cleaned with 30%H_2O_2 at 60^oC. Copper etching solution

etches the electroplated copper structures faster than the sputtered seed layer, therefore electroplating thickness and width should be adjusted to compensate for this loss. The Ti/TiN etching solution does not create such a problem.

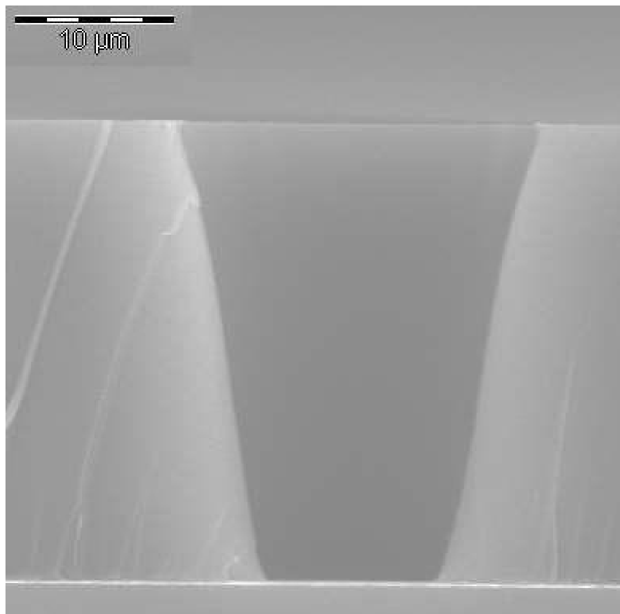

Fig. 4. Cross-Section SEM image of the AZ4562 layer after exposure and development

IV. Measurement

Fabricated transmission lines are measured with a HP8510C network analyzer on a probe station with GSG probes of 100 μm pitch size. Since the designed line widths do not match the pitch size, a tapered section is added for outside connection as seen in Fig. 5. De-embedding structures for these tapers are also added [7].

Measured attenuation values for the transmission lines fabricated on HRS substrate are given in Fig. 6. The spikes around 17 and 33 GHz are due to the resonance behavior of the lines, where measured S11 has very low values.

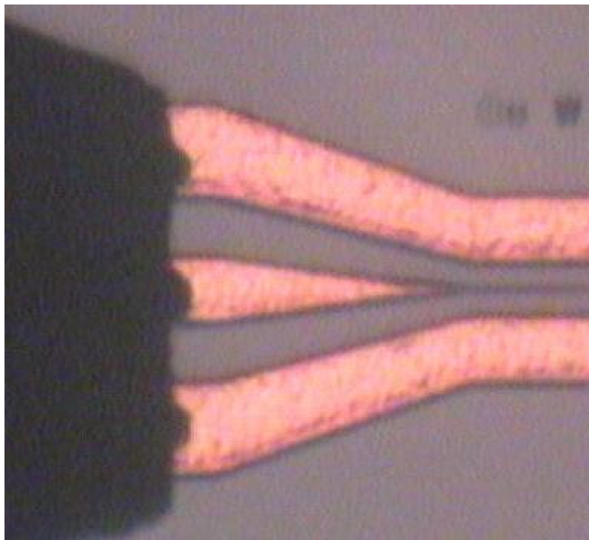

Fig. 5. Picture of the tapering section for the outside connectivity. Taken while measuring by a GSG 100 probe.

Same layout is also fabricated on glass substrate. Results are given in Fig. 7.

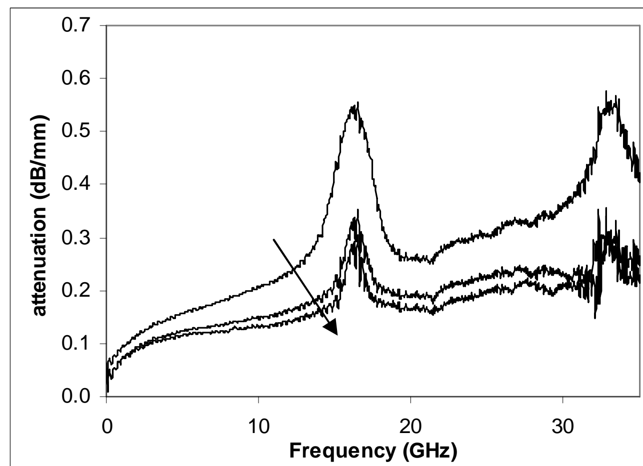

Fig. 6. Measurement results for HAR Cu CPW lines fabricated on HRS substrate. Arrow direction shows the increasing signal width 5, 10, an 15 μm respectively.

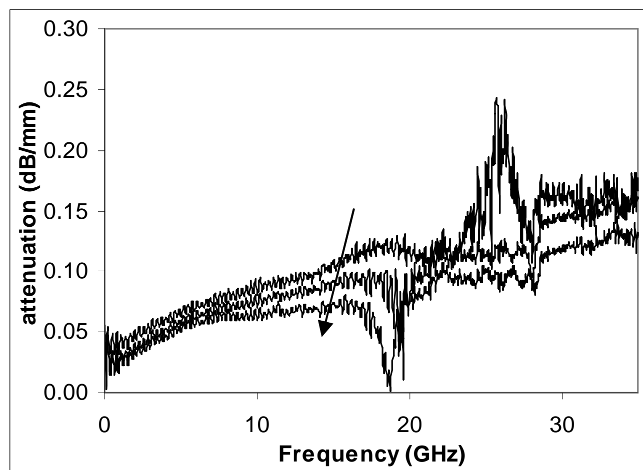

Fig. 7. Measurement results for HAR Cu CPW lines fabricated on glass substrate. Arrow direction shows the increasing signal width 5, 10, and 15 μm respectively.

V. Discussion

Attenuation of the measured lines on HRS, which is the most important setback in narrowing down the CPW lines, has a fairly low value as can be seen in Fig. 6. It is even lower in the case of a glass substrate. In Table I we compare the attenuation values obtained with those reported in previous works [3-6]. The results obtained with the narrow CPW structures built using the HAR process are comparable with those of conventional CPWs with very wide signal lines. The HAR process enables the designer to reduce the width of the lines by roughly 60%, without compromising the performance.

TABLE I
UNITS FOR MAGNETIC PROPERTIES

Substr	S	W	t	α 10GHz	α 20GHz	α 30GHz	ref
GaAs	88	16	1	0.15	0.18	0.21	[3]
Air	250	25	1.2	0.05	0.05	0.06	[4]
Air	190	55	1.2	0.02	0.02	0.03	[4]
HRS	50	25	4	0.13	0.15	0.17	[5]
HRS	45	22.5	1	0.19	0.24	0.29	[6]
HRS	10	20	14	0.15	0.19	0.24	-
Glass	10	20	11	0.07	0.09	0.14	-

S is the signal line width, W is the spacing between signal and ground, t is the thickness of metallization. All three properties are given in micrometers. α is the attenuation of the line in (dB/mm)

VI. CONCLUSION

High aspect ratio copper plating process is a simple process that can be applied as a post process module for RF ICs. Its application to CPW line implementation yields a low attenuation, which enables the design of narrow transmission lines. The experimental results obtained demonstrate that a lateral size reduction of 60% can be achieved, while maintaining the loss at a level comparable to those of conventional CPWs built using very wide lines.

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