

Wideband CMOS Low Noise Amplifier including an Active Balun

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Abstract — An inductorless LNA with active balun is proposed for multi-standard radio applications between 100MHz and 6GHz [1]. It exploits a combination of a common-gate (CG) stage and an common-source (CS) stage with replica biasing to maximize balanced operation, while simultaneously canceling the noise and distortion of the CG-stage. In this way, a Noise Figure (NF) close to or below 3dB can be achieved, while good linearity is possible if the CS-stage is carefully optimized. Moreover, good output balancing can be achieved. The best performance is achieved between 300MHz to 3.5GHz with gain and phase errors below 0.3dB and ± 2 degrees, 15dB gain, $S_{11} < -14$ dB, IIP3 = 0dBm IIP2 higher than +20dBm at a total power consumption of 21mW. The circuit is fabricated in a baseline 65nm CMOS process, with an active area of only 0.01mm². The circuit simultaneously achieves impedance matching, noise canceling, distortion canceling and a well balanced output.

I. INTRODUCTION

Upcoming software-defined and multi-standard radio architectures demand wideband LNAs [2]. In contrast to a multi-LNA solution, a wideband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single-ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip baluns with low losses are typically narrowband so that several baluns would be required in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly.

Combining the balun and LNA functionality into a single integrated circuit is an attractive option to realize a wideband low noise receiver front-end. Only a few wideband LNA-balun combinations with sufficient low noise figure for multi-band receivers have been published [2-4]. These circuits all exploit the noise canceling topology published in [5, Fig. 4b]. Although these circuits have a single-ended input and differential output, the (im)balance of the output signal is not reported. Furthermore, the circuit in [2, Fig. 8a] inherently has a gain difference between its two paths, leading to an unbalanced output signal. Both paths use an equal load resistor (R_L), however, the transconductance (g_m) differs more than a factor of 2, leading to a gain difference ($\Delta g_m \cdot R_L$) of at

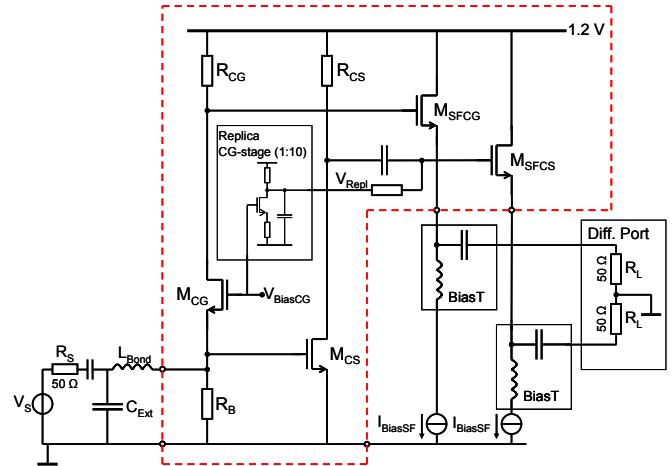


Figure 1. Schematic of the Inductorless Wideband Balun-LNA; the circuit within dashed box is integrated on chip.

least 6dB. Next to this, the circuits in [2-4] all use integrated inductors. As in newer CMOS technologies the area-costs increase, area-consuming integrated inductors become increasingly expensive. Thus, for CMOS processes an inductorless implementation is strongly preferred.

This paper presents the Balun-LNA published in [1] and details how distortion canceling can be exploited to obtain high linearity. The Balun-LNA features high linearity, low-noise and a well balanced output signal. The wideband circuit is designed in a baseline 65nm CMOS process with a 1.2V supply voltage, aiming for high linearity. The circuit is described in section II. Section III shows how noise canceling of the input transistor noise and a balanced output signal can be obtained simultaneously, using the Noise Canceling Technique. Section IV demonstrates that distortion cancelling is also possible, and shows how this can be exploited to achieve good second order linearity. V gives the measurement results. Finally the conclusions are drawn in Section VI.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the balun-LNA circuit based on the topology proposed, but not implemented on silicon, in [5]. The circuit inside the dashed box is implemented on silicon. The input signal is amplified via two paths, a non-inverting Common Gate (CG) path and an inverting Common Source (CS) path. The voltage gains of these two paths are designed to be equal, giving the balun function. The outputs of both amplifier paths are buffered by identical source-followers, both having 50Ω

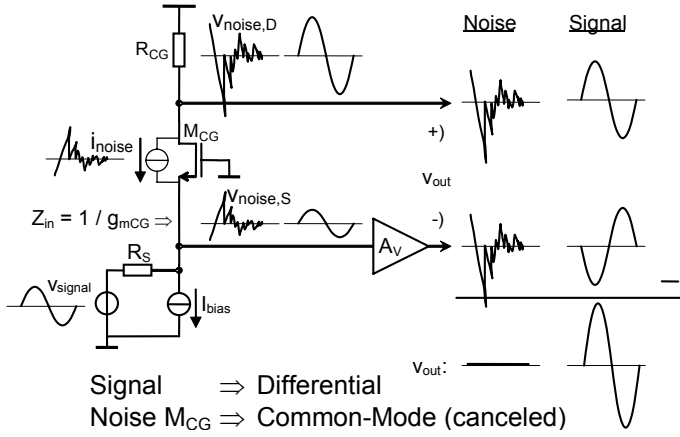


Figure 2. The Noise Canceling Technique applied to a CG-stage.

output impedance. The source-followers are currently used as measurement buffers; in a complete receiver design they can drive a mixer. To maximize balanced operation, the DC-levels at the gates of the source followers are chosen equal. This is achieved by AC-coupling the output of the CS-stage to its source-follower and generating the DC-level (V_{Repl}) by a scaled-replica of the CG-stage. The cut-off frequency of the AC-coupling is designed to be at 10MHz. This is more than a decade below the intended operation frequency, which keeps the error in phase difference of the two paths within a few degrees of 180° .

The CG-stage inherently gives a broadband input match. The real part of the input impedance of the LNA is mainly set by $1/g_{mCG}$ of transistor M_{CG} in parallel with resistor R_B . When the input impedance is matched to the source impedance ($g_{mCG} \approx 1/R_S$, for $R_B \gg R_S$), the noise of M_{CG} is the dominant factor in NF. Without taking any measures its noise would set the lower limit of the Noise Figure (NF) to $\sim 4\text{dB}$. However, by applying the Noise Canceling Technique [5], the noise of the CG-transistor can be canceled at the differential output. This Noise Canceling Technique is explained briefly in the next section.

Since the noise of M_{CG} can be canceled, the noise of M_{CS} remains. However, here the transconductance (g_{mCS}) can be chosen larger than $1/R_S$ while the input match is still performed by M_{CG} . The transconductance of M_{CS} (g_{mCS}) is chosen 5 times higher than g_{mCG} to limit its noise contribution. The resistor R_B acts as a current source and is chosen 7 times higher than R_S , thereby limiting its noise contribution.

III. SIMULTANEOUS NOISE CANCELING AND BALANCING

In this paper we dimension the CG-CS topology in such a way that simultaneous impedance matching, noise canceling and a balanced output signal are obtained. A balanced output requires the gains of the two paths to be equal.

Fig. 2 shows a simplified schematic of the circuit. The voltage amplifier (A_V) represents the CS-stage (M_{CS} and R_{CS}) of Fig. 1 and R_B is replaced by an ideal current source (I_{bias}). The noise generated by M_{CG} can be represented by a current source (i_{noise}). This current generates a voltage at the source-

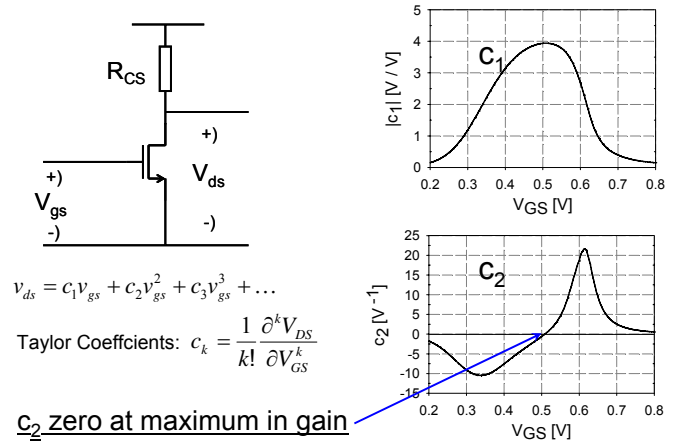


Figure 3. No second order distortion in CS-stage at gain maximum.

node of M_{CG} ($v_{S,noise} = \alpha \cdot i_{noise} \cdot R_S$) and a fully correlated voltage at its drain ($v_{D,noise} = -\alpha \cdot i_{noise} \cdot R_{CG}$) in anti-phase. The factor α depends on the CG-transconductance (g_{mCG}) and R_S : $\alpha = 1 / (1 + g_{mCG} \cdot R_S)$. The noise of M_{CG} can be canceled when it becomes a common-mode signal at the differential output (v_{out}). Therefore, the gain of the CS-stage should be equal to: $A_V = v_{D,noise} / v_{S,noise} = -R_{CG} / R_S$. In order to match to the source impedance, the CG-transconductance should be equal to: $g_{mCG} = 1/R_S$. The required gain of the CS-stage can be rewritten as: $A_V = -g_{mCG} \cdot R_{CG}$, this equals the gain of the CG-stage, except for the inversion. Thus, at the output (v_{out}), the signal is fully differential (well balanced) and the noise of M_{CG} is common-mode signal, which is canceled when taking the differential output.

IV. EXPLOITING DISTORTION CANCELING

As derived in [5], not only the noise of the CG-device can be cancelled, but also its non-linearity. This becomes clear when realizing that both the noise and the non-linearity of a transistor can be modeled as a current source between its drain and source. Using the noise canceling technique the transfer of these current sources to the (differential) output are zeroed and simultaneous noise and distortion canceling is obtained. As the distortion due to the CG-transistor is canceled, the remaining source of non-linearity is the CS-transistor.

The 2nd order distortion of the CS-stage is low when it is biased around its gain maximum. Fig. 3 shows the CS-stage together with the non-linear relation of drain-source (v_{ds}) and gate-source (v_{gs}) voltage. On the right hand side of Fig. 3 the gain ($|c_1|$) of the CS-stage versus V_{GS} is plotted (note: V_{GS} is the DC-bias value). The 2nd order Taylor coefficient (c_2) represents the amount of 2nd order distortion and is also shown in Fig. 3. This coefficient (c_2) is zero at the maximum in gain, as it is proportional to the derivative of c_1 . This explains that the CS-stage has low 2nd order distortion when it is biased close to its maximum in gain.

Fig. 4 shows IIP2 and IIP3 of the CS-stage versus the DC-value of V_{GS} . The peak in IIP2 at the gain-maximum ($V_{GS} = 0.5\text{V}$) is clearly visible. An IIP2 of more than $+20\text{dBm}$ can be

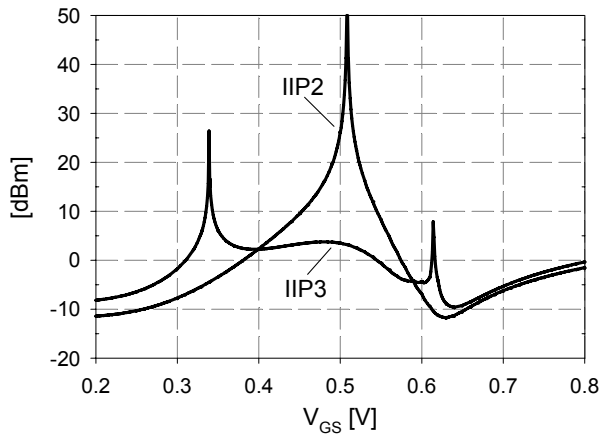


Figure 4. IIP2 and IIP3 of the CS-stage plotted versus V_{GS} .

achieved in a reasonable range of V_{GS} . In this range the IIP3 is larger than +2dBm.

The complete CG-CS circuit can thus be designed to have low distortion as the distortion of the CG-stage is canceled and the distortion of the CS-stage is low.

IV. MEASUREMENTS

The LNA, which has an active area of only $110\mu\text{m} \times 80\mu\text{m}$, has been fabricated in a baseline 65nm CMOS process and is mounted on a PCB. The in- and outputs are bonded, the supply and bias are applied using a probe, see Fig. 5.

A. Gain, Input-match and Isolation

Fig. 6 shows the measured single-ended input to differential output S-parameter gain, S_{ds21} . This parameter characterizes the gain of the LNA using a 50Ω single-ended input port and a 100Ω differential output port. In practical use, the LNA will usually be followed by an on-chip mixer with a voltage-type input, and matching to 50Ω at the outputs is not needed. The most meaningful gain parameter is then the (unloaded) voltage gain. To convert S_{ds21} into voltage gain, 6dB needs to be added to account for the voltage-halving at the matched output, and an additional 3dB to take the conversion from

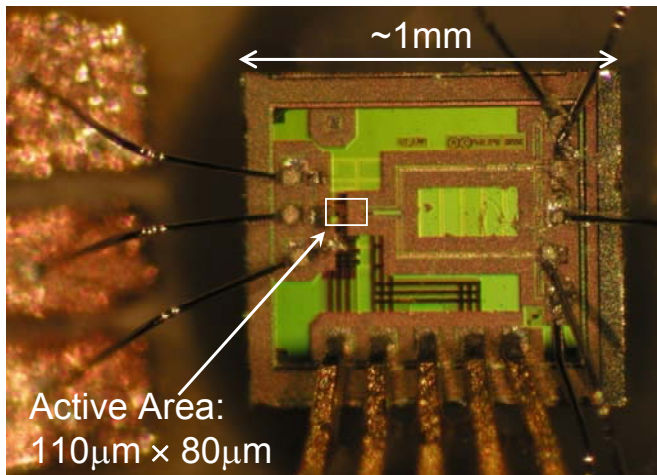


Figure 5. Die photo of the bonded Wideband Balun-LNA.

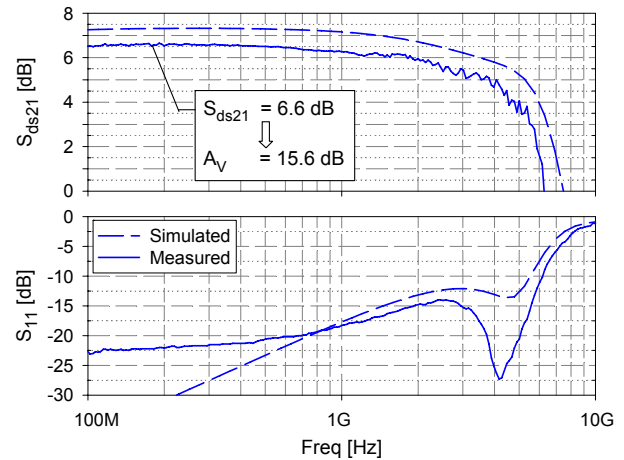


Figure 6. Simulated and measured S-parameters, S_{ds21} (Gain: single-ended in, differential out) and S_{11}

50Ω input to 100Ω output into account. Thus, the voltage gain is within $15.1\text{dB} \pm 0.5\text{dB}$ from 100MHz up to 2.5GHz. The 3dB bandwidth is 5.2GHz. Fig. 6 shows that S_{11} is below -10dB up to 6.2GHz. The resonance of the input bondwire inductance ($\sim 1\text{nH}$) and an external capacitor (600fF) broadens the input match with a few GHz.

The common and differential output to single-ended input isolations (S_{sc12} and S_{sd12}) are better than -30dB and -40dB respectively.

B. Noise Figure

Fig. 7 shows that the measured Noise Figure (NF) is below 3.5dB from 0.2 to 5.2GHz and below 4dB from 0.1 to 6GHz. An advantageous property of the Noise Canceling technique is that the power and noise matching can be obtained simultaneously [5]. The simulated NF equals the simulated NF_{\min} over a large bandwidth and only starts to deviate at higher frequencies due to the increasing impedance mismatch at the input. The increase of NF_{\min} at low frequencies is due to $1/f$ -noise, the increase at high frequencies is due to the drop in gain.

C. Gain and Phase Imbalance

The balun performance was characterized on 20 samples at nominal bias conditions, equal to the simulation conditions.

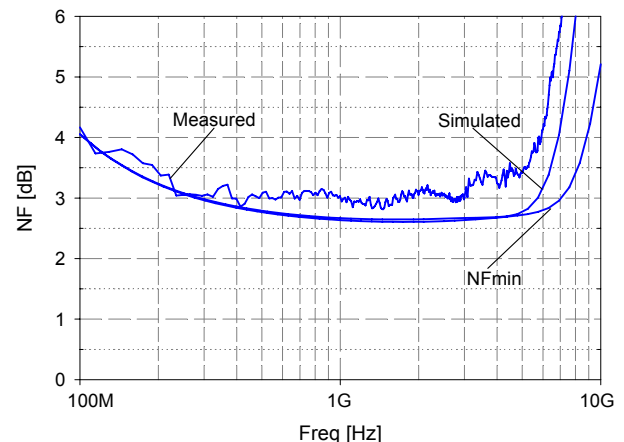


Figure 7. Measured Noise Figure, simulated NF and NF_{\min} .

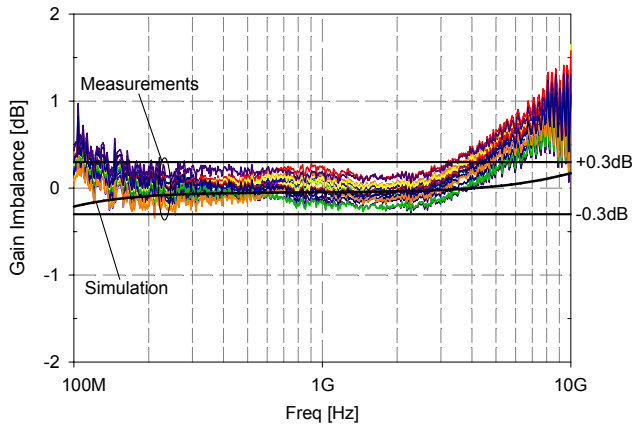


Figure 8. Gain imbalance, simulated and measured (20 samples).

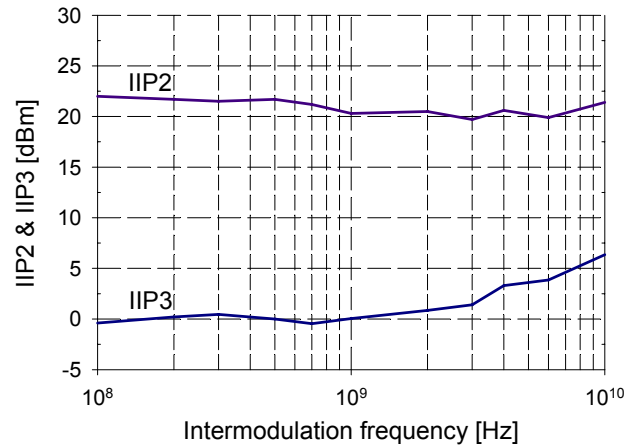


Figure 10. Measured IIP2 and IIP3 versus intermodulation frequency.

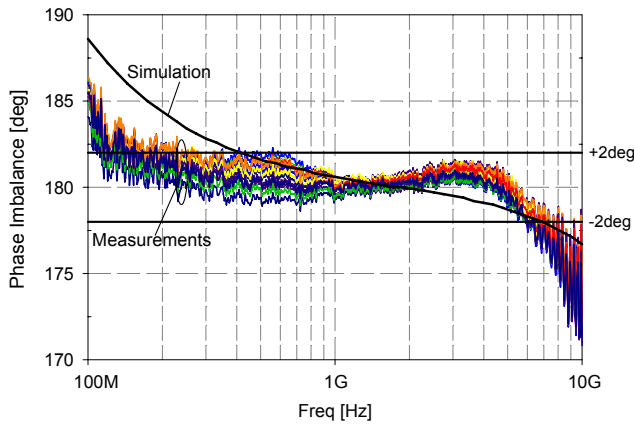


Figure 9. Phase imbalance, simulated and measured (20 samples).

These measurements were performed using wafer-probing. The gain and phase imbalance measurements are shown in Figures 8 and 9. In the band from 300MHz to 3.5GHz the gain imbalance is smaller than ± 0.3 dB and the phase imbalance remains within ± 2 degrees. The somewhat larger spread in phase difference in the 300–800MHz range is caused by a resonance-effect in the output cables and non-optimal probe contacting. If desired, fine tuning of the balun functionality is possible, e.g. via the bias of the CS or GS stage or via the bulk of the CG transistor.

D. Linearity

Wideband standards like WiMedia-UWB and DVB-H require wideband RF-frontends with high linearity. For 2nd

order distortion, a narrowband receiver is only sensitive to the effects of an interfering modulated carrier which leaks through the mixer, corrupting the signal at the mixer output. Next to this effect, a wideband receiver also has to deal with interferers that have sum or difference frequencies equal to the wanted signal frequency, corrupting the signal already in the LNA. Analysis of interferer scenarios for two wideband standards, WiMedia-UWB and DVB-H, show that the required IIP2 of the LNA is in the order of +20dBm.

Fig. 10 plots the measured 2nd order and 3rd order intercept points versus the frequency of one of the intermodulation tones. To determine the IIP2, one fixed 900MHz tone (e.g. GSM) is used, whereas another input tone is swept in frequency. For intermodulation frequencies below 900MHz the difference frequency is taken, for frequencies above 900MHz the sum frequency is taken as the intermodulation frequency.

The IIP3 is determined using two closely spaced tones and is around 0dBm. The increase in IIP3 with frequency can be explained by the increasing impedance mismatch at the input. The reason for the high IIP2 obtained (higher than +20dBm over the full 100M–10GHz range) is explained in Section IV. The effects of non-linear transistor capacitances are not dominant as the circuit is designed for wideband operation, by keeping the capacitances small compared to the load resistors (R_{CG} and R_{CS}). The spread of IIP2 was measured on 20 samples, while keeping the biasing fixed. The worst-case was found to be +18dBm while other samples showed an IIP2 as high as +34dBm.

TABLE I. COMPARISON OF BALUN-LNAs, PASSIVE BALUNS AND INDUCTORLESS SINGLE-ENDED LNAs.

Ref	Freq. Band [GHz]	NF [dB]	Gain A_v [dB]	IIP2 [dBm]	IIP3 [dBm]	Pdiss (core) [mW]	Proc. ²⁾ V_{supply}	# coils area [mm ²]	Balun?	Gain imbal. [dB]	Phase imbal. [deg]
This Work	0.2 – 5.2	< 3.5	13 – 15.6	> +20	> 0	21 (14)	65nm 1.2V	– 0.009	YES	< 0.3	< 2
[2] JSSC 2006	0.8 – 6	<3.5	18 – 20	?	>-3.5	12.5	90nm 2.5V	2 ?	YES	> 6 ³⁾	?
[3] CICC 2005	0.9 – 5	< 3.5	18 – 19	+4 (sim)	+1 (sim)	12	0.18μm 1.8V	4 ~0.4	YES	?	?
[4] RFIC 2005	2.7 – 4.5	< 5	18 – 19.6	?	-8	16.2 (12.6)	90nm 1.2V	1 0.2	YES	?	?
[6] MTT-S 2005	0.8 – 2.5	< 4 ¹⁾	$S_{ds21} \approx -4$	high	high	passive balun	0.18μm –	2 0.073	YES	< 0.4	< 3.2
[7] MTT-S 2005	1.5 – 3.5	< 1 ¹⁾	$S_{ds21} \approx -1$	high	high	passive balun	GaAs –	6 0.42	YES	< 1.3	< 4
[5] JSSC 2004	0.2 – 2.0	< 2.4	10 – 14	+12	0	35	0.25μm 2.5V	– 0.075	NO	N/A	N/A
[8] ISSCC 2006	0.5 – 8.2	< 2.6	22 – 25	?	-4 / -16	42	90nm 2.7V	– 0.025	NO	N/A	N/A

¹⁾ Insertion Loss ²⁾ CMOS unless specified differently ³⁾ As derived from component values in schematic

VII. CONCLUSIONS

Table I shows a comparison of the balun-LNA to three other wideband CMOS active baluns [2-4], two passive baluns implemented in CMOS [6] and GaAs [7] and two wideband inductorless single-ended LNAs [5,8]. The proposed balun-LNA is more wideband than the passive integrated baluns [6,7] while showing smaller gain and phase imbalances. The LNA performance of the implemented circuit is competitive to non-balun LNAs [5] and [8]. The circuit is integrated in a digital baseline 65nm process using a 1.2V supply voltage. Still, at this low supply voltage, it achieves high linearity by exploiting distortion canceling and optimizing the CS-stage for high linearity. The active area is small, as no integrated inductors are required. In contrast to [2] the balun-LNA presented in this work simultaneously achieves impedance matching, noise canceling and a well balanced output.

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