

Slow-wave Differential Interconnect for 40Gb/s IC Design

Michael T. Reiha and John R. Long

ERL / DIMES, Delft University of Technology, 2628 CD Delft

Abstract — A slow-wave differential interconnect is designed and simulated in a low-ohmic silicon process. Design issues related to interconnects for high-speed architectures (e.g., 40Gb/s) include achieving low-loss ($< 1\text{dB/mm}$) and low phase-velocity variation (i.e., group delay $< 10\%$) over a bandwidth of at least 70% of the 40 Gb/s bit-rate. Phase distortion is of particular importance in high bit-rate receivers as it primarily affects intersymbol interference and bit-error rate. The slow-wave structure exhibits lower attenuation in the differential mode and its mechanisms are controlled primarily by back-end-of-line passivation layers as well as minimum line-spacing

Index Terms — OC-768, Slow-wave Interconnect.

I. INTRODUCTION

Foreseeable consumer demand for broadband services such as 4G wireless systems will flood backend optical networks with an increase in data traffic. These networks will be forced to operate at higher speeds in order to support multimedia tributaries such as 4G handsets. Optical networks will expand in infrastructure, requiring more electro-optical interface equipment at a lesser cost, while next generation optical systems like SONET OC-768 will attempt to stem the influx of traffic at channel data transfer rates in excess of 40 Gb/s. However, improvements introduced by OC-768 will have to scale in tandem with the cost of network exhaustive user devices. In other words, cost-effective Si-based technologies should be further utilized in the realization of high-yield and highly-reliable OC-768 chipsets. This poses a formidable design task for any technology, as fibre system capacity is incriminated by a factor of four every 3-5 years generation (current systems operate at 10 Gb/s while the fibre capacity is in the THz range).

A differential interconnect is a circuit element that is typically integrated in high-speed circuits that utilize distributed delay-lines (e.g., distributed amplifiers). The benefits of using differential interconnects include minimizing band-limiting parasitic effects induced by lossy (i.e. low-ohmic) silicon substrates as well supporting fully-differential circuits that inherently improve common-mode rejection.

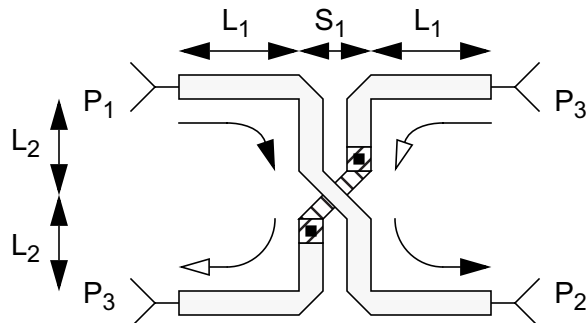


Fig. 1. 4-port section of the proposed slow-wave differential interconnect.

tion. However, conventional differential interconnects (such as coupled-pair lines) achieve time (or phase) delay at the expense of larger silicon area (compared to uncoupled lines) because of its inherent negative magnetic coupling. Compromising delay with area limits IC design to designing lower-power distributed circuits for adequate yield and reliability. In spite of this shortcoming, current deep submicron BiCMOS technologies possess gain bandwidth products between 100-200GHz, lending itself as a potential candidate for concurrent high-speed, high output power circuits (such as modulator driver design), prompting the need for a novel, high-speed interconnect solution.

In this paper, a slow-wave differential interconnect implemented in a commercial $0.13\mu\text{m}$ BiCMOS technology is designed for SONET OC-768, where bit-rates use bandwidth in excess of 40GHz. Design issues associated with differential interconnects include concurrently achieving a low-loss (i.e., minimum attenuation), compact form-factor (i.e., minimum silicon area) that boasts sufficient bandwidth for 40Gb/s (at least 70% of the bit-rate). The interconnect group delay requires a variation $< 10\%$ of the bit-period over the specified bandwidth in order to minimize inter-symbol interference (ISI) and jitter [1]. Both group delay and form factor requirements are achieved by using a differential structure that supports slow-wave propagation under odd-mode excitation. Slow-wave propagation using sili-

con-based interconnects has been shown to reduce signal attenuation, enabling a low-loss interconnect solution at higher frequencies [2]. The phase-velocity in the slow-wave structure is less than 1/5 of the phase velocity characterized using conventional coupled lines, lending itself as a compact interconnect solution for high-speed, high output power circuits such as the modulator driver.

II. SLOW-WAVE INTERCONNECT DESIGN

The proposed slow-wave interconnect (seen in Fig. 1) shows a pair of microstrip lines used to transport incidental wave propagation from the input (P1,P3) to the output (P2,P4). The slow-wave phenomena is exploited by the positive mutual magnetic coupling between the input and output ports via the closely spaced conductors. A simplified electrical model of the interconnect is shown in Fig. 2.

Self-inductance L_1 is used to separate any parasitic coupling between adjacent slow-wave coupled lines. The amount of slow-wave coupling is controlled primarily by the self-inductance L_2 and the magnetic coupling coefficient k_1 . In other words, by using a larger line-line separation (lowered k_1), inductance L_2 (i.e., the length of interconnect) would need to be increased to keep the slow-wave propagation factor constant. However, the secondary effects of using a lower magnetic coupling are two-fold. First, the lengthened line introduces more series resistance (i.e., metal-loss due to skin and proximity effects). The frequency dependence associated with this metal-loss becomes difficult to model in an equivalent RLC circuit (especially at frequencies above 30GHz). Second, the lowered interwinding capacitance C_w as a result of the increased line-spacings results in increase of electric field distribution penetrating closer to the frequency-dependant lossy silicon substrate which is also difficult to model at higher frequencies (i.e., analogous to the metal loss mechanisms).

It is paramount to use minimum spacing (determined by the technology) between the slow-wave coupled lines (i.e., maximum k_1). In such a design, the attenuation will be lower (in magnitude) and less frequency dependant (i.e., less influenced by the lossy substrate at frequencies > 30GHz). The amount of inductance L_1 and L_2 is an intricate balance between desired differential characteristic impedance (i.e., 50Ω), time-delay per section and bandwidth (i.e., > 40GHz). For example, increasing either L_1 or L_2 will lower the Bragg limit (cut-off fre-

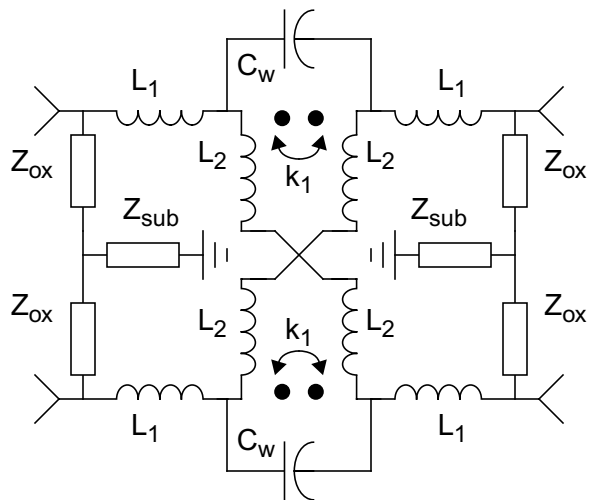


Fig. 2. Simplified electrical circuit of the slow-wave interconnect.

quency of the transmission line), but not having enough inductance L_1 will make a low-ohmic characteristic impedance (i.e., 50Ω) difficult to achieve and also allow parasitic coupling with other slow-wave coupled stages.

III. SIMULATION RESULTS

A compact slow-wave interconnect section was simulated using the ADS Momentum simulator. The dielectric stack-up is specified in Table I.

TABLE I: DIELECTRIC STACK

Dielectric	Thickness (μm)	Relative Permittivity
Air	300	1
Polymide	2.5	9.5
SiO ₂	12	4
Si Substrate	300	12

In addition to the dielectric stack, two aluminum metals with respective thickness' of 4μm and 1.5μm were used to construct the interconnect section. The interconnect uses equal dimensions (see Fig. 1) of 100μm for L_1 and L_2 . Spacing S_1 is set to 4μm in order to give an aspect ratio of 1 (i.e., considering the thickness of the top-conductor metal).

Three simulation cases were performed through a series of parameter extractions (e.g., even/odd-mode attenuation, eve/odd-mode characteristic impedance). The first case uses an interconnect with no shielding from the

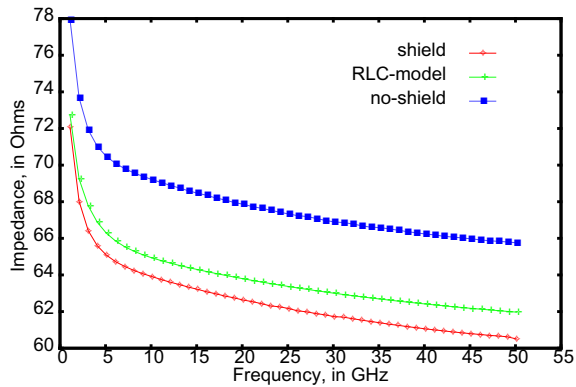


Fig. 3. Simulated even-mode characteristic impedance

lossy substrate. The second case depicts a simulated interconnect with a floating strip shield as described in [2]. The contrast between shielded and non-shielded simulations is used to identify enhancements (or impairments) of the shield use. The S-parameters of the shielded interconnect was then extracted into an equivalent *RLC* network for the third simulation. The extraction tool is a graphical, interactive program called SiMBIX which was developed at the TU Delft Electronics Laboratory in an effort to model broadband interconnects for both time (i.e., transient) and frequency domains.

The even-mode characteristic impedance is shown in Fig. 3. Both the shielded and extracted networks are within agreement while the non-shielded structure exhibits slightly higher impedance over all frequencies.

In contrast, the odd-mode characteristic impedance shown in Fig. 4, shows less variation over the 50GHz frequency range. Interestingly, the *RLC* network is a closer fit to the non-shielded structure. However, this

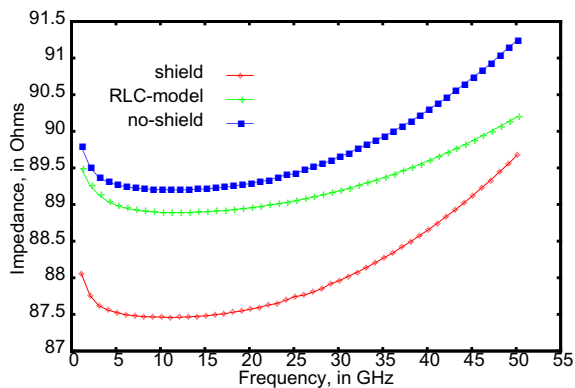


Fig. 4. Simulated odd-mode characteristic impedance.

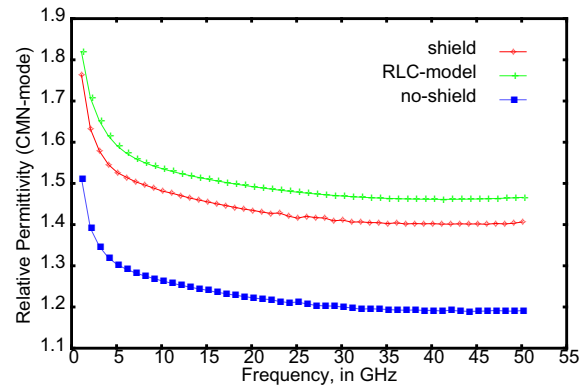


Fig. 5. Simulated even-mode relative permittivity.

could be classified as an anomaly considering the shielded and non-shielded structures are in relative agreement with each other. In other words, the floating shield has little impact in varying the odd-mode characteristic impedance.

The even-mode relative permittivity (hence, wave propagation speed) is shown in Fig. 5. Again, the *RLC* network closely mimics the shielded results. In addition, the non-shielded case exhibits a faster wave-speed than the shielded case, but only slightly. Comparatively, the true nature of the interconnect is shown in Fig. 6. The effective relative permittivity is between 33-35 at lower frequencies. Given that the relative permittivity used in the dielectric stack are low in value, it can be assumed that the reduction in speed is due to the concurrent mutual magnetic coupling and the high interwinding capacitance. Furthermore, the slow-wave is broadband in nature (i.e., < 10% variation of 50GHz) but loses this property at higher frequencies. This is understood by considering the slow-wave factor as a product, similar

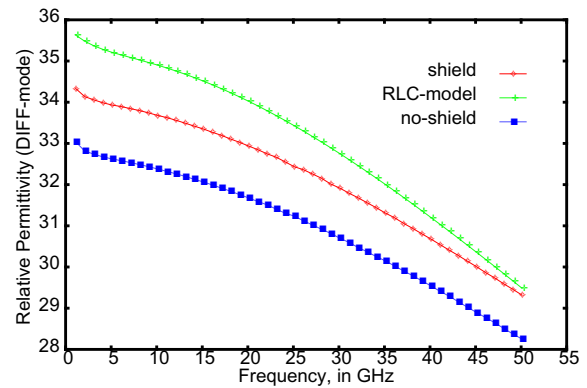


Fig. 6. Simulated odd-mode relative permittivity.

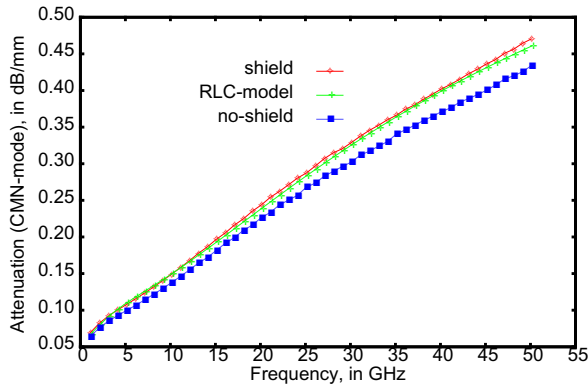


Fig. 7. Simulated even-mode attenuation.

to the gain-bandwidth product used to merit RF amplifier design. That is, to achieve a slower wave speed, the Bragg frequency (hence, usable bandwidth) must be reduced (i.e., for that particular mode). The intrinsic achievable slow-wave factor is therefore a function of the interwinding capacitance and magnetic coupling. Since commercial silicon technologies mainly differ in the top-metal thickness (hence, minimum allowable line-spacing and magnetic coupling factor), the slow-wave capability of a particular process is controlled by the back-end-of-line process steps (i.e., passivation layers and thickness’).

The even-mode attenuation (Fig. 7) increases in frequency due to the skin-effect in the metals as well as the substrate mechanisms. Conversely, the odd-mode attenuation is lower in magnitude by approximately 25%. Thus, the added advantage of using this differential interconnect is the reduction in wave speed with a concurrent reduction in attenuation. It should be noted that the reduction in attenuation is variable and can be

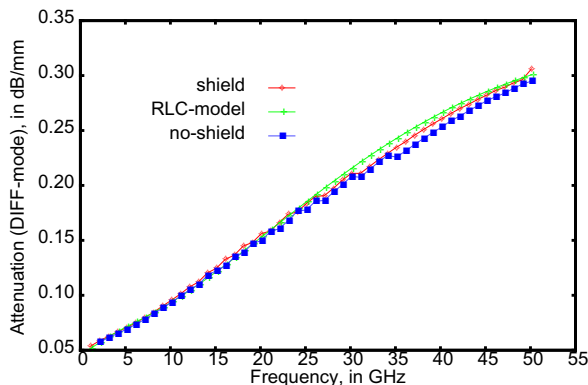


Fig. 8. Simulated odd-mode attenuation.

further reduced by choosing an appropriate line width that has a larger skin-depth in the even-mode than in the odd-mode. It is expected that such a design (e.g., wide line-width) would also contribute more attenuation into the substrate. However, the use of the floating shield would reduce the substrate effects, as shown in [2].

IV. CONCLUSION

In this paper, a slow-wave differential interconnect was simulated in a low-ohmic silicon technology. Shielded and non-shielded structures were compared with an extracted *RLC* network. The reduction in wave speed in the differential mode was shown to be band limited but with less than 10% variation, a possible candidate as a high-speed interconnect in circuits used for 40Gb/s architectures [1]. The differential mode attenuation is reduced in tandem with the speed, allowing for a low-loss, compact-area design element, suitable for distributed amplifiers.

ACKNOWLEDGEMENT

The authors wish to acknowledge the financial support provided by STW contract no. DCS 6422.

REFERENCES

- [1] E. Sackinger, *Broadband Circuits for Optical Fiber Communication*, J. Wiley & Sons, 2005.
- [2] T.S.D. Cheung, J.R. Long “Shielded Passive Devices for silicon-based monolithic microwave and millimeter-wave integrated circuits”, *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1183-1200, May 2006.