

# Encapsulation of a resonating structure using substrate transfer and thin film processes

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*Abstract*— In this paper a novel way of fabricating and sealing MEMS-devices next to the drive and read-out circuitry on a (Bi-)CMOS wafer is proposed. In the process the active wafer is glued to a glass substrate after the wafer has been fully processed (substrate transfer technology). After etching trenches from the backside through the silicon into the fieldoxide the MEMS device will be released in HF. Afterwards the cavity is sealed with a PECVD layer. In this paper the results of a preliminary study of the trench sealing properties of silane based PECVD oxide and nitride layers are also reported.

*Keywords*— MEMS, packaging, substrate transfer

## I. INTRODUCTION

Packaging is a big challenge in the fabrication of MEMS devices, since these devices cannot be packaged directly in a standard plastic or ceramic package as done for ICs. Such packages would alter or even destroy the moving parts of the MEMS device. The MEMS devices have to be packaged in a complex and expensive housing with a cavity under controlled pressure. These packages can contribute up to 70% of the device costs [1].

Alternatively the structure is protected on wafer level scale, which is commonly done by wafer bonding using anodic [2] or eutectic bonding [3]. The pressure and gas composition in the package can be easily adjusted, since bonding can take place either in vacuum or in an inert gas atmosphere. This technology requires relatively large bonding areas on the silicon and has relative high demands to the wafer flatness, which makes an

integration into a standard (Bi-)CMOS process difficult. Another drawback of this method is that vias have to be etched through the top-sealing wafer to contact the device electrically. Wafer bonding is mostly used for stand-alone MEMS devices with the drive and read-out circuitry located on a separate die next to the MEMS device.

Currently the trend goes to 0-level packaging to avoid wafer bonding [4]. In this technology the MEMS-structure is protected by a sacrificial layer (e.g. oxide) followed by a thick capping layer. In a first step holes are etched into the capping layer, then the sacrificial layer is etched through these holes to release the structures. The holes are sealed by a LPCVD or PECVD sealing layer. The pressure in the package is defined by the gas atmosphere during the layer deposition. This technique requires relatively little additional space on the silicon and works even with relatively high topography on the wafer. The capping layer needs to be relatively thick to prevent material be deposited on the moving structures which would alter their properties. For a commercial use of this technique, the deposition has to be done at high temperatures (>500°C) to achieve a sufficient deposition rate, which reduces the compatibility with a (Bi-)CMOS process. To achieve full flexibility in the choice of the atmosphere inside the package a two-step sealing process was proposed, where the sealing of the cavity is done after the layers have been deposited by a reflow process at temperatures above 700°C [5]. High temperature steps could introduce additional stress to the MEMS device that

could alter the device properties or even destroy the device.

From the discussion above the requirement of a package for a combined-MEMS-(Bi-)CMOS devices can be summarized as follows:

- All the additional processes must be low temperature steps (<400°C), not to alter the doping profile of the active devices.
- It must be possible to adjust the pressure in the MEMS-package since different applications may require different pressures (i.e. sensors might require higher damping than RF-filters).
- The package must protect the MEMS device reliably and permanently from the influence of the environment (humidity, dust etc.).
- From a cost perspective the required size for the package on the silicon chip must be minimized. Its thickness should also be minimized since the trend goes to thinner and thinner dies to reduce the size of the electronic devices (PDA, cell phones etc).
- To be feasible for mass production the process must be cheap and compatible with standard IC processing equipment.

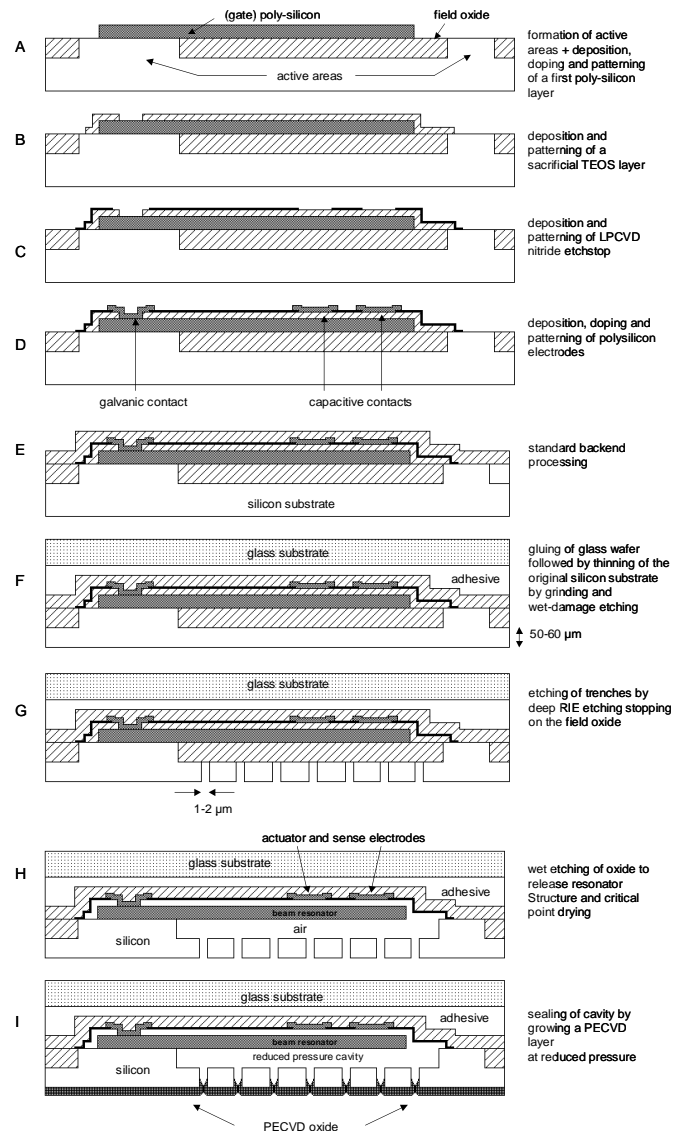
If the MEMS-device is on the same chip as the drive and the read-out circuitry, the additional steps must not interfere with the CMOS processing and alter the characteristics of the electric devices. Negligible influence of the MEMS-processing to the (Bi-)CMOS processing would allow an easy transfer of the MEMS device to different (Bi-)CMOS generations.

The proposed novel process, combining substrate transfer technology [7] and surface micromachining fulfills not only the above requirements for a MEMS package but also adds only two more layers to the backend-of-line processes. The actual release and packaging of the MEMS device will be done after the IC-part is completed and tested, after the wafer is glued to a glass substrate (figure 1).

## II. PROPOSED PROCESS FLOW

In our new approach the MEMS structure itself is defined in the gate-polysilicon layer, on top of the fieldoxide. The fieldoxide acts as sacrificial layer during the release etch. In case the MEMS-device requires a different polysilicon thickness as the gate-polysilicon layer, an additional polysilicon layer can be introduced in the process-flow (figure 1a). After the (Bi-)CMOS-processing is completed, a TEOS-layer (i.e. the first layer of the dielectric stack of the (Bi-)CMOS backend) is deposited on top of the resonator. The TEOS is patterned so that the resonator can be

electrically contacted (figure 1b). The thickness of the TEOS-layer defines the distance between the electrode and the resonator. In the next step an LPCVD-nitride layer is deposited and patterned. The nitride extends over the TEOS and has direct contact to the substrate silicon. This layer acts as etch stop during the release etch. The electrodes are defined by a second thin polysilicon layer. Both of these layers are additional steps compared to a standard (Bi-)CMOS-process flow (figures 1c and 1d). Apart from the release etch the MEMS device is now ready and the standard (Bi-)CMOS metallization can follow. The wafer can also be tested before the release etch of the MEMS device (figure 1e). After the wafer has left the IC-fab, the wafer is glued to a glass substrate, e.g. using an acrylic glue. The wafer sandwich is then grinded back until approximately 50-60 μm silicon remains. A wet



**Figure 1: Proposed process flow to package a MEMS device using substrate transfer and thin film technology**

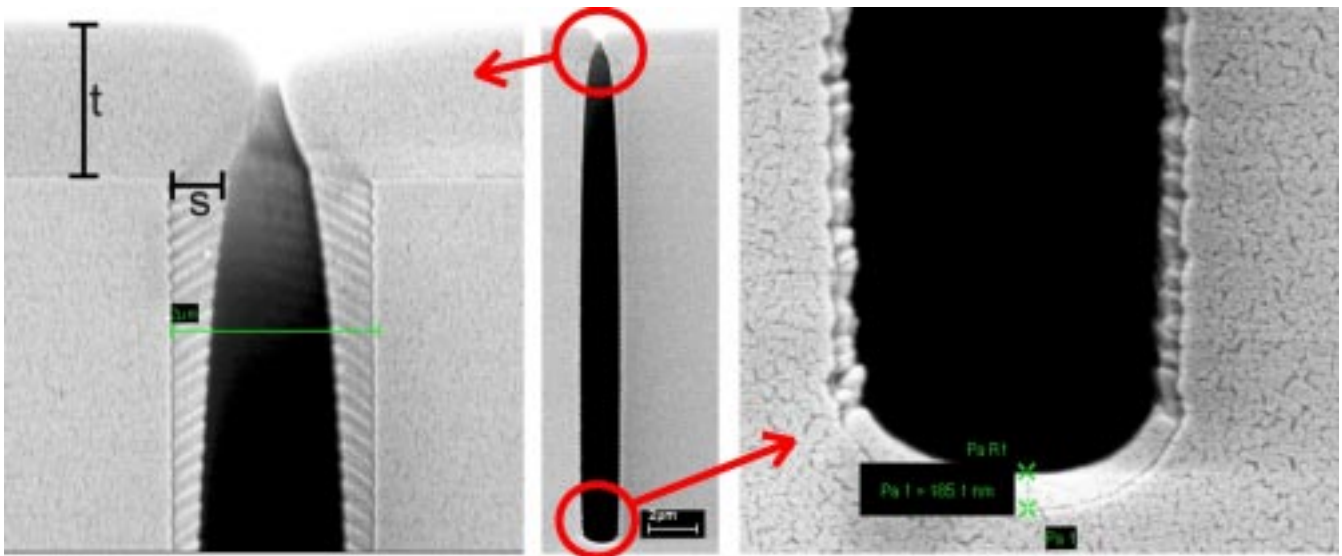


Figure 2: Nitride deposited on top of a 2  $\mu\text{m}$  wide trench with nitride deposited on the bottom of the trench.

chemical stress release etch step follows the grinding (figure 1f). A drawback of the glue used in this process is that it cures by exposition to UV-light, thus glass has to be used as substrate. Due to the low flatness of the glass wafer, it is impossible to thin the wafer sandwich further, with a silicon substrate it would be possible to grind the wafer down to 20-30  $\mu\text{m}$ . Trenches are etched from the backside of the wafer sandwich through the silicon into the fieldoxide (figure 1g). These holes act as etch holes during the following release etch in HF or BOE. To prevent sticking of the resonator to the electrode the structures have to be dried using a critical point dryer. The MEMS structure is now released (figure 1h). The trenches are then sealed by depositing a PECVD layer with a poor step coverage. The structure is encapsulated at the pressure defined by the deposition process (figure 1i). In a final step the bond pads are opened from the backside by etching holes into the silicon.

Table 1 Process parameters for the deposition of the nitride and oxide layers

	Plasmaoxide	Plasmanitride
Pressure:	2,2 Torr	2,2 Torr
Temperature	275 °C	275 °C
SiH <sub>4</sub> flow:	0,205 slm	0,4 slm
N <sub>2</sub> O flow:	6 slm	3,5 slm
N <sub>2</sub> flow:	3,15 slm	1 slm
Power HF:	1000 W	400 W
LF:	0W	600 W

### III. EXPERIMENT

For investigating the sealing properties of different PECVD layers, trenches have been etched into a test wafer using the BOSCH-process on a RIE-STC etching system. The trenches were approximately 20  $\mu\text{m}$  deep and their width varies from 0.75  $\mu\text{m}$  to 3.5  $\mu\text{m}$ . In order to investigate loading effects, the spacing of the trenches was varied between the width of the trenches and 10  $\mu\text{m}$ .

In an initial preliminary study a low-stress nitride and a silane based oxide layer were deposited with a Novellus Concept One PECVD tool at Philips Semiconductor Hamburg on the testwafers. The process parameters are listed in table 1. The only difference to layers used as dielectric layers in the (Bi-)CMOS

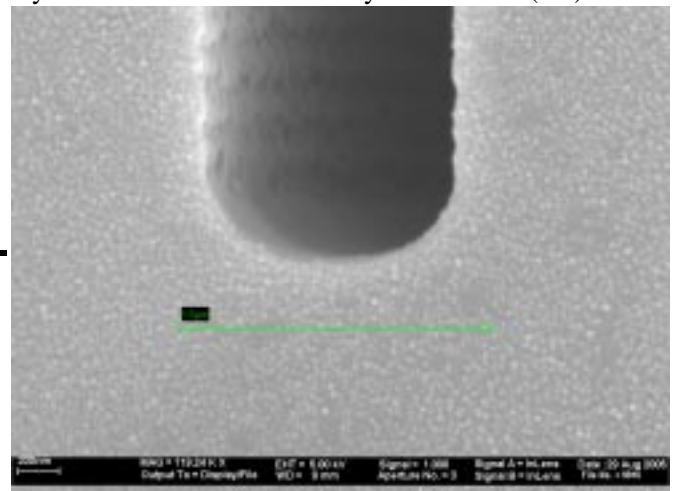
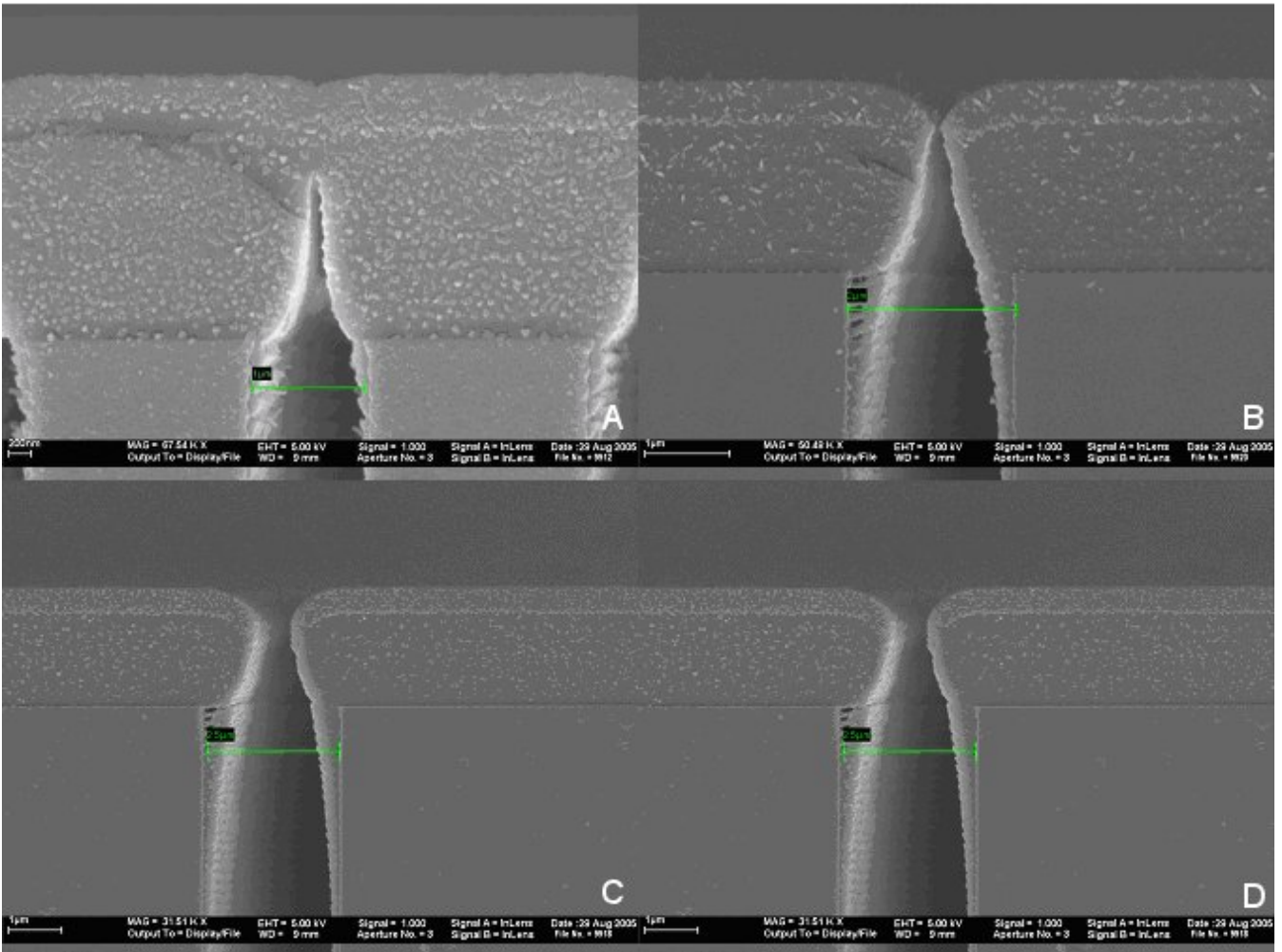


Figure 3 Bottom of a 1.4  $\mu\text{m}$  wide trench having no oxide on the sidewalls after the deposition



**Figure 4: Sealing properties of PECVD silicon oxide on trenches with 1  $\mu\text{m}$  (A), 1.4  $\mu\text{m}$  (B), 1.9  $\mu\text{m}$  (C) and 2.3  $\mu\text{m}$  (D) wide trenches**

backend-of-line process is that the temperature of the heater block (wafer temperature) was reduced from 400°C to 275°C since the acrylic glue used to bond the active wafer to the glass substrate in the substrate transfer process starts to decompose at 310°C. The sidewall coverage of the trenches was studied by investigating the testwafers with a scanning electron microscope (SEM) in cross section. Since the contrast between the silicon of the testwafer and the PECVD layer was not sufficient to see the different layers in the SEM, the samples were etched for 5s in BOE or alternatively for 15s in 5% HF solution. To compare the sealing properties of the different layers the sidewall coverage is defined as the ratio of the material deposited on the side at the very top of the trench (s) to the thickness (t) of the layer on top of the wafer (figure 2).

## IV. RESULTS

### A. Nitride

Due to its good properties as passivation layer and diffusion barrier a silicon nitride layer was first investigated as sealing layer. The deposited layer had a thickness of about 1.5  $\mu\text{m}$  and was able to close trenches with a width of 1  $\mu\text{m}$ . The 1.9  $\mu\text{m}$  wide trenches had a sidewall step coverage (s/t) of approximately 0.4. The nitride layer on the bottom of the trench was 185 nm thick what corresponds to a bottom step coverage of 0.13. It can be seen that the layer on the bottom is thicker than on the sidewall (figure 2). This layer would alter the resonant frequency of the MEMS device. Assuming a 0.5  $\mu\text{m}$  thick polysilicon resonator and a 25% overlap of the resonator with the etch holes, the 185 nm nitride would result in an increase of the mass of the resonator by approximately 12%, that leading to a

shift of the resonant frequency of approximately 6%. Due to stress relaxation at the silicon-nitride interface during the movement of the resonator the quality factor of the device would also be reduced [7]. Therefore the nitride layer appears not be feasible as sealing layer.

### B. Oxide

The deposited layer had a thickness of 1.7  $\mu\text{m}$ . To prevent the etching of the silicon oxide during the dipetch for the SEM preparation, an additional layer of approximately 0.5  $\mu\text{m}$  plasma nitride was deposited on top of the silicon oxide. One of the concerns that arose during the SEM preparation was that the oxide on the sidewall of the trench would be etched very fast by the dip etch due to its high roughness and its missing protective nitride layer. But since no significant underetch at the nitride oxide interface was observed (figure 4c), it can be concluded that the alteration of the oxide layer on the sidewall during the dip etch of the trench can be neglected. Figure 3 shows that at the bottom of the 1.4  $\mu\text{m}$  wide trenches no oxide is deposited, also the deeper sidewall of the trench is free of oxide, which makes the oxide layer feasible to be used to seal the trenches without altering the resonant frequency of the device. Similar to the sealing results with the nitride layers the 1  $\mu\text{m}$  wide trench was completely sealed (figure 4a). It is not quite clear whether the 1.4  $\mu\text{m}$  wide trench is already sealed by the oxide or only by the protective nitride layer (figure 4b). The sidewall step coverage depends apparently on the width of the trench and varies from 0.07 for the 1  $\mu\text{m}$  wide trench to 0.34 for the 2.3  $\mu\text{m}$  wide trench (figure 5). The sidewall step coverage of the oxide layer is approximately 40% lower than the sidewall step coverage of the nitride layer, which is advantageous for the sealing properties of the MEMS device.

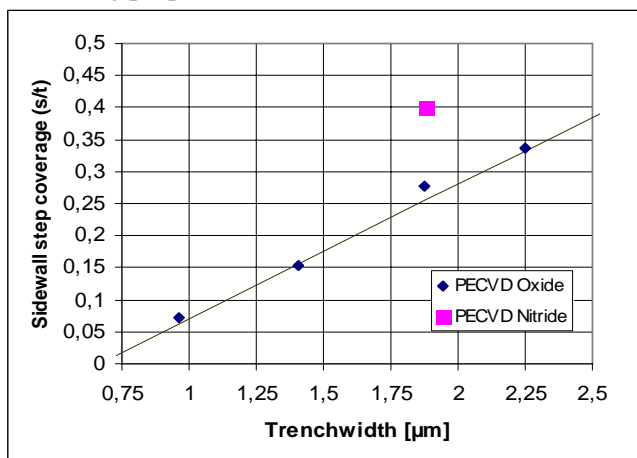


Figure 5 Step coverage as function of the trench width

## V. CONCLUSIONS

A novel way of fabricating and sealing MEMS devices on an standard (Bi-)CMOS wafer has been presented. Silane based PECVD oxide and nitride layers are able to seal 1  $\mu\text{m}$  wide trenches and can therefore be used to seal a cavity for a MEMS resonator. Whereas the sidewall step coverage of the oxide is poor enough that no oxide is deposited on the bottom of the trench, the nitride layer has a step coverage good enough that even in a 20  $\mu\text{m}$  deep trench enough nitride is deposited on the bottom e.g. to significantly alter the resonant frequency of a MEMS resonator. Thus only the oxide layer can be recommended for sealing MEMS devices.

## VI. ACKNOWLEDGEMENT

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## VII. REFERENCES

- [1] V.M Bright, C.R. Stoldt, D.J. Monk, M.Chapman, A.Saloan *Packaging of Advanced Micro- and Nanosystems* in H. Baltes, O. Brand, G.K. Fedde, C. Hierold, J.G. Korvink O. Tabata Enabling technology for MEMS and Nanodevices, Wiley-VCH Weinheim, Germany 2004
- [2] A.V. Chavan, K.D. Wise, *Batch-processed vacuum-sealed capacitive pressure sensors*, J. of Micromechanical systems, vol 10 p. 580-588, 2001
- [3] M.B. Cohn, Y. Liang, R.T Howe, A. P. Pisano, *Wafer-to-wafer transfer of microstructures for vacuum packaging* Technical Digest Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, USA, 3-6 June 1996, Cleveland Heights, OH, USA: Transducer Res. Found, 1996, p 32-5
- [4] K. Ikeda, H. Kuwayama, T.Kobayashi, T. Watanabe, T. Nishikawa, T.Yoshida and K. Harada, "Silicon pressure sensor integrates resonat strain gauge on Diaphragm, Sensor ans Actuators A, vol A21, pp 146-50, 1990
- [5] C. Rusu, H. Jansen, R. Gunn, A. Witvrouw, "Self-aligned 0-level sealing of MEMS devices by a two layer thin film reflow process" *Microsystem Technologies*, Germany \* vol 10 (Aug. 2004), no 5, p 364-71
- [6] R. Dekker, K. Dessein, J.-H. Fock, A. Gakis, C. Jonville, O.-M. Kuijken, T.-M. Michielsen, P. Mijlemans, H. Pohlmann-, W. Schnitt, C.-E. Timmering, A.-M.-H. Tombeur, "Substrate transfer: enabling technology for RF applications", *IEEE International Electron Devices Meeting 2003*, Washington, DC, USA, 8- 10 Dec. 2003 / 785507
- [7] E. Evoy, M. Dümling, T. Jaruhar *Nanoelectromechanical Systems*, in M. Di Ventra, S. Evoy, J. R. Heflin *Introduction to Nanoscale Science and Technology*, Kluwer Academic Publisher 2004