

# Schottky to Ohmic Transition in Pd/Ge Contacts on n-GaAs

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**Abstract**—This paper presents results of the electrical characterization of a Ge/Pd metallization scheme for *n*-type GaAs. A transition from Schottky to ohmic behavior is observed as the temperature of the Post-Deposition Anneal (PDA) is increased. Ohmic characteristics of the contacts are observed after anneal for 1 minute in a N<sub>2</sub> ambient at 400 °C and 450 °C.

**Index Terms**—Contact Resistance, Gallium Arsenide, Ohmic Contacts

## I. INTRODUCTION

WITH standard Si technology facing serious obstacles and reaching its physical limitations, there is an interest in research on alternative semiconductors allowing integration in the established technology platforms. In this context, a key role is played by III-V semiconductors such as GaAs and related material (InAs, InGaAs,...). The high mobility of III-V materials makes them ideal for high-frequency applications.

With a low lattice mismatch with Ge (only 0.07%), it appears straightforward to conceive as a next step the integration of III-V in Ge and Si technology. However, in order to reach such integration, important issues have to be addressed.

Recent efforts [1] have been focusing on the development of passivation layers for GaAs MOSFETs, proving that III-V are excellent candidates to be employed as channel materials for the next technology platforms.

Another concern, in view of integration, is to attain ohmic contacts on III-V developed with processes which are compatible with the ones employed in Si technology. The ability to create ohmic contacts to semiconductors is extremely important, as they allow injection and extraction of current from the terminals of any type of devices. A basic requirement of an ohmic contact is that it has a minimal impact on electrical characteristics, i.e., causing no potential drop across the contact. When a metal is put in contact with a semiconducting material, the mechanisms for current to flow are well known. For lowly doped materials, carriers can go over the energetic barrier (which depends on the affinity of the

semiconductor and the work function of the metal) by Thermo-ionic emission. For heavy doping conditions, the barrier becomes narrower and the probability of tunneling through it is high. This is the regime of Field-emission current. For intermediate doping levels the two mechanisms can occur at the same time, thus enabling a regime of Thermo-ionic field-emission.

It has been established that when a metal (or an oxide) is in contact with a GaAs substrate, the Fermi level of the structure is pinned in the middle of the band-gap. The explanation for this behavior has been ascribed to both the high density of Surface States ( $D_{SS}$ ) of GaAs [2] and to defect levels at the metal-semiconductor interface [3]. This phenomenon is independent of the metal and therefore makes creating a low-resistivity metal contact on GaAs difficult. Fermi level pinning also occurs in GaAs-related materials. In the case of In<sub>x</sub>Ga<sub>1-x</sub>As, the Fermi level is pinned at energy values approaching the conduction band as  $x$  goes to 1: in InAs the Fermi level is found to be pinned at the conduction band [4].

Conventional ohmic contact schemes for GaAs are gold-based sintered structures like Au/Ge/Ni for *n*-type material [5], and Au/Zn for *p*-type [6]. Such metallization strategies, despite offering a very low contact resistance, present important drawbacks: non-uniformity, surface roughness and a poor thermal stability due to a complex alloying process. Scaling down Au-based metallization to sub-micrometer dimensions is even more complicated. To overcome these limitations, reduce the thermal budget for ohmic contact formation and allow scalability, there is a strong interest in providing alternative contact schemes. These have been widely investigated, and excellent results have been reported using a Ge/Pd structure. First employed by Sinha et al. in 1975 [7], subsequent studies [8], [9] clarified the mechanism of Solid Phase Epitaxial Growth (SPEG) on which it is based. The technique involves the deposition of a metallic transport medium, Pd, onto GaAs, on top of which an amorphous layer of Ge is then deposited without breaking the vacuum. The thickness of the layers is chosen so that, upon anneal, the entire layer of Pd is consumed in the formation of a palladium germanide. The remaining amorphous Ge is then transported across the germanide to grow epitaxially at the GaAs interface. In addition, in-diffused Ge atoms serve as donors when incorporated on Ga sites, leading to a higher  $n^+$  doping. This results in a higher field-emission component and a better contact resistance. Transported Ge can also be doped, for example placing a thin

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layer of Sb inside the Pd layer [10].

## II. EXPERIMENTAL DETAILS

### A. Test Structures

To determine the contact resistance for ohmic contacts in semiconductors, Transfer Length Method (TLM) test patterns are used: they consist of a two-terminal structure with more than three contact pads. When a voltage is applied between two pads, the contact resistance and specific contact resistance can be determined by the linear relationship between the measured resistance and the gap spacing between the contacts. In such TLM structures, current crowding and spreading, as well as edge currents can seriously affect the results. To overcome these problems circular geometries are used. Circular Transfer Length Method (CTLM) contact resistance assessment provides an easy and rather straightforward quantitative result on the metal-semiconductor junction behavior [11]. In Fig. 1 a schematic representation of a single CTLM structure is shown.

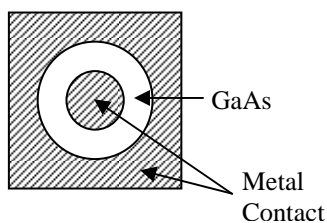


Fig. 1. Schematic of a single CTLM contact. The inner metal contact is separated by a ring-shaped layer of semiconductor material

Unlike traditional TLM, the CTLM has the advantage of not requiring a mesa etch step. In this case voltage is applied between the inner and the outer metal contact, and current flowing across is measured and the resistance changes with the gap spacing. Plotting the measured resistance as a function of the gap spacing typically yields a non-linear curve which can be made linear using correction factors [12]. This curve expresses the relationship between the total resistance and the gap spacing. The measured resistance  $R$  is given by the formula [13]:

$$R = \frac{R_{sh}}{2\pi R_1} (s + 2L_T) \cdot c$$

where  $R_{SH}$  is the sheet resistance,  $L_T$  the transfer length,  $s$  the spacing,  $R_1$  the inner metal contact radius and  $c$  the correction factor, given by the following formula:

$$c = \frac{R_1}{s} \ln \frac{(R_1 + s)}{R_1}$$

From the intercept with the  $y$ -axis twice the value of the contact resistance  $R_C$  can be extracted. The intercept with the  $x$ -axis yields a value of  $2L_T$ ,  $L_T$  being the transfer length

(inverse of attenuation constant).  $L_T$  values vary in the range of a few micrometers to several tens, with a shorter  $L_T$  indicating a better ohmic contact [13].

By conventional lift-off lithography, CTLM patterns were defined: electrical measurements were performed on two series of circular structures, with central diameters of 200 and 60  $\mu\text{m}$ , and the spacing varying from 8 to 256  $\mu\text{m}$ . More details are given further.

### B. Fabrication Process

The schematic process flow to fabricate the test patterns is shown in Fig. 2. On  $n$ -type Si-doped  $10^{18} \text{ cm}^{-3}$  GaAs substrates, a 20 nm thick layer of sacrificial  $\text{SiO}_2$  was deposited by Chemical Vapor Deposition (CVD). This layer was employed as a protective layer during the lithography steps, and etched by a buffered HF dip immediately before the metal layers were deposited. 50 nm of Ge and 50 nm of Pd were thermally evaporated onto the sample at a pressure of about  $2 \times 10^{-6}$  mbar.

A Rapid Thermal Anneal (RTA) was performed in a  $\text{N}_2$  ambient for 1 minute at various temperatures ranging from 200 to 450  $^\circ\text{C}$ . It has been pointed out [14] that for higher temperatures the structure of the compound semiconductor starts to degrade. Current-Voltage (I-V) electrical characterization was performed on the sample as deposited and following the annealing process.

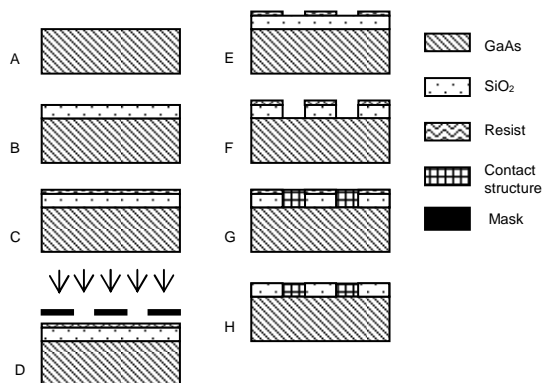


Fig. 2. Flow chart of the process to obtain CTLM structures: (A) Prepared substrate (B) Sacrificial  $\text{SiO}_2$  deposited by CVD (C) Resist spun-on for lithography processes (D) Exposure of resist (E) Development of the patterned wafer (F) Etching of  $\text{SiO}_2$  (G) Metal deposition (H) Lift-off: pattern ready to be tested.

## III. RESULTS

Fig. 3 shows the different I-V curves measured on the test structures with an internal dot diameter 200  $\mu\text{m}$ . The evolution towards the ohmic behavior as the temperature of the RTA process is increased is evident. The onset of ohmic operation occurs at 400  $^\circ\text{C}$  and improves with an additional 50  $^\circ\text{C}$ .

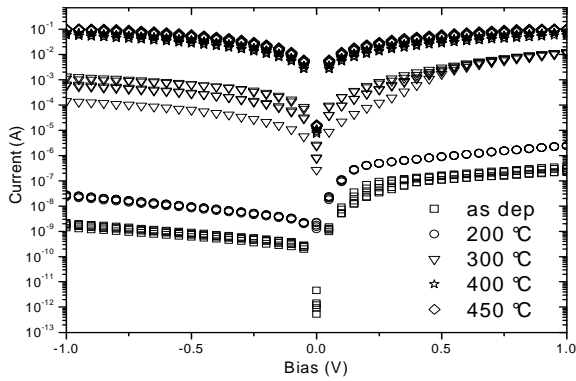


Fig. 3. I-V curves for the Pd/Ge CTLM contact of inner diameter 200  $\mu\text{m}$ . The different symbols refer to the different temperatures of the PDA treatment. Ohmic behavior starts for the sample annealed at 400  $^{\circ}\text{C}$  and improves by an additional 50  $^{\circ}\text{C}$ .

From electrical measurements on the CTLM structures it is possible to extrapolate values for the contact resistance of the Ge/Pd layer on GaAs. The relationship between the measured resistance and spacing for samples after anneal at 450  $^{\circ}\text{C}$  in  $\text{N}_2$  flow for 1 min is shown in Fig. 4. The two lines refer to the two series of contacts, with inner contact diameters of 200 and 60  $\mu\text{m}$ . A linear relationship is obtained with the application of the correction factors to the measured values, which depend on the contact sizes. The extracted values for contact resistance for the 200  $\mu\text{m}$  and for 60  $\mu\text{m}$  series of CTLM structures respectively are  $1.4 \times 10^{-3} \Omega \cdot \text{cm}^2$  and  $2 \times 10^{-4} \Omega \cdot \text{cm}^2$ . These are not exceptional results, but it definitely confirms that the Pd/Ge scheme is a candidate for low resistance ohmic contacts to GaAs and related materials, with scaling potential to the sub-22 nm CMOS technology node. A more in depth investigation of this contact scheme is currently ongoing, with the aim of assessing the structure and contact formation mechanisms by means of physical characterization and other analyses. This should lead to a further reduction of the contact resistance, by optimizing the layer stack. Future work will also focus on InGaAs layers on InP substrates and on replacing Ge by other group IV elements (Si, Sn).

#### IV. CONCLUSION

The Pd/Ge contact scheme on GaAs shows extremely interesting features and it's proven to be an excellent candidate for low contact resistance ohmic contacts on III-V materials. Furthermore the process of making such contacts seems to be compliant with Si technology specifications. Further investigation will be carried out to complete the picture on the physical structure of this metal scheme on GaAs and related materials.

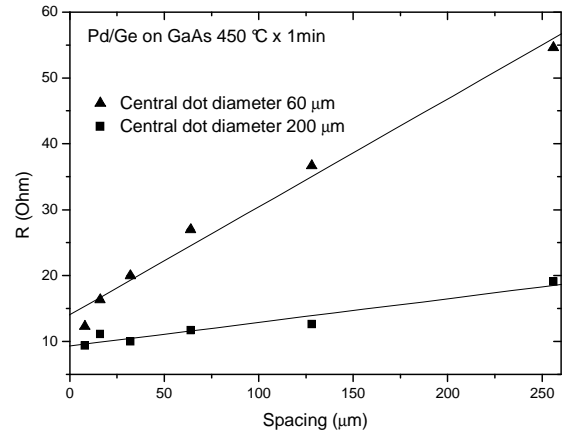


Fig. 4. The relationship between the measured resistance  $R$  and the contact spacing  $s$ . The metal layer consists of 50 nm Ge with 50 nm Pd on top of it. This metal contact has undergone a PDA treatment in a  $\text{N}_2$  ambient at 450  $^{\circ}\text{C}$  for 1 minute. The two lines refer to the two series of contacts with inner diameter of 60 and 200  $\mu\text{m}$ , respectively.

#### V. ACKNOWLEDGMENTS

The authors would like to thank Sophia Arnauts for the  $\text{SiO}_2$  deposition, Evi Vrancken and Dennis Lin for the support in lithography processes.

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