Electrical Characterization of PVD Aluminium Nitride Deposited on Silicon

Luigi La Spina, Siddharth Panwar, Hugo Schellevis, and Lis K. Nanver

***Abstract*—The electrical properties of the PVD AlN have been investigated by means of metal-insulator-semiconductor structures. The layers show an insulating behavior with a resistivity higher than $10^{12}\ \Omega\cdot\text{cm}$ for a thickness of 15 nm, and it increases with the thickness of the layer. Capacitance-voltage measurements are performed in several conditions and the results are presented and discussed. The dielectric constant is comprised between 9 and 11.5.**

***Index Terms*—Aluminium nitride, C-V measurements, physical-vapor-deposition, reactive sputtering, thin films.**

I. Introduction

Aluminium nitride (AlN) has been object of a considerable interest in the last decade due to its properties [1]-[14]. In particular, in our previous work AlN has been used to reduce the self-heating in silicon-on-glass bipolar junction transistors [15]. These devices are particularly prone to suffer from electrothermal effects because of the low thermal conductivity of surrounding materials, e.g. silicon dioxide and glass. In fact, the most commonly used dielectrics in silicon technology, such as silicon oxides and nitrides, are very poor thermal conductors. A reduction of the thermal resistance of the individual devices could be achieved integrating a material with higher thermal conductivity. Physical-vapor-deposited (PVD) AlN is a possible candidate. It is a very versatile III-V compound: it possesses a large energy band-gap and is compatible with standard silicon technology. Use of this material as an insulating layer above aluminium metallization on oxide has been demonstrated in our silicon-on-glass devices. A more effective heat spreading would be achieved if the AlN could be placed directly on the device silicon.

In this paper the electrical properties of the PVD AlN when deposited on silicon have been investigated by means of MIS (metal-insulator-semiconductor) structures. Current-voltage (I-V) and capacitance-voltage (C-V) characteristics are studied in detail and a physical interpretation of the non-ideal behavior of the curves is given. Compared to previous work [16], this paper analyzes the aluminium nitride in thin films with reduced thickness ranging from 15 nm up to 300 nm.

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II. Experimental

Two different sets of MIS structures are fabricated onto p-Si (100) wafers with a resistivity of $2-5\ \Omega\text{cm}$. In the first set, the thickness of the aluminium nitride layer is 100, 200 or 300 nm, whereas it is 15, 30, or 45 nm for the second set.

The aluminium nitride film is deposited by reactive magnetron pulsed-DC sputtering, in a Trikon Sigma sputter machine, with a pure Al target. A pulsed-DC power of 2 kW with a pulse width of 1616 ns and a frequency of 250 kHz is used. The substrate temperature is 380 °C for samples with AlN thicknesses from 100 to 300 nm and 280 °C for the deposition of AlN layers from 15 to 45 nm. In addition, two more wafers are fabricated with AlN layers of 15 and 45 nm deposited with a temperature of the substrate of 380 °C. The pressure is fixed to 5.0 mtorr. Nitrogen incorporation is achieved with a N_2 flow of 75 standard cubic centimeters per minute (sccm) and an argon flow of 38 sccm. No RF bias is applied and the tooling factor, i.e. the deposition speed over the applied power, is 169 $\text{Å}\text{min}^{-1}\text{kW}^{-1}$.

III. Results And Discussion

A. I-V Measurements

The results reported in this Section are obtained from measurements at room temperature on a Cascade probing station with an HP 4156C parameter analyzer.

The electrical resistivity has been measured with I-V measurements on capacitors with different areas, ranging from 0.0028 to 0.020 cm^2. A typical I-V characteristic is reported in Fig. 1. The range of voltage in which the AlN presents an insulating behavior increases with the thickness of such material. The resistivity of 100-nm-thick layer of AlN is in the order of $10^{12}\ \Omega\text{cm}$ in the range from –13 V to 13 V, whereas it is higher than $10^{13}\ \Omega\text{cm}$, in the range from –18 to 20 V, for thicker AlN layers, namely 200 nm and 300 nm.

Similar measurements are performed also on the test structures with thin AlN layers. The value of vertical resistivity is higher than $10^{12}\ \Omega\text{cm}$, in a range from –4 V to 10 V, even for a 15-nm-thick AlN layer. However, comparing the capacitors from the two sets, it should be noted that the structures with thinner AlN layer are not as robust as the ones with thicker AlN layer and tend to break down if a positive voltage of more than 20 V is applied. For negative voltages,

large currents can be made to flow through the capacitors without causing any permanent damage.

B. C-V Measurements

The area of the structure used in all the measurements reported in this Section is 0.0079 cm^2. C-V curves are obtained with an HP 4284A Precision LCR-meter operating up to 1 MHz.

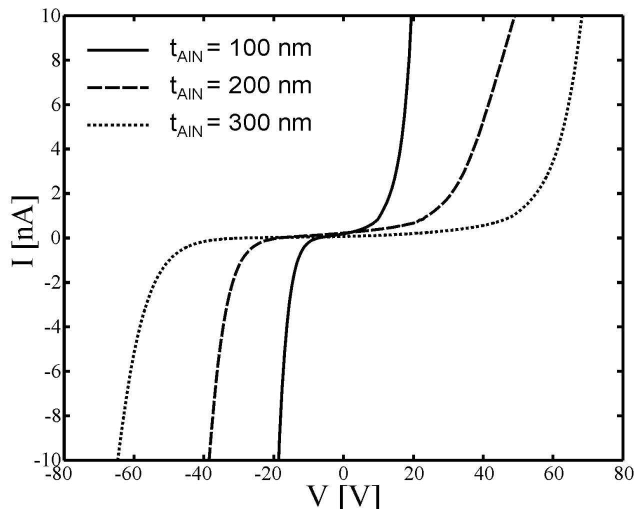

Fig. 1. I-V characteristics of structures with 100-, 200-, and 300-nm-thick AlN layers.

The first set of measurements, on wafers with thicker AlN layers, at both high frequency (HF) and low frequency (LF), are performed in dark. The C-V curves suggest that inversion is not achieved and, instead, the capacitors go in deep depletion, as can be observed in Fig. 2(a). Even slow voltage sweep rates are not helpful in preventing deep depletion and creating an inversion layer.

Some other non-ideal effects are also observed. A flattening of capacitance in the region between accumulation and deep depletion is seen in the C-V curves and, as evident from Fig. 2(a), it gets wider with increase in the frequency. This ledge of constant capacitance lasts only for a limited voltage range after which capacitors enter deep depletion. The same measurements are performed under light and shown in Fig. 2(b). A comparison of Figs. 2(a) and (b) suggests that the ledge of constant capacitance becomes larger under the influence of light.

A sudden change in the slope of the C-V curve, termed as a "bump", is also observed in many cases near the edge of accumulation/depletion zone in both LF and HF measurements, as highlighted in Fig. 2(b).

In the same figures, it can be also seen that the regions where LF and HF curves should ideally overlap, i.e. accumulation and depletion, the LF curve is lying above the HF curve. This observation can be attributed to the effect of an interface capacitance C_{it}. Just like how the minority carriers in the inversion region cannot follow the ac signal when high frequency is applied, the interface traps are also unable to respond to high frequency ac signals. At low frequencies, conversely, the traps begin to contribute to the charge flow. In other words, the effect of the traps on the measured capacitance can be modeled as interface capacitance, which comes in parallel with the depletion capacitance resulting in the increase of the total capacitance [17].

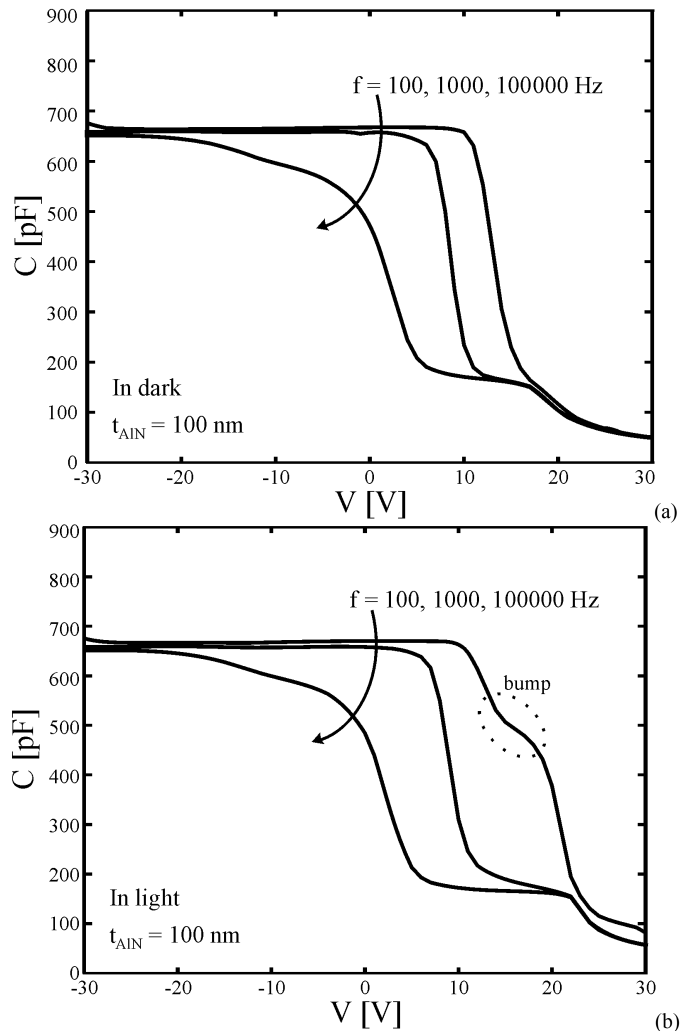

Fig. 2. C-V curves of a MIS capacitor with 100 nm of AlN at different frequencies performed (a) in dark, and (b) in light.

Fig. 3(a) compares the C-V measurements done in light with the ones in dark for the structure with 100-nm-thick AlN layer, which has the strongest non-ideal behavior among the structures of the first set. The measurements in Fig. 3(a) are performed with a light source stronger than the one used for the measurements in Fig. 2(b). Fig. 3(b) shows the C-V plot of the same structure when biased in accumulation for 120 seconds, followed by a sweep from accumulation to deep depletion and a similar biasing and sweep done in the other direction, i.e. from deep depletion to accumulation. The first observation is that pre-biasing the structure in accumulation or deep depletion for 120 seconds has no effect on the C-V behavior (compare Fig. 3(b) with dashed lines of Fig. 3(a)), proving that no additional charges were introduced into the dielectric from the substrate due to the biasing. This would have been evident if there had been any shift in the relative position of the C-V curves in the two cases, i.e. with and

without biasing at a constant voltage for 120 s.

Hysteresis is observed in both cases, when the capacitor is biased and when not, with a negative shift in the flatband voltage due to a positive fixed charge density.

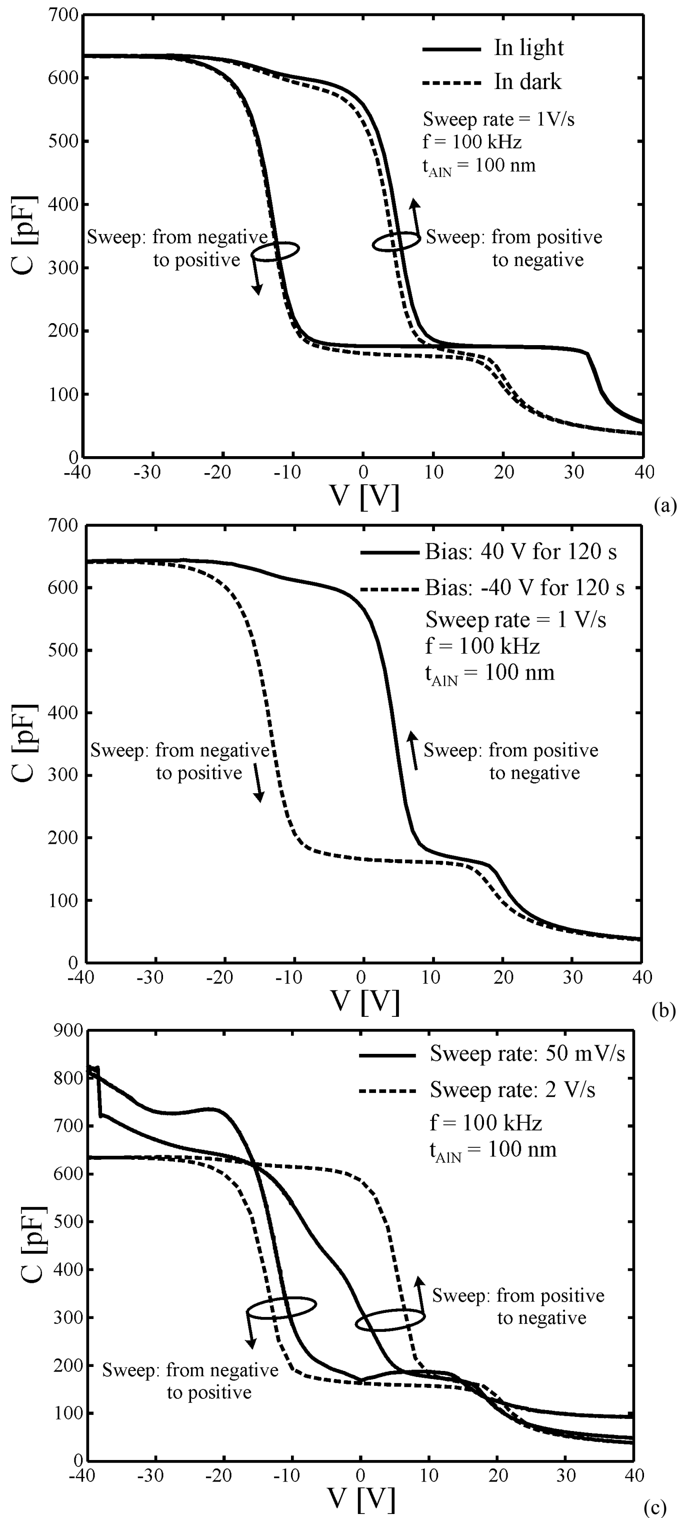

Fig. 3. C-V characteristics of a structure with 100-nm-thick AlN layer at high frequency. Influence of the: (a) light, (b) pre-biasing, and (c) sweep-rate.

The bump near accumulation is only visible when the sweep is done from deep depletion to accumulation (see Fig. 3(b), solid line). This abrupt change in the slope of the curve suggests a sudden change in the trap density. Due to their high emission constants, the negatively charged interface states that are beyond a limiting energy state from the conduction band cannot be discharged by emission process but only by hole capture, which cannot be achieved before the majority carrier concentration is high [18], [19]. Hence the bump is observed closer to the accumulation region and only when sweeping from positive to negative voltages. Accordingly, as seen by comparing Figs. 2(a) and (b), a strong bump is introduced in the low frequency measurement when done in light, due to the presence of more minority carriers.

The ledge, already mentioned previously, could possibly originate from the interface traps or from the lack of minority carriers. High-k dielectric materials like ZrO_2, HfO_2 and La_2O_3 [20]-[24] have been known to have frequency dependent distortion. However, the effect of the frequency in these materials is the opposite of the one noticed for AlN. For AlN the ledge becomes more prominent at high frequencies (see Fig. 2), but the opposite is true for other materials. If this phenomenon were due to interface traps, then biasing the capacitor in depletion region for some time or slowing the sweep rate should make the ledge wider. Indeed, biasing in depletion allows more complete thermal filling of the interface traps by electrons, and slow sweep rates keep the interface and the majority carriers in thermal equilibrium. However, in our experiments, biasing for 120 s at constant voltage (in strong accumulation or deep depletion) had no effect on the behavior and, moreover, the ledge was widened when the sweep was done from accumulation to depletion, which is contrary to what observed in [18] for other materials. Also, changing the sweep rate had no effect on the width of the ledge. As shown in Fig. 3(c), slower sweep rate reduces the absolute value of the slope of the C-V curve in depletion (the stretching of gate voltage axis), but does not increase the width of the ledge. To summarize we can say that: (i) the ledge increases with increase in frequency, (ii) is independent on the pre-biasing at a constant voltage and on the sweep rates, and (iii) does not enlarge when sweep is done from deep depletion to accumulation. All the three observations point to the fact that the ledge is not due to the traps. Use of light clearly widens the ledge, as illustrated in Fig. 3(a). For all these reasons, it seems that the ledge is simply the manifestation of minority carriers being generated. In the case of dark measurements the minority charges are not enough to make a complete inversion layer, but the formation of inversion layer gets assistance from the extra minority carriers generated by light. In other words, the ledge is just the onset of inversion whose extent depends on the availability of the minority charge carriers. The widening of the ledge when the sweep is done from accumulation to deep depletion can be explained on account of the expected negative shift in the flatband voltage and, consequently, in the point of the onset of inversion, due to the presence of positive fixed charge density in the dielectric.

Similar C-V measurements were performed also for the second set of wafers. Fig. 4 shows the low and high frequency behavior in light. None of the curves presents a rise in the

capacitance for inversion when measured at low frequency and all the wafers, for both high and low frequency measurements, converge to the same value of the minimum depletion capacitance.

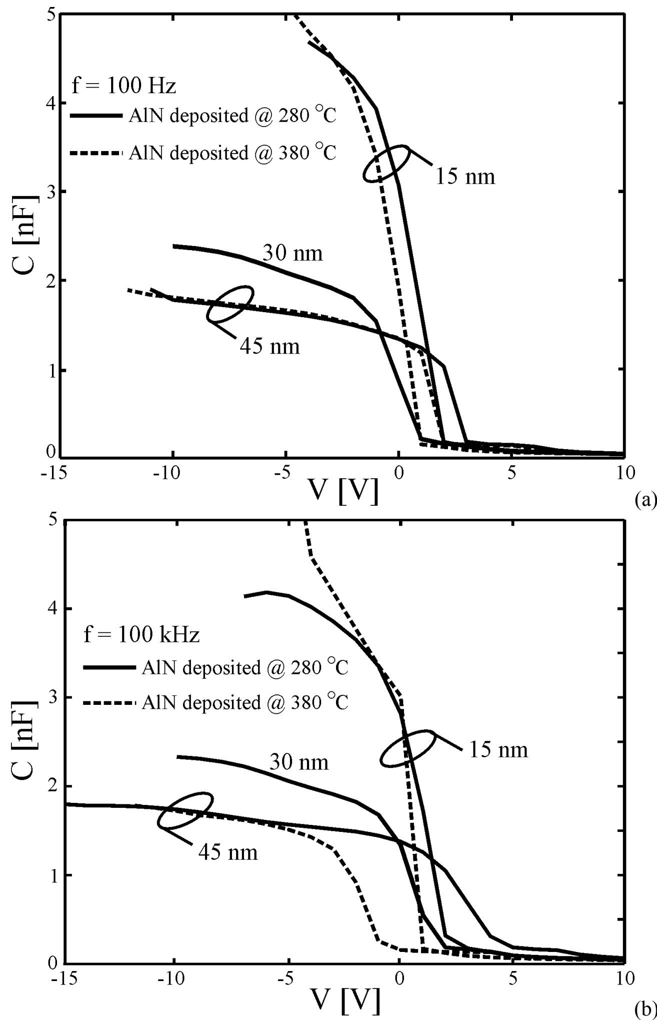

Fig. 4. C-V characteristics of capacitors with a thin layer of AlN. Analysis at (a) low-frequency, and (b) high-frequency.

Although the measurements in Fig. 4 are performed under light, the behavior in positive voltage range resembles deep depletion, since there is no flattening of the capacitance value, which is expected when inversion is achieved. As done for the previous set of wafers, the voltage sweep rate is reduced to see if that helps in promoting minority charge carrier generation. Fig. 5(a) shows the C-V curves of the capacitor with 30-nm-thick AlN layer, deposited at 280 ºC, with two different voltage sweep rates. A slower sweep rate increases the flatness of the curve (solid line) in the positive voltage range indicating the formation of an inversion layer.

Hysteresis can be seen also for capacitors with a thin layer of AlN, as it becomes clear from Fig. 5.

The effect of biasing the capacitor at a constant voltage in accumulation and deep depletion for 120 seconds is also studied, and reported in Fig. 5(b). Unlike the capacitors with thick AlN layers, the sweep done from accumulation to deep depletion after biasing the capacitor in accumulation for 120 seconds introduces a further negative shift in the flatband voltage, though the C-V behaviors for the sweep from deep depletion to accumulation are quite similar to each other when done with and without biasing. This implies a net increase in the fixed positive charge of the dielectric caused by biasing, which could be either due to ejection of trapped electrons from the dielectric or injection of holes into the dielectric [25].

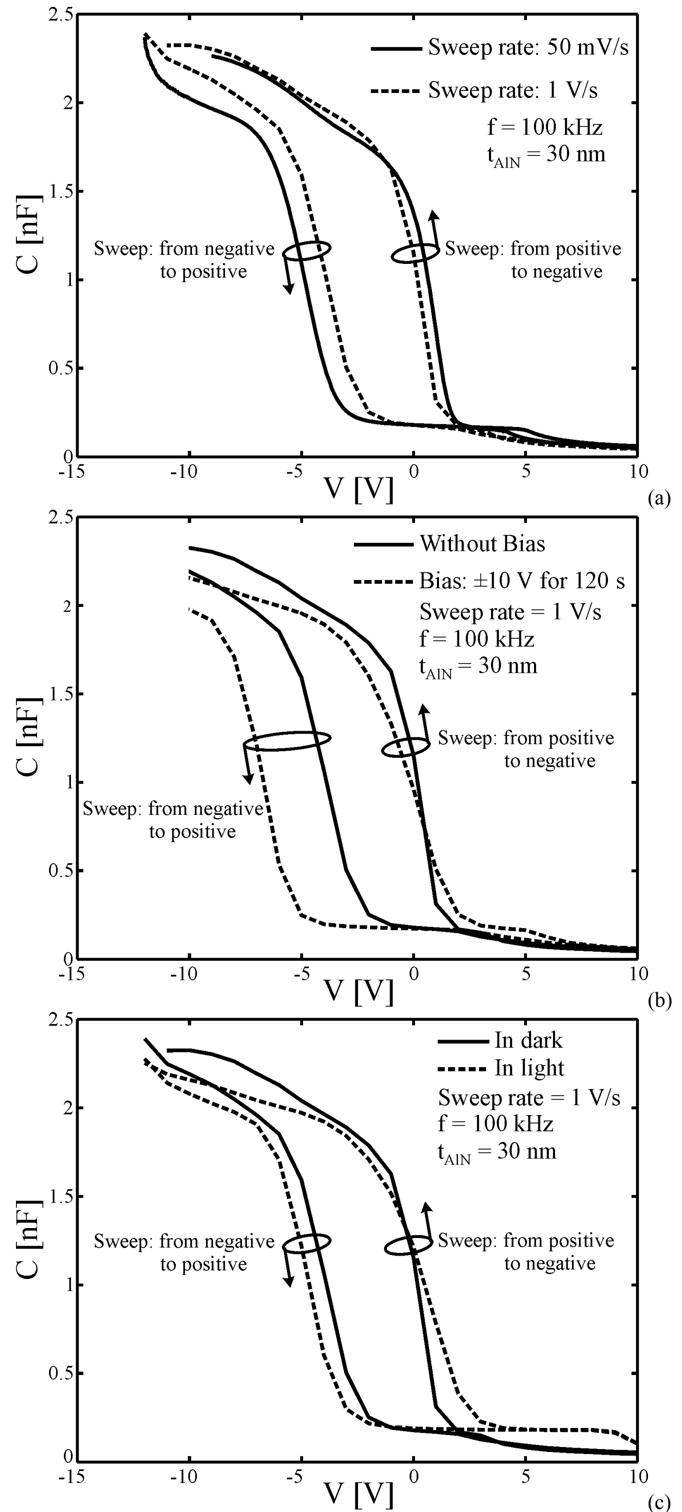

Fig. 5. C-V characteristics of a capacitor with a layer of 30 nm of AlN. Influence of the: (a) sweep-rate, (b) pre-biasing, and (c) light.

Fig. 5(c) illustrates the formation of a light assisted inversion layer that keeps the capacitance values above the values measured in dark for most of the positive voltage range.

From the above observations it can be concluded that, like the first set of wafers, most of the deviations from ideality are caused by the lack of minority charge carriers. However the non-ideal effects are not as exaggerated as in the first set of wafers. We see that the wafer with 30-nm-thick deposition of AlN responded to slower sweep rates whereas the wafers with thicker deposition of AlN have identical behavior for different sweep rates and enter deep depletion in all the cases. The better response of wafers from the second set for slower sweep rates could be due to a better control of the gate provided by the smaller gate thickness.

The dielectric constant of AlN is also computed for all the capacitors, with varying thicknesses of AlN, using the measured value of accumulation capacitance, and it falls within the range of 9-11.5.

IV. Conclusion

AlN is used as an insulator in MIS structures. Several capacitors have been analyzed with AlN thicknesses ranging from 15 nm to 300 nm. The results show that, with respect to the measured properties, the AlN can supply a reliable and reproducible isolation.

The interface Si/AlN has been investigated through C-V analysis. The effect of traps has been observed in the form of bumps near accumulation when the sweep is done from deep depletion to accumulation and reduction of the slope, in absolute value, in the depletion region. Measurements performed under light have led to an enhancement of the inversion layer due to an increment in minority charge carrier generation. Frequency dependence of capacitance results in higher capacitance values when frequency decreases.

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