

Sigma-Delta Modulators of 2nd- and 3rd-Order with a Single Operational Transconductance Amplifier for Low-Power Analogue-to-Digital Conversion

Alexander Mora-Sanchez, Dietmar Schroeder, and Wolfgang H. Krautschneider

Abstract—The use of a single amplifier to realise switched-capacitor (SC) based 1-bit low-pass sigma-delta modulators is presented. Sampling and integration operations are executed concurrently whereas the single amplifier is time-shared. It is shown that this method offers less power consumption than the traditional counterpart for modulation orders less than 4.

Index Terms—single-OTA, sigma-delta modulator, time-sharing, low-power.

I. INTRODUCTION

Sigma-delta ($\Sigma\Delta$) modulators are widely used in high-resolution analogue-to-digital (AD) conversion which is also robust to the inaccuracies of the analogue components. In [1] the traditional architecture of a 1-bit low-pass N^{th} -order single-loop $\Sigma\Delta$ -modulator is explained. This architecture corresponds to a chain of N SC-integrators with distributed feedback; thereby, the power consumed by the active components, i.e. amplifiers, is directly proportional to N .

In order to reduce the power consumption, an alternative structure which makes use of a single amplifier to conceive the 1-bit N^{th} -order $\Sigma\Delta$ -modulator for $N > 1$ is presented. Contrary to the traditional approach, where the sampling and integration operations are carried out consecutively within the sampling period T_s , the alternative structure performs those operations concurrently within T_s , while the number of integrations defining the modulation order is attained by time-sharing the single amplifier, a concept adapted from [2].

II. WORKING PRINCIPLE

Consider the SC-circuit depicted in Fig. 1. During $\phi_1 = 1$ the signal at input V_1 is sampled into C_{s1} and the charge present in C_{s2} is accumulated into C_{f2} . When ϕ_2 is active, the charge contained in C_{s1} is dumped into C_{f1} and at the same time the output voltage is sampled into C_{s2} . The processing of input V_2 is similar to that of input V_1 , except that it is sampled twice

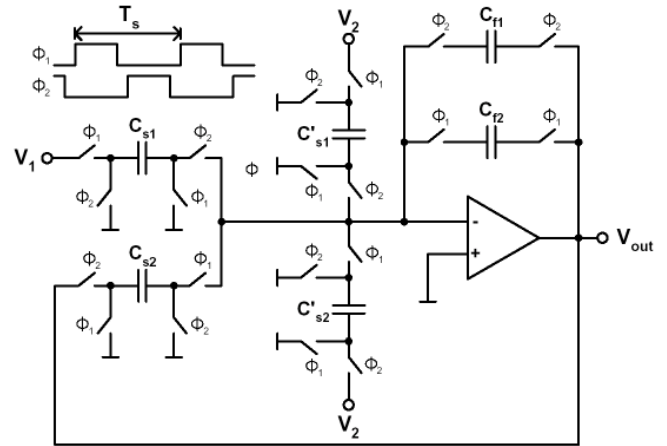


Fig. 1. Concurrent sampling and integration SC-circuit.

both during ϕ_1 and ϕ_2 . Note that sampling and integration take place concurrently.

Assuming ideal switches and amplifiers, it can be demonstrated following the analysis procedure of [3] that, if the inputs and output of the SC-circuit are taken when ϕ_1 is active, the transfer functions $V_{out}(z)/V_1(z)$ and $V_{out}(z)/V_2(z)$ are

$$\frac{V_{out}(z)}{V_1(z)} = H_1(z) = \frac{a_1 a_2 z^{-1}}{(1 - z^{-1})^2} \quad (1)$$

$$\frac{V_{out}(z)}{V_2(z)} = H_2(z) = \frac{a_2 b_1 z^{-1}}{(1 - z^{-1})^2} + \frac{b_2 z^{-1}}{1 - z^{-1}}, \quad (2)$$

with $a_1 = C_{s1}/C_{f1}$, $a_2 = C_{s2}/C_{f2}$, $b_1 = C'_{s1}/C_{f1}$ and $b_2 = C'_{s2}/C_{f2}$. By time-sharing the amplifier the circuit realises a double-integration on V_1 as well as a single- and double-integration on V_2 within T_s , which are precisely the operations a traditional 2nd-order $\Sigma\Delta$ -modulator performs on its input and feedback signals, respectively. Ultimately, the single-amplifier SC-circuit of Fig. 1 is employed to derive the 1-bit 2nd-order $\Sigma\Delta$ -modulator shown in Fig. 2, with a simpler clocking scheme as well as fewer switches than the one-opamp 2nd-order modulator reported in [4]. The modulator's signal transfer function $STF(z)$ and noise transfer function $NTF(z)$ are given by

A. Mora-Sanchez is with the Department of Microelectronics, Hamburg University of Technology, D-21073 Hamburg, Germany (Phone: 0049-40-428783727; fax: 0049-40-428782877; e-mail: rodrigo.mora@tu-harburg.de).

D. Schroeder and W. H. Krautschneider are with the Department of Microelectronics, Hamburg University of Technology, D-21073 Hamburg, Germany (e-mail: {d-schroeder, krautschneider}@tu-harburg.de).

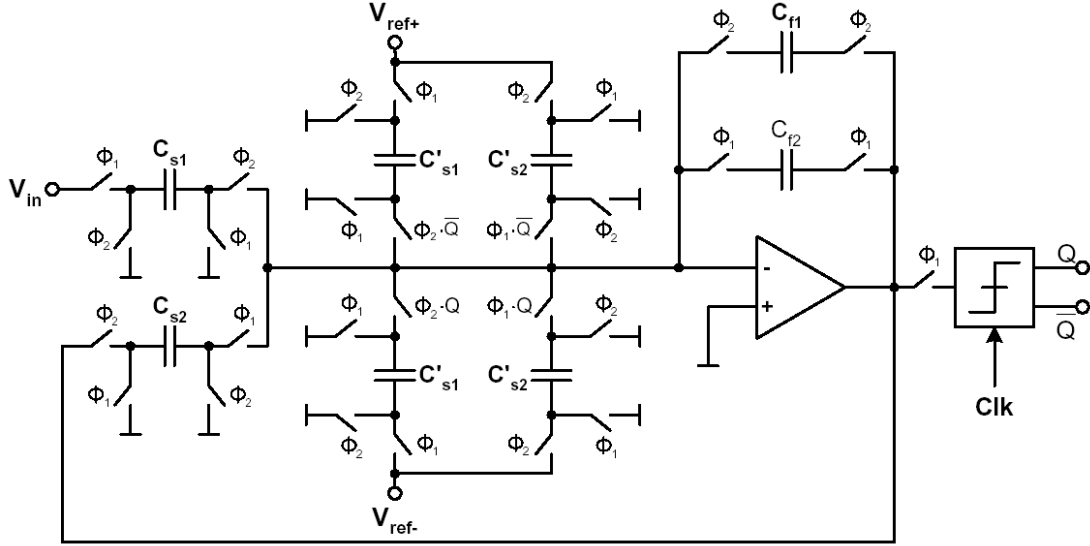


Fig. 2. Circuit-level representation of the 1-bit 2nd-order $\Sigma\Delta$ -modulator.

$$STF(z) = \frac{a_1 a_2 z^{-1}}{1 + (a_2 b_1 + b_2 - 2)z^{-1} + (1 - b_2)z^{-2}}, \quad (3)$$

$$NTF(z) = \frac{(1 - z^{-1})^{-2}}{1 + (a_2 b_1 + b_2 - 2)z^{-1} + (1 - b_2)z^{-2}}$$

where the quantiser is modelled as an additive white-noise source.

In Fig. 3, the proposed concept is extended to a 1-bit single-amplifier 3rd-order $\Sigma\Delta$ -modulator, wherein the amplifier has a time of $T_s/3$ to execute each integration. The corresponding $STF(z)$ and $NTF(z)$ can be demonstrated to be

$$STF(z) = \frac{a_1 a_2 a_3 z^{-1}}{1 + \alpha z^{-1} + \beta z^{-2} + \delta z^{-3}}, \quad (4a)$$

$$NTF(z) = \frac{(1 - z^{-1})^{-3}}{1 + \alpha z^{-1} + \beta z^{-2} + \delta z^{-3}}$$

with

$$\begin{aligned} \alpha &= a_2 a_3 b_1 + a_3 b_2 + b_3 - 3 \\ \beta &= 3 - 2b_3 - a_3 b_2 \\ \delta &= b_3 - 1, \end{aligned} \quad (4b)$$

and $a_1 = C_{s1}/C_{f1}$, $a_2 = C_{s2}/C_{f2}$, $a_3 = C_{s3}/C_{f3}$, $b_1 = C_s/C_{f1}$, $b_2 = C_s/C_{f2}$, $b_3 = C_s/C_{f3}$.

However, a higher modulation order N demands the amplifier to be faster since each integration has to be completed within a time T_s/N , thus imposing a limit to the feasibility of the approach from the power consumption standpoint.

III. POWER CONSIDERATIONS

Assuming that an operational-transconductance amplifier (OTA) is utilised as amplifier and that its settling time is linear and non-slew-rate limited when working as an SC-integrator, the reasoning considered in [5] will be followed in order to gain insights about the power consumption in terms of bias currents. Thus, for the amplifier in the traditional N^{th} -order modulator's SC-integrator (denoted OTA1), the relationship between speed and power consumption is determined by

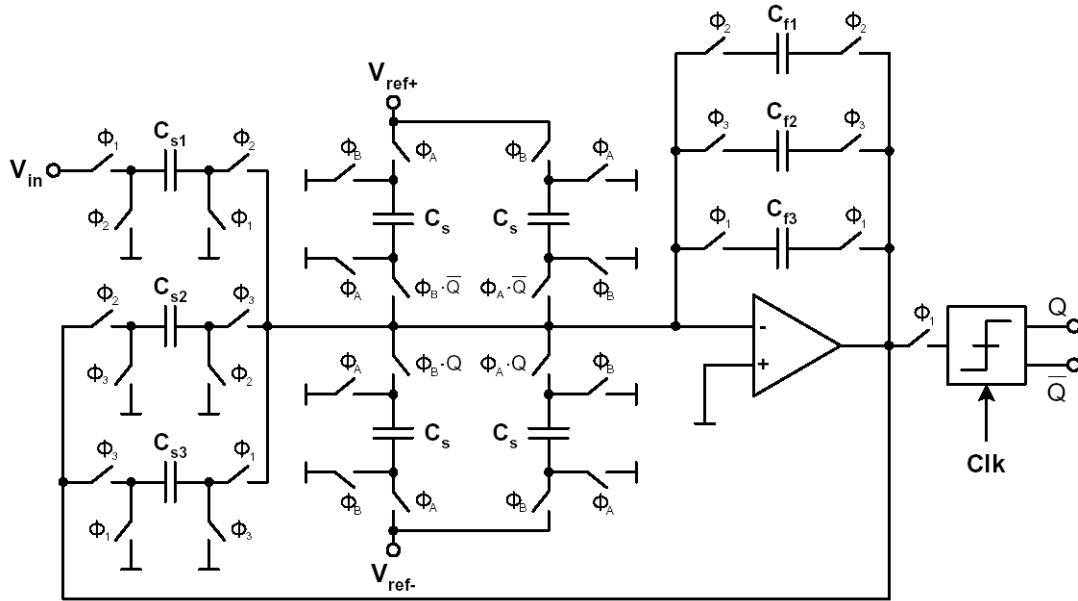
$$GBWP_1 = \frac{1}{C_1} \cdot \sqrt{2K \cdot \frac{W_1}{L_1} \cdot I_{DS1}}, \quad (5)$$

where $GBWP_1$ is the OTA's gain-bandwidth product, C_1 is the total equivalent loading capacitance in its integrator functionality, K , W_1 and L_1 are the input stage transistor's transconductance parameter, width and length, respectively, and I_{DS1} , the bias current through those transistors. Consequently, the traditional N^{th} -order modulator, where each SC-integrator has a time of $T_s/2$ to perform the integration, consumes a power directly proportional to $N \cdot I_{DS1}$, assuming that the amplifiers within the last $N-1$ SC-integrators are not scaled.

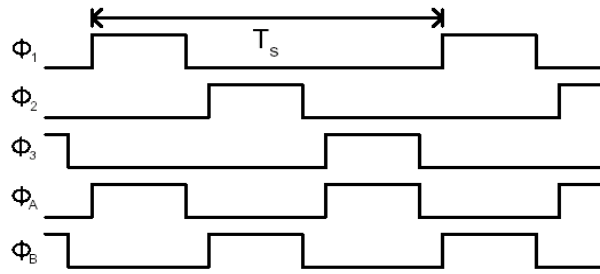
On the other hand, in a single-amplifier N^{th} -order $\Sigma\Delta$ -modulator there is a time of T_s/N for it to compute an integration. In this case, the amplifier (denoted OTA2) needs to be $N/2$ times faster than OTA1, i.e.,

$$GBWP_2 = \frac{N}{2} \cdot GBWP_1 = \frac{1}{C_1} \cdot \sqrt{2K \frac{W_1}{L_1} \left(\frac{N^2}{4} \cdot I_{DS1} \right)}; \quad (6)$$

therefore, OTA2 consumes a power directly proportional to



(a)



(b)

Fig. 3. Circuit-level representation of the 1-bit 3rd-order $\Sigma\Delta$ -modulator: (a) schematic, (b) clocking scheme.

$(N^2/4) \cdot I_{DS1}$ for transistor geometries and loading conditions similar to OTA1. As a consequence, in a 2nd-order and a 3rd-order modulator, 50% and 25% of the power is saved, respectively, by the single-amplifier approach, while for a 4th-order modulator no power is saved anymore.

IV. SIMULATION RESULTS AND DISCUSSION

The SC-circuits of Figs. 2 and 3 have been simulated with SWITCAP2 in order to corroborate the functionality and the performance of the 1-bit single-amplifier $\Sigma\Delta$ -modulation concept. The coefficients of the modulators are $a_1 = b_1 = 0.25$, $a_2 = b_2 = 0.125$, $a_3 = b_3 = 0.50$, which both guarantee that the outputs of the OTA remain bounded within the reference voltages (set to ± 1.65 V) and make the 3rd-order single-amplifier modulator be conditionally stable according to the root locus criteria [1]. Fig. 4 plots the power spectrum density (PSD) of the systems of Figs. 2 and 3 after sampling a 0.50 V, 100 Hz sinus signal at 100 kHz and acquiring 100000 output

samples. The 2nd-order and 3rd-order modulators achieve 69.2 dB and 87.6 dB signal-to-noise ratio, respectively, for an oversampling ratio of 128. These values have been also confirmed through Matlab/Simulink simulations. However, the effect of the OTA's non-idealities and noise mentioned in [6] need to be mapped to the proposed modulators to infer their impact on the performance. Other effects such as the on-resistance of the sampling and feedback switches as well as charge injection induced errors can be minimised [1][6][7]. These issues, together with OTA-scaling to achieve more power savings, will be addressed in future work.

V. CONCLUSION

The realisation of 1-bit single-amplifier single-loop $\Sigma\Delta$ -modulators has been addressed. It was shown that this approach represents an attractive solution for low-power applications requiring AD-conversion (e.g. portable biomedical applications, portable phones) if 2nd- or 3rd-order modulators are used.

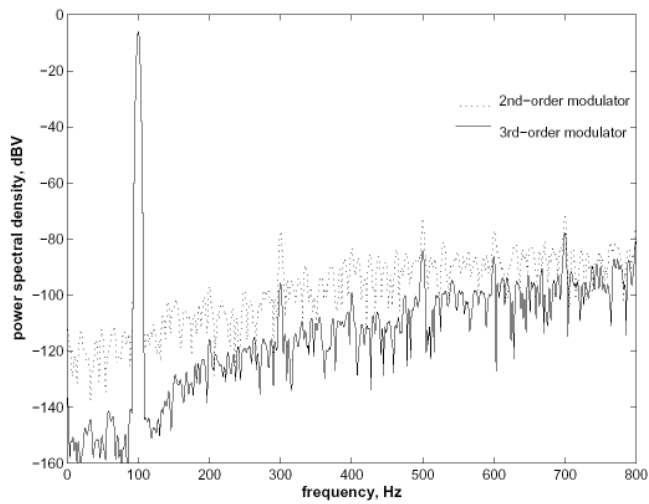


Fig. 4. Power spectrum of the single-amplifier modulators.

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