Low-Frequency Noise Characterization of Ultra-shallow Gate N-channel Junction Field Effect Transistors

G. Piccolo, F. Sarubbi, L. J. K. Vandamme, M. Macucci, T. L. M. Scholtes and L. K. Nanver

***Abstract*—A recently developed technique for ultra shallow pn junction formation has been applied for the fabrication of ring-gate n-channel junction field effect devices (JFET) devices. Several different geometries, gate formation parameters and channel doping profiles have been realized and characterized with respect to I-V and C-V characteristics both on wafer and after packaging. Low-frequency noise measurements have been performed on packaged devices by mean of a cross-correlation scheme. Data have been compared both with that of similar devices fabricated in a standard process and with simulations results. The devices show good DC performance, and the transconductance values achieved, with respect of the channel dimensions, are notably high. No G-R noise was detected, but the devices yielded a high flicker noise component. This phenomenon is shown to be neither correlated to the device area nor to incidental trapping levels at the junction interface. It is therefore assumed that perimeter effects are decisive for the enhancement of the *1/f* spectrum.**

***Index Terms*—Junction-field-effect transistors, low-frequency noise, ultra-shallow junctions.**

I. Introduction

PRESENT days see a continuous spreading of low level signal systems, which have in noise onset the lowest limit of sensitivity. A large part of electronic systems operate in the RF frequency range, where noise sources are fully known, characterized, and their effect can be properly handled. There is nevertheless an important niche of low-frequency devices application in sensitive systems. Low-frequency noise, also called *flicker noise* or *1/f noise*, remains an unsolved issue though largely discussed and studied [1]-[6]. No unified theory has been developed for the physical causes of this kind of noise: whereas the presence of interfaces, particularly defective ones, undoubtedly enhances its onset, Hooge [1] provided large experimental evidences of the bulk nature of *1/f* noise. Due to the noisy interface with oxide, MOSFET devices do not suit low-frequency low-noise applications, and BJT, which is commonly used for low noise application, cannot be used in case of high impedance signal sources. JFET can fill this gap perfectly, being less noisy than MOSFET but providing a high impedance input. Despite this, the actual entity and frequency range of *1/f* noise in modern JFETs are shown inadequately in literature, but for Levinson [7] that made an effort to fill this lack.

This work proposes to contribute to this effort, presenting the results of measurement run on test devices fabricated in DIMES laboratories.

The devices tested cover a quite wide combination of elements in term of channel dimensions and doping profiles, thus an analysis of resulting data had required a parameter that does not suffer for these differences. Hooge's empirical model describes the low-frequency power spectral density as

$$S_V = \frac{\alpha_H V^2}{Nf} \tag{1}$$

where α_H , Hooge's coefficient, is a constant typical for each kind of devices, V is the voltage drop across the channel expressed in Volts, N is the number of free carriers in the channel volume and f is the frequency in Hz. The quantity $C=\alpha_H /N$ does not depend on how we express the power spectral density (e.g. current fluctuation, voltage fluctuation, resistance fluctuation, etc.) and it is referred to as relative noise. If normalized by the sheet resistance R_{sh} of the conductive section of the device, i.e. the channel in our case, it gives a parameter that allows a comparison of different featured devices. The ratio $C_{us}=C/R_{sh}$ is called normalized relative noise.

II. Devices Under Test

A. Structure and technology details

All tested devices are double gate n-channel JFETs. Both top- and bottom-gate are externally accessible and have been driven separately.

Gate control is dependent on both the doping concentration and the abruptness of the gate plug. The gate effectiveness defines the transconductance value g_m, thus the gain of the device. In order to obtain the highest performance on a

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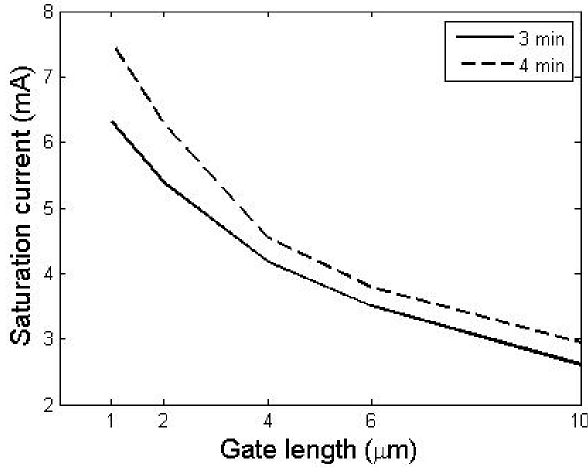

Fig. 1: Saturation current with respect of gate length, plotted for two different B-deposition times. Gate width is 430.4 μm for all the devices.

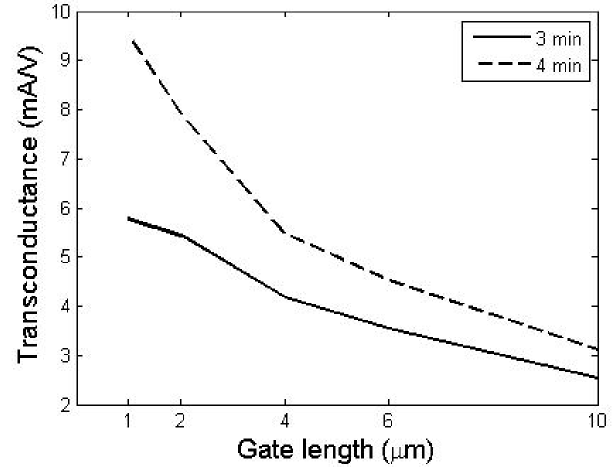

Fig. 2: Transconductance with respect of gate length, plotted for two different B-deposition time options. Gate width is 430.4 μm for all the devices.

standard bipolar process (that cannot realize, e.g., good quality schottky contacts), a thin layer deposition technique has been developed in DIMES by Sarubbi *et al.* [8], and here, for the first time, applied on JFET structures to realize the top-gate plug. This technique uses a pure boron atmospheric/low-pressure chemical vapor deposition (AP/LPCVD) in an epitaxial reactor to form less than 2-nm-thick δ-doped boron-silicide (B_xSi) layers on the silicon surface.

The bottom-gate is achieved by locally enhancing the substrate doping to provide a more abrupt junction with the channel. Nevertheless, this results in a poorer effectiveness of the bottom-gate if compared to the top-gate action in controlling the channel cross-section thickness. Thus, the devices have been driven through the top-gate, and the bottom-gate has always been biased so as to minimize the bottom-gate-to-channel depleted zone, i.e. short circuited to source.

The devices have been designed with a ring layout to make it easier to subtract parasitic effects.

Several top-gate lengths, from 1 to 10 micrometers, combined with several channel doping profiles have been characterized in order to investigate possible dependencies from device features. A set of standard devices has also been characterized to provide further elements of comparison for the devices under test (DUTs).

B. DC values

In order to verify the normal device operation and to provide elements for a correct interpretation of noise measurement data, DUTs underwent standard DC characterization and a CV doping profiling. Data have also been compared to device simulation on SUPREMIV. DC measurements have been performed on wafer using a Microtech Cascade probe station and acquiring data on an Agilent 4156C parameter analyzer. DC parameters, as saturation current I_{dss}, gate pinch-off voltage V_p, transconductance g_m and their trend with geometrical dimensions of the channel fitted both the comparison with the standard device and the simulation. It is to be highlighted, however, the higher values of g_m achieved, in accordance with the more shallow and abrupt top-gate to channel junction. Some results are shown in Figs. 1-3, where it is also highlighted the dependence of these parameters on the Boron deposition time.

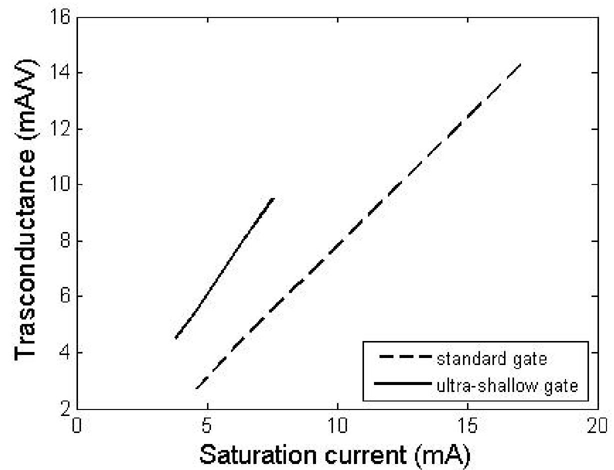

Fig. 3: Comparison of transconductance value with respect of saturation current between standard gate and ultra-shallow gate devices. Gate width is 430.4 μm for all the devices.

III. Measurement Setup

First thing to do when detecting low and ultra-low current or voltage noise levels, as nowadays obtainable from semiconductor devices, is to properly set up the system, to ensure that what is measured really comes out from the DUT. If the device noise happens to be very low, an amplification stage can be inserted between the DUT and the measuring instrument. If the DUT is an operating active device, the amplifier stage can be designed using the DUT itself as input active device. Otherwise, Low-Noise Amplifiers (LNA) or Ultra-low Noise Amplifiers (ULNA) can provide the required enhancement of the input signal. Nevertheless, it is now their

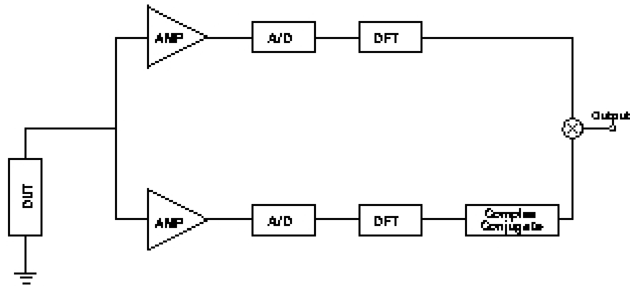

Fig. 4: Block diagram for a digital cross-correlation spectrum analyzer. In our system the amplifiers are external, while the A/D and signal processing part is implemented in the HP 3562A.

input equivalent noise that sets the sensitivity, which can make the measurement inaccurate as well. Noise measurements are also particularly sensitive to electro-magnetic interferences that can couple with wires used to connect different parts of the system: it is therefore important to operate in an environment that is properly shielded. Electronic components, due to current flux, can themselves produce electromagnetic radiation. To avoid any coupling among different parts of the measurements system, power supply, DUT, and amplification blocks have been separately shielded, and all interconnections have been made with coaxial cables. Ground loops have also to be avoided, since they couple easily with 50 Hz harmonics: the ground reference must be provided to all the blocks, taking care to connect each part only once. The use of a power supply for biasing is not strongly recommended, since power supplies are generally noisy, and, moreover, they are connected to the 50 Hz mains, which usually carries disturbances. Lead or Lithium batteries represent a better solution for supplying both the device and the amplifiers. A resistive voltage divider or a trimmer can be used to obtain the desired bias on the device, but the first is preferable, having no moving contacts which can contribute unwanted noise components. In our system, the DUT has been biased applying a voltage to the top gate and forcing the current on the drain terminal. Our devices, anyway, yield noise levels that were comparable to, or lower than, the front-end equivalent input noise sources, and thus a cross-correlation technique has been applied to achieve a sufficient accuracy. This technique is based on processing signals from two independent channels operating in parallel. It takes advantage of the un-correlation between the noise sources of the two input stages. Voltage noise is more efficiently measured with a parallel configuration, as that shown in Fig. 4. The signal from the DUT is read by two independent voltage amplifiers: in our system we made use of two external low-noise voltage amplifiers, namely *EG&G Brookdeal 5003* and *5004* characterized by a noise input equivalent voltage of 12 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz, and of 3 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 Hz, where the noise spectra is white. This configuration

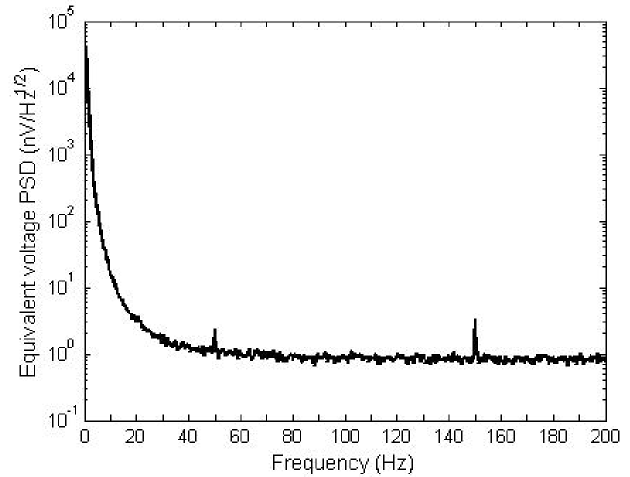

Fig. 5: Power spectrum for a standard gate device on a semi-logarithmic plot. *1/f* noise appears to have a poor component. The device has a gate width of 430.4 μm and a gate length of 1μm.

realized a reduction of the input equivalent noise voltage down to 1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz and 0.158 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$. To be noted that this scheme requires a DUT impedance much smaller than the amplifier input one. The complete signal processing is performed by the *HP 3562A Dynamic Signal Analyzer* that can operate in a frequency range from 10.2 mHz to 100 kHz.

IV. Measurement Results

Standard devices show very homogeneous results, with spectra shaped as the example shown in Fig. 5. For all tested devices, the ground noise fits the thermal noise of the channel and the low-frequency noise shows a clear 1/f spectrum with a corner frequency to the white noise around 30 Hz for all the devices. Hooge's coefficient achieves values around 10^{-8} and typical values for C_{us} in the order of 10^{-19} cm^{-2}. On the contrary, the ultra-shallow devices show a high *1/f* noise

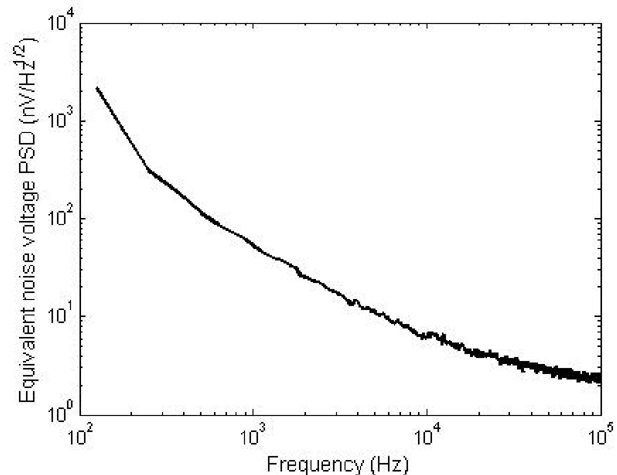

Fig. 6: Power spectrum for an ultra-shallow gate device plotted on logarithmic scale due to the wide frequency range covered. The device has a gate 430.4 μm wide and 1 μm long.

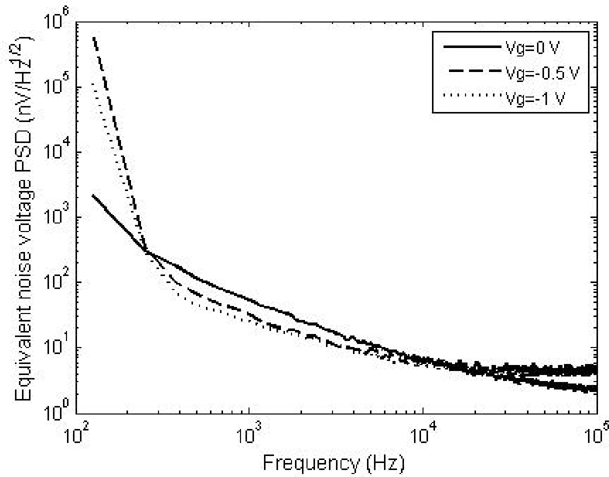

Fig. 7: Power spectra obtained on the same device by progressively increasing the negative top gate bias. For -1 V applied the channel results completely pinched-off. The device has a gate 1 μm long and 430.4 μm wide.

component, with no evident corner frequency to white noise up to 100 kHz, as shown in Fig. 6. This leads to Hooge's coefficient and C_{us} values of about 10^{-5} and 10^{-17} respectively. In the hypothesis that such a behavior is to be ascribed to traps states at the B_xSi-Si interface between the gate plug and the channel, a series of measurement has been conducted progressively pinching-off the channel conductive section in order to push the current away from the noise source. Results proved however that the hypothesis was wrong, since forcing the current flow away from the interface yield no appreciable effect on noise spectra, as reported in Fig. 7. Perimeter effects are therefore assumed to play a dominant role in the enhancement of the *1/f* component.

It is to be noted that, independently of the amplitude, all measured spectra exhibited a $1/f^{\gamma}$ trend, with γ within a range of 0.9-1.3, for at least a decade; therefore we can state that no G-R noise has been seen, either on standard or on ultra-shallow gate devices.

Acknowledgment

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