A 16GHz VCO and Quadrature Injection-Locked Divider Circuits

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Abstract—This paper presents the design of a CMOS Local-Oscillator (LO) circuit which comprises a 16GHz VCO and quadrature divider and is intended for a 24GHz dual down-conversion automotive radar receiver front-end. An LC-type differential VCO with optimal accumulation-mode varactor and differentially driven on-chip transformer gives wide frequency tuning range with competitive phase noise performance. Quadrature injection-locked divider covers the whole VCO tuning range by tracking its self-resonant frequency to the VCO frequency. Simulated in IBM 90nm CMOS technology with 1V supply, the 16GHz VCO consumes 13mW and the frequency tuning range is about 18% with phase noise of -97dBc/Hz at 1MHz offset. The divider consumes 18mW and locks to the VCO output with 6.02dB phase noise degradation.

Index Terms—VCO, Quadrature divider, LO generation, Automotive radar, Millimeter-wave.

I. INTRODUCTION

Automotive collision avoidance radar helps increasing vehicle safety and reducing number of fatalities in road crashes. The Short-Range-Radar (SRR) which occupies a 4GHz ultra-wide-band (UWB) spectrum between 22 to 26GHz detects object movements around a vehicle using multiple radar sensors [1] and has about 10 centimeters of range resolution. Continuous frequency modulation (FMCW) of a wideband VCO generates the UWB signal with high power efficiency because the transmitter and receiver are continuously active compared to the pulse radar having a high duty cycle [2]. Relative velocity and range of the target object is determined by the frequency difference of the transmitted and received signal, typically by a mixer circuit. CMOS is an attractive technology for implementing these sensors because of its potential for high level of integration with the baseband units and a low system cost.

This paper presents the design of a CMOS Local-Oscillator (LO) circuit that serves as the frequency reference of a 24GHz FMCW SRR radar. The circuit comprises a 16GHz VCO and a quadrature injection-locked divide-by-2 circuit and is shown in Fig. 1 together with the dual down-conversion mixers. The VCO and divider share the same tuning voltage (V_{tune}) for their self-resonant frequencies tracks each other in a 2-to-1 manner [3]. This ensures reliable injection locking of the divider over the wide VCO frequency range. Dual down-conversion receiver reduces the NF degradation due to the transistor flicker noise [4], which is significant in CMOS technology. This is because the received signal is well amplified and converted to an 8GHz IF before reaching the baseband circuit. Lower the NF increases the accuracy of the radar detection. The transmitted signal is generated by summing the VCO and divider output frequency. This reduces the frequency pulling from the transmitter power amplifier to the VCO and relaxes the isolation requirements of both the VCO circuit and sensitive signal paths.

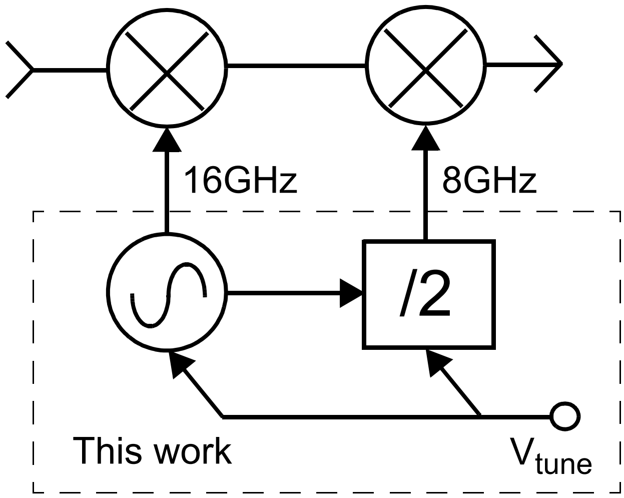

Fig. 1 Block diagram of a 24GHz dual down-conversion receiver front-end

II. VCO DESIGN

The VCO schematic is shown in Fig. 2. The frequency tuning network is a parallel resonant tank consisting of an differentially-driven symmetric transformer with primary and secondary wounding of T_{1-2} and accumulation-mode

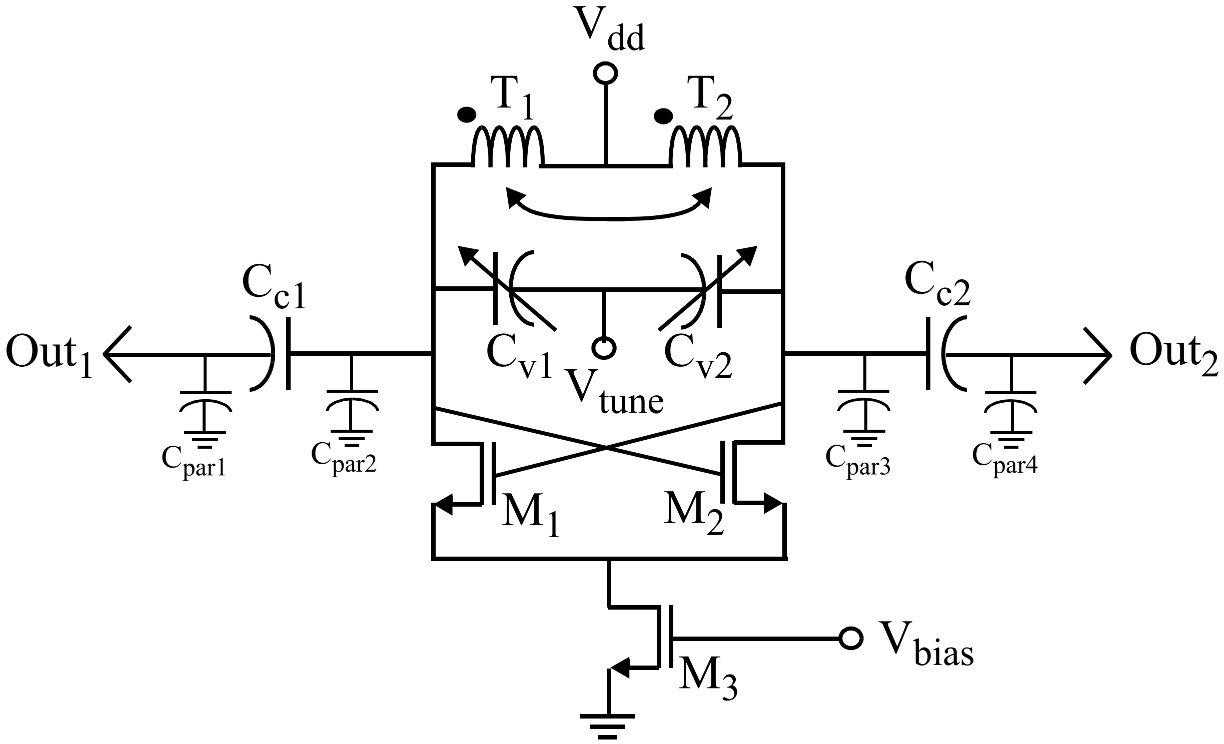

Fig. 2 Differential VCO with accumulation-mode varactor and differentially driven on-chip transformer

MOS varactor C_{v1-2}. The negative resistance synthesized by cross-coupled NMOS differential pair M_1,M_2 which cancels losses of the tank elements in order to sustain oscillation. The outputs are AC coupled to the divider by capacitances C_{c1-2} with their associated parasitic included. These parasites limit the maximum oscillation frequency and tunability of the VCO and should therefore be minimized by proper device selection and optimal sizing.

The transformer is optimized by parameters such as turns number, outer dimension and trace width. A smaller coil footprint is possible by exploiting the positive mutual coupling of adjacent wires in a multi-turns spiral. However, for a symmetric transformer, an underpass layer is required at the crossing junction [5] which increases the transformer series loss in a digital CMOS process that uses thin metal for the lower layers. A wider width gives lower ohmic loss but the substrate loss could be dominated at 16GHz, which hurts the Q and thus the VCO phase noise. A large substrate capacitance is also prohibited for the wideband requirement. The final transformer design is optimized as a single turn coil with metal width of 7μm and outer dimension of 140μm. The coil is verified by EM simulations using Momentum from ADS and the self-inductance of each wounding is 147pH. The simulated current density plot is shown in Fig. 3 proving that an octagon shape gives low current crowding [6] at 16GHz.

The Q-factors of the varactor and capacitive parasitic are inversely proportional to frequency and are affected by

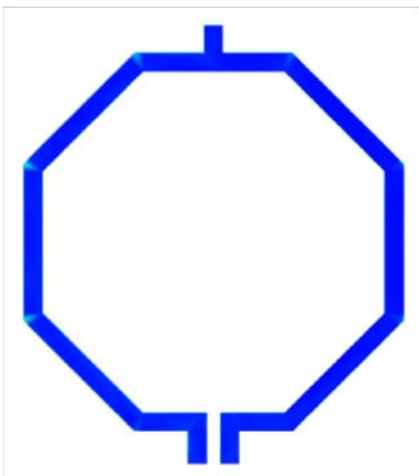

Fig. 3 Transformer current density at 16GHz

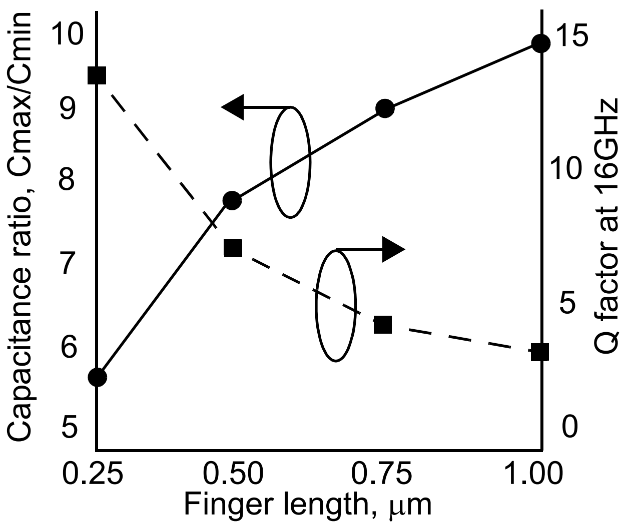

Fig. 4 Capacitance ratio and Q factor of an accumulation mode varactor versus finger length

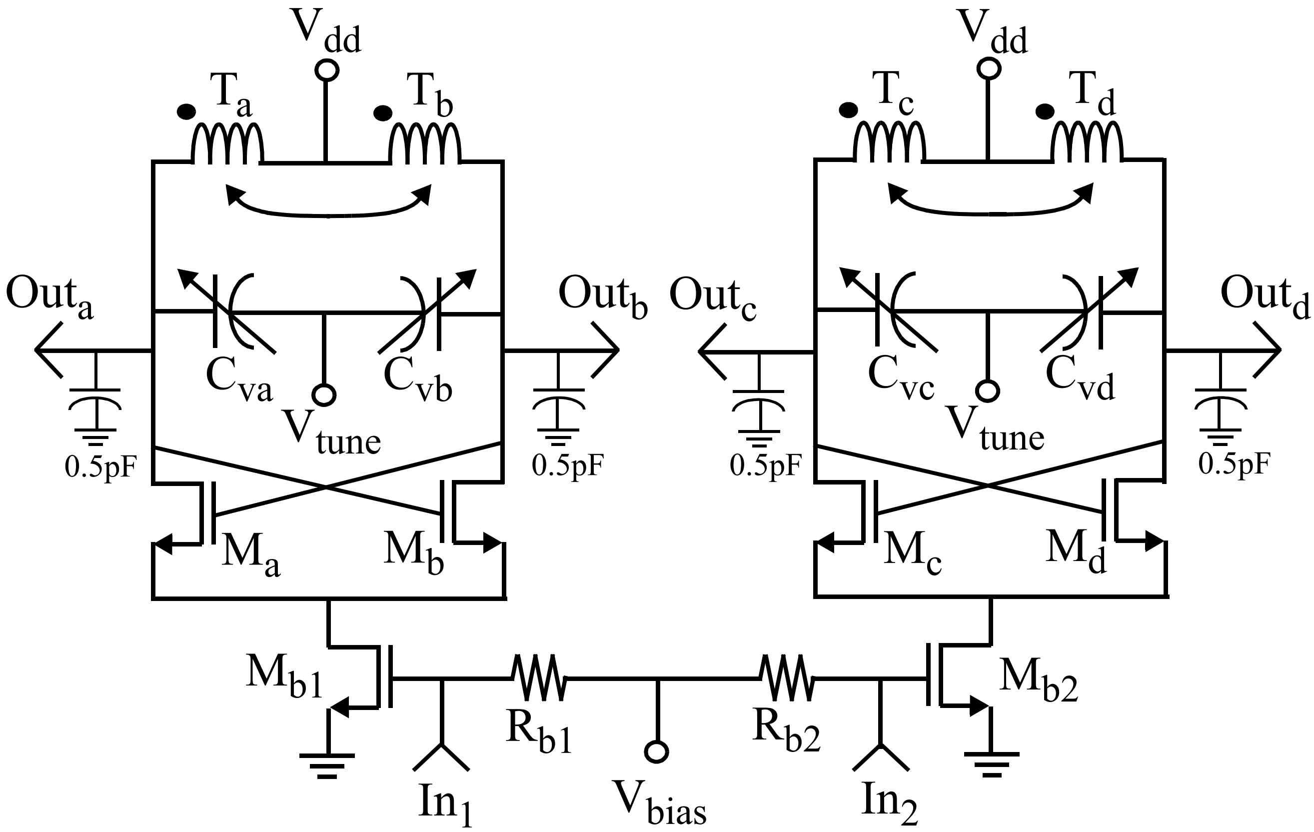

Fig. 5 Quadrature injection-locked divider with tunable self-resonant frequency

interconnect resistance, the resistance of diffused junctions, and losses in the semiconductor bulk. For example, the capacitance tuning ratio and corresponding Q-factor for an accumulation-mode 20x1μm finger varactor in 90nm RF-CMOS from simulations are shown in Fig. 4. The series resistance and capacitance are extracted from the real and imaginary parts of the simulated Z-parameters, respectively. As the length of each varactor finger is varied from 0.25μm to 1.0μm, it can be seen that the C_{max}/C_{min} ratio increases with increasing finger length from 5.6 to 9.9. The Q factor, on the other hand, decreases with finger length. Longer finger length gives a larger accumulation and depletion capacitance under the gate oxide layer and is favour for capacitance tuning, but this induces a larger channel resistance for the varactor. With the transformer having a Q of 25, the finger length is chosen as 0.25μm in order to maintain a high Q resonant tank for the VCO. Tuning range is maximized by using a low inductance value together with a 20x20x1μm varactor bank.

III. DIVIDER DESIGN

The divider schematic is shown in Fig. 5 which consists of two LC-type injection-locked oscillatory cells. Each cell is similar to the VCO circuit depicted in Fig. 2 with an appropriate scaling for the components values for a lower self-resonant frequency of 8GHz. Most importantly, the tunable range of the divider should be exactly half to that of the VCO for a high safety margin. The four 0.5pF capacitors are attached to the outputs of the divider to model the loading from the subsequence stages to the divider. Transistors $M_{b1\text{-}2}$ provide the DC bias current to the divider cell and simultaneously act as an injection device. The gate terminals are connected to V_{bias} via resistors $R_{b1\text{-}2}$ and the inputs are AC coupled to $In_{1\text{-}2}$ (via $C_{c1\text{-}2}$ in Fig. 2). The optimization of the differential transformer and varactor are the same as described in Section II.

IV. SIMULATION RESULTS

The VCO and injection-locked divider are simulated in IBM 90nm CMOS technology. Fig. 6 shows the frequency tuning

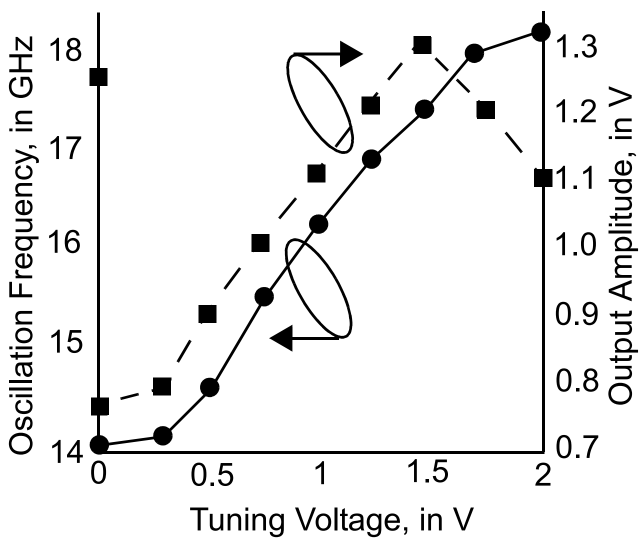

Fig. 6 VCO frequency tuning curve and voltage amplitude

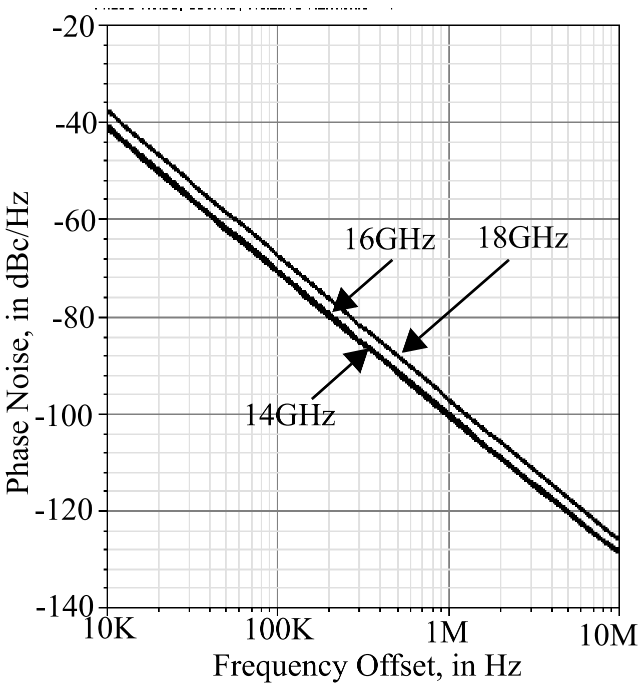

Fig. 7 VCO phase noise at 14, 16 and 18GHz

curve and single-ended output voltage amplitude. Tuning is continuous and monotonic from 14.02 to 18.36GHz with a 0 to 2V tuning voltage. The tuning range is 18% which marginally exceeds the SRR system requirement of 16.7%. The minimum output voltage amplitude is $0.75V_{pk}$ which is large enough to drive the divider and mixer circuits.

Phase noise is simulated at three oscillation frequencies and the results are shown in Fig. 7. At 1MHz frequency offset, the phase noise are -100.8, -100.1, and -97.1dBc/Hz for an oscillation frequency of 14, 16, and 18GHz, respectively.

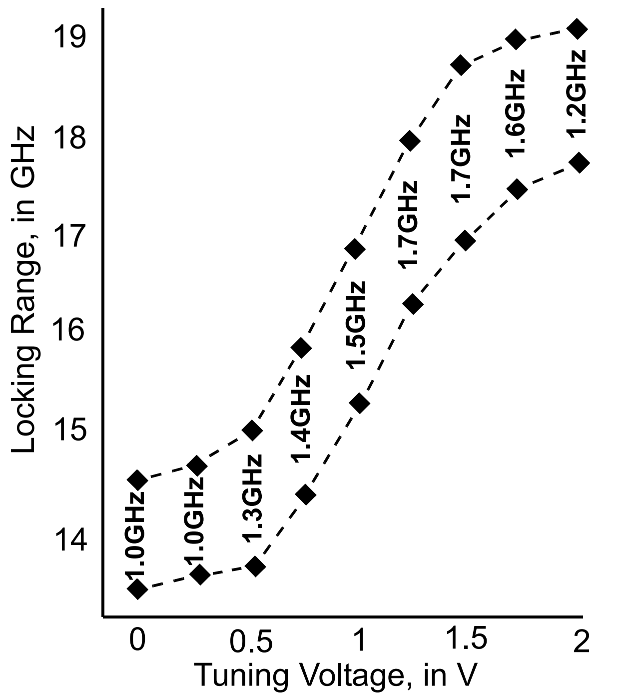

Fig. 8 Divider locking range over the overall bandwidth

The noise slope maintains -30dB up to 10MHz offset, caused by the high flicker noise of the CMOS technology. Additionally, the VCO is not optimized for lowering the $1/f^3$ noise intercept point but for wideband and high output voltage amplitude. The VCO consumes 13mW from a 1V supply.

The divider locks to the VCO over the entire frequency range. The locking range over the 14 to 18.4GHz VCO frequency is shown in Fig. 8 and it varies from 1.0 to 1.7GHz. The minimum design margin from the lock range is +/-0.5GHz. The divider gives a minimum output voltage of $0.7V_p$ across the tuning range. The power consumption is 18mW from a 1V supply with an ideal 6.02dB phase noise degradation compared to the VCO output.

V. CONCLUSION

A CMOS Local-Oscillator (LO) circuit which comprises a 16GHz VCO and quadrature divider are designed and simulated in a 90nm CMOS process. Techniques including differentially symmetric transformer in octagon shape and optimal finger width of accumulation-mode varactor give a wideband VCO with low phase noise and high output amplitude. Continuous tracking of the divider self-resonant frequency to the VCO frequency with appropriate components scaling gives a high safety margin for the injection locking. Proposed to be integrated into a dual down-conversion receiver for 24GHz short-range-radar, the VCO gives a tuning range of 18%, phase noise of -97.1dBc/Hz and minimum output voltage amplitude is $0.75V_{pk}$. The divider covers the whole frequency range. The complete circuits consumes 31mW from a 1V supply.

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