

A Re-Timing Pre-Driver for 40Gb/s Modulator Driver Design

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Abstract — A re-timing pre-driver is simulated in a commercial 0.13 μ m BiCMOS technology. Design issues related to re-timing pre-drivers for high-speed architectures (e.g., 40Gb/s) include optimal re-timing of the quadrature data streams and high-speed symmetric rise/fall times (e.g., $t_r < 6$ -8psec) for current switches biased at 3mA-12mA. Amplitude distortion is of particular importance in high bit-rate transmitters as it primarily affects intersymbol interference and bit-error rate. The pre-driver uses translinear current switches to minimize current overshoot, improving the latch speed and amplitude distortion

Index Terms — OC-768, Pre-Driver, Translinear.

I. INTRODUCTION

Foreseeable consumer demand for broadband services such as 4G wireless systems will flood backend optical networks with an increase in data traffic. These networks will be forced to operate at higher speeds in order to support multimedia tributaries such as 4G handsets. Optical networks will expand in infrastructure, requiring more electro-optical interface equipment at a lesser cost, while next generation optical systems like SONET OC-768 will attempt to stem the influx of traffic at channel data transfer rates in excess of 40 Gb/s. However, improvements introduced by OC-768 will have to scale in tandem with the cost of network exhaustive user devices. In other words, cost-effective Si-based technologies should be further utilized in the realization of high-yield and highly-reliable OC-768 chipsets. This poses a formidable design task for any technology, as fibre system capacity is incriminated by a factor of four every 3-5 years generation (current systems operate at 10 Gb/s while the fibre capacity is in the THz range).

A pre-driver is a circuit element that is typically integrated in high-speed circuits that require low-power digital signaling (e.g., 2-3 mA) to be buffered to higher power levels (e.g. 16 mA). The benefits of using an edge-triggered (i.e., re-timing) pre-driver approach include mitigating signal distortion effects induced by emitter-follower buffering (e.g., asymmetric rise/fall

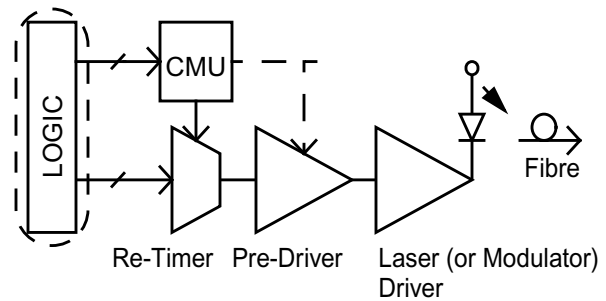


Fig. 1. Typical transmitter architecture for opto-electronic applications

times, peaking) as well supporting the option of designing for multi-data channels for use in distributed amplifiers (or modulator driver designs).

In this paper, a clocked pre-driver in a commercial 0.13 μ m BiCMOS technology is designed for SONET OC-768, where bit-rates use bandwidth in excess of 40 GHz. Design issues associated with the clocked pre-driver include concurrently replicating fully-differential data (Gb/s) and clock (GHz) signals while maintaining a compact form-factor (e.g., minimum number of devices). Two quadrature data channels operating at 20Gb/s are concurrently edge-triggered (and buffered) by a 20GHz clock source. The clock source is also driven (buffered) to a higher power level in which the quadrature data channels are combined into a single 40Gb/s output via a high-speed selector. By operating the pre-driver at half-rate (20Gb/s), the inverting and latching stages can be designed without the need for on-chip passives (e.g., peaking inductors) which are traditionally used to extend signal bandwidth at the expense of peaking [1]. In addition, fully-differential clock signaling is provided by translinear amplifying stages, which are used to drive the data-latching stages, reducing the overall buffer fan-out (i.e. device and power reduction) between clock and data paths. Thus, a compact high-speed pre-driver which encompasses the bene-

fits of data re-timing is demonstrated, lending itself as a potential circuit for 40Gb/s modulator driver design

II. RE-TIMING PRE-DRIVER DESIGN

A typical transmitter used in electro-optical applications is illustrated in Fig. 1. Intended data is first re-timed and driven (buffered) to higher bias levels that allow a modulator driver (or laser driver) to be concurrently operated at high-speeds with an eventual decent extinction ratio. The disadvantage of this classical approach is that the pre-driver operates at full-rate. That is, each buffering level must be able to operate at full-rate. While speed-enhancing circuit techniques (e.g., inductive peaking) in tandem with high- f_T BiCMOS technologies (e.g., $0.13\mu\text{m}$ 200GHz- f_T) have continued to allow this classical approach to operate above and beyond 40Gb/s [1], it comes with compromise. Firstly, inductive peaking in both ECL and $E^2\text{CL}$ design can cause significant signal distortion (via non-uniform) group delay at frequencies above 20GHz. Without careful emitter-follower optimization, this effect can translate into unwanted over/undershoot and asymmetric rising and falling edges, yielding the need for additional waveform control circuitry.

The proposed pre-driver (seen in Fig. 2) attempts to mitigate the aforementioned effects by driving (buffering) the data at half-rate (20Gb/s). A disadvantage to this approach is that more hardware is required to transport the data to a high-speed selector. In addition, since the two data paths operate in quadrature, data-re-timing throughout the buffer chain is needed in order to maintain proper timing margins at the selector stage. Since signal integrity along the clock line is paramount, a transconductor preceding the clock line is used to adjust (and cancel) any possible input DC offsets, which consequently would maintain a 50% duty-cycle.

Schematic of the clock driver cell is shown in Fig. 3. It is a cascode current switch followed by double emitter following stages. The use of the cascode buffer allows for high-speed operation with increased driving capability (i.e., greater fan-out) relative to a single inverter. However, the cascode configuration (in the clock driver) in a bipolar technology also allows for an alternative means for driving the subsequent stages of the clock driver and data latches. That is, by driving the latches from the differential pair, the cascode (common-base device) allows the data latches to be driven via translinear loop. The inherent advantage of the translinear loop is its high-speed. In addition, it reduces the RC loading at the output of the buffer cell, which ensures high-

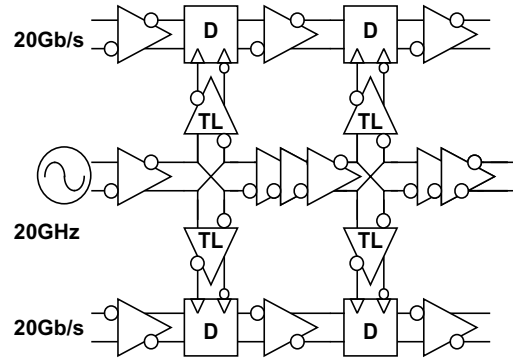


Fig. 2. Simplified electrical circuit of the clocked pre-driver.

speed driving of the following clock stage. Furthermore, the current-mode clock signals from the translinear differential pairs are guaranteed to be in phase ensuring proper timing margins. For example, if the clock signals are buffered through one (or two) emitter followers, any mismatch in these networks (e.g., bias resistor) may cause pulse-width distortion as well as skewing in the quadrature data signals. Lastly, additional buffers are inserted in the clock line to improve (re-construct) the clock signal and to also match the propagation delay(s) for optimal latching and data selecting timing margins. With optimal timing margins, the amount of jitter appearing in the data signals is reduced, which improves the eventual eye-quality of the high-swing output signal of the modulator driver.

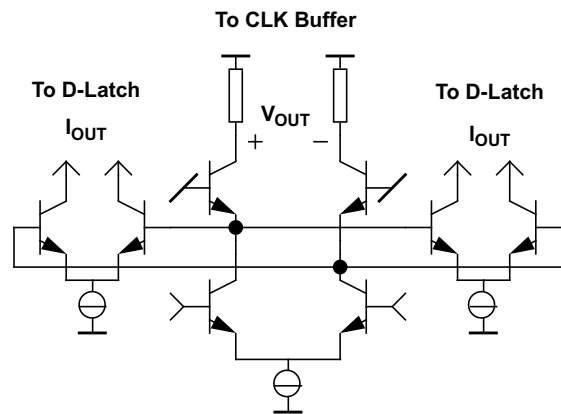


Fig. 3. Simplified electrical schematic of the translinear clock buffer.

III. SIMULATION RESULTS

A post-layout pre-driver design was simulated using the Cadence Spectre simulator. The transit frequency as a function of the collector current density for this particular 0.13 μm BiCMOS technology is depicted in Fig. 4. For all intents and purposes, the current switches used in the clock and data buffers are biased at a collector density which corresponds to 80% of the maximum transit frequency. Biasing the devices such that maximum transit frequency coincides at the switching point ensures fast-switching operation which also minimizes the propagation delay of the gate [2]. However, the ft-curve (see Fig.4) also illustrates a sharp roll-off beyond maximum ft, prompting the need for models which accurately capture the effects seen in the high-current regime (e.g., HICUM or Mextram).

At higher bias levels (e.g., > 4mA) current switch operation in a $E^2\text{CL}$ chain becomes more problematic to control. That is, larger capacitances (device and interconnect) causes unwanted overshoot. For example, the differential pair of a current switch is being driven by a low impedance voltage source (i.e., output impedance of a double emitter-follower buffer). However, the differential pair also drives a low-impedance cascode device. Thus, fast transient currents will first propagate through the device overlap capacitance before charging the base-emitter junction. Methods used to control the amount of overshoot usually involve either increasing the output impedance of the emitter-follower network, thereby degrading the rise/fall times (i.e., decreasing the bandwidth) of the traversing signal, or biasing the differential pair devices in the high-current regime. Given that SiGe HBT devices already operate at higher current densities (relative to other III-V HBTs), other (more reliable) high-speed circuit techniques are needed to control overshoot.

Translinear circuit design techniques are inherently high-speed, given that they operate in the current-mode. That is, translinear circuits drive low-impedance nodes and are evidently used in broadband RF circuits. Thus, the transient operation of a translinear switching pair is of particular interest. Fig. 5 illustrates the output current of both a transconductor and translinear switching pair. The overshoot seen in the transconductor pair is a function of the overlap capacitance as aforementioned. However, the overshoot in the translinear pair is absent. This is understood by first considering that the voltage levels at the base terminal are significantly smaller when being current driven. However, current-mode

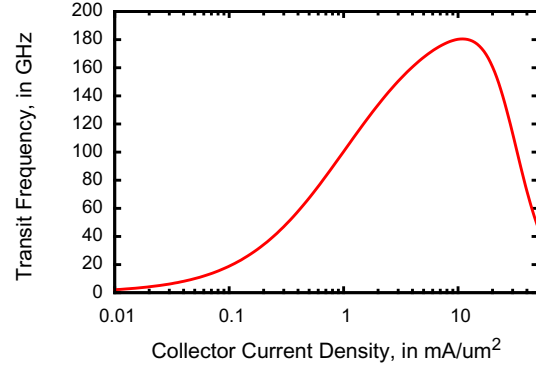


Fig. 4. Transit frequency curve as a function of current density.

operation does not guarantee overdamped, or even critically-damped switching operation. Bandlimiting mechanisms in the current-mode include parasitic resistances which is most identifiable as base resistance. Thus, devices with higher base resistance (smaller tail current) are band limited in producing critically damped transient currents. Moreover, larger tail current devices (i.e., devices with less base resistance) can also exhibit variable damped responses. For example, it can be shown that the transient current response of a translinear pair is a function of the ratio of collector current densities of the differential pair and the common-base pair. That is,

$$J_{A2} > J_{A1} \rightarrow \textit{overdamped}$$

$$J_{A2} < J_{A1} \rightarrow \textit{underdamped}$$

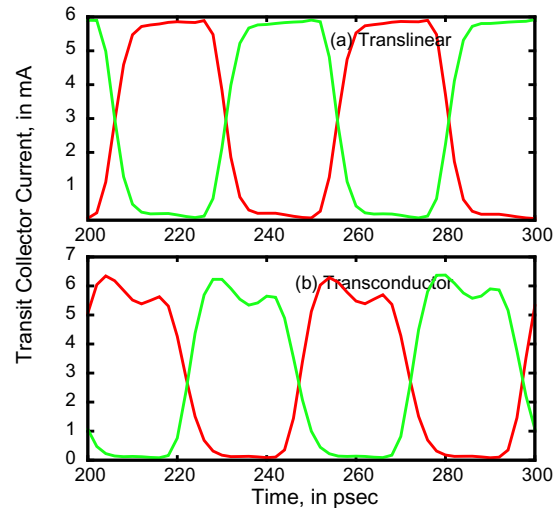


Fig. 5. Transient currents of (a) Translinear (b) Transconductor differential pairs biased at 6mA tail current

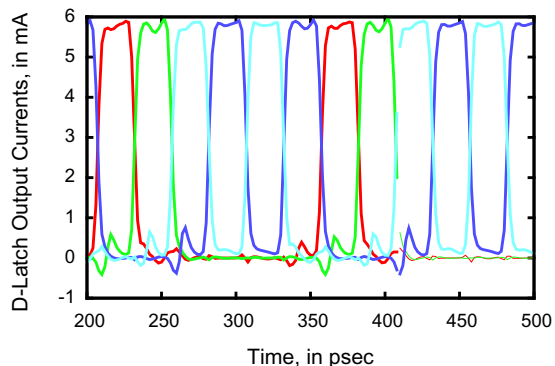


Fig. 6. Simulated D-latch output currents biased at 6mA.

These relations have important implications. Aside from being able to adjust the dampening of the transient currents, the above relations also imply that the translinear switching pair can be oversized or effectively biased at lower current densities, mitigating any self-heating hysteresis effects that often cause deep sub-micron devices to be compromised. Fig. 6. shows the output current(s) of a re-timing D-latch biased at 6mA and driven by translinear differential pair. The absence of overshoot from the translinear pair minimizes the amplitude distortion of the latch. In re-timing circuits such as latches, this is of particular importance given that the transient currents drive a positive feedback loop which requires fast settling time without excessive ringing.

One shortcoming of the proposed architecture is that the base currents used to drive the translinear pairs are subtracted from the currents used to drive the clock line. Fig. 7. illustrates this effect. The resultant waveforms

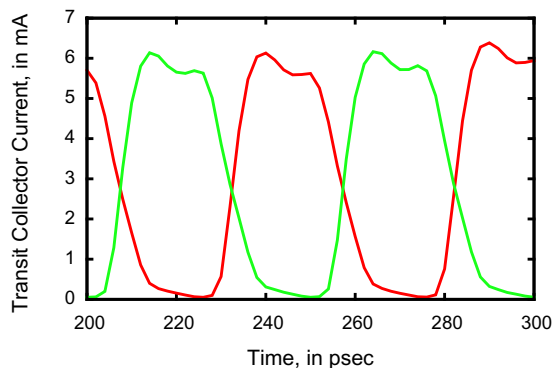


Fig. 7. Simulated cascode collector current following the translinear driving stage.

can be approximated as having fast rising edges but, slower falling edges. However, this distorted waveform can be reconstructed with symmetric edges by inserting a pair of current-switch buffers before the proceeding translinear stage. These buffers also provide adequate propagation delay in order to satisfy the re-timing margin of the two quadrature data paths.

IV. CONCLUSION

In this paper, a re-timing pre-driver for 40Gb/s applications was simulated in a 0.13 μm BiCMOS technology. The re-timer is operated at half-rate which negates the need for peaking inductors, allowing for a compact design. Two data paths operating in quadrature demands an accurate propagation delay budget for optimal re-timing. This is partly achieved but driving the re-timing latches with translinear differential pairs. The use of translinear current switches allows for high-speed switching with negligible overshoot, improving the stability of the re-timer. The high-speed translinear switches can operate at a lower collector current density, preventing possible self-heating effects at higher bias currents. The re-timing predriver design is a potential candidate for burgeoning 40Gb/s architectures.

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