

Monolithic Three-Dimensional Stacking of Integrated Circuits with a Low-Temperature Process

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Abstract—Three-dimensional integration of integrated circuits (3D ICs) seems to be an attractive approach to reduce the interconnect length and decrease power dissipation while increasing the circuit's speed. Two layers of low-temperature fabricated single-grain thin-film transistors (SG TFTs) have been monolithically integrated. NMOS mobilities are 565 and 393 cm^2/Vs and pMOS mobilities are 159 and 141 cm^2/Vs , for the top and bottom layers respectively. A heat simulation using Finite Elements Method (FEM) is performed to investigate the temperature profile of the bottom layer devices during the fabrication of the top layer devices. A three-dimensional (3D) inverter has also been fabricated, with one transistor on the bottom layer and the other on the top layer. The inverters showed an output voltage swing of 0 to 5 V with a switching voltage of around 2 V.

I. INTRODUCTION

Increased length of the interconnects in the current VLSI circuits is becoming the bottle neck for the performance of these systems. Downscaling the transistors allows for higher chip density which requires more interconnects and thus less wire pitch. One solution to these issues is to change the current IC architecture by stacking layers of active devices on top of each other. This can reduce the interconnect length and the RC delay caused by the interconnects. The total device density of the chip increases without any downscaling of the transistors or decreasing the pitch between the devices. Also, the freedom of design offered by three-dimensional (3D) integration can be used for increasing the system-on-panel (SoP) functionalities.

There are different approaches to 3D IC integration: package level [1], wafer level [2] or device level integration [3]. The first two approaches have limited interconnect density between the stacked layers. This limitation is due to the alignment accuracy of about 1 μm between the packages or the wafers. Vertical stacking in device level or monolithic integration will give the largest decrease in interconnect length and highest density of interconnects between the stacked layers. These advantages do not come for free. It is known that in order to make this process successful, some serious technological issues need to be solved. These issues are mainly regarding the thermal management, planarization of the processed layers and obtaining high quality silicon layers and gate dielectric in low-temperature.

There have been reports on monolithic integration [3]. The main issue in this report was the matching of the characteristics, mainly mobility between transistors on different active layers. Insufficient planarization was the main reason for this. Also the high temperature ($\sim 900^\circ\text{C}$) needed to form high quality silicon for the top layers caused degradation in the bottom layers. Another limitation was the usage of single-crystalline Si wafer as seeding the top layer Si growth in other successful reports [4]. This limits the application to microelectronics only and is useless for large area electronics.

High mobility single-grain thin film transistors (SG TFTs) have been reported by our research group in the past. Using the so called μ -Czochralski reported in [5], we crystallize a layer of amorphous silicon (a-Si) into a array of location-controlled single-grain crystalline silicon (SG Si). By designing the channel of the MOS devices inside these grains, we obtain mobilities in the order of 600 cm^2/Vs [6]. The maximum temperature during the fabrication process of SG TFTs is 350 $^\circ\text{C}$ after the low pressure chemical vapor deposition (LPCVD) of a-Si.

These SG TFTs are the perfect candidate for stacked electronics. They can be fabricated using low-temperature process, they do not require seeding for crystal growth and they have high mobilities which is suitable for realizing fast digital [7] and analog [8] circuits.

II. FABRICATION PROCESS

Figure 1 shows the steps of fabrication process. The process flow starts with μ -Czochralski process: location-controlled crystallization of a-Si. Cavities of 700 nm depth and 100 nm diameter are made in 1.5 μm thick SiO_2 on a bulk-Si wafer, using dry etching and successive SiO_2 deposition grown from tetra-ethyl-ortho-silicate (TEOS) [5]. The cavities are filled with 250 nm thick low-pressure chemical vapor deposition (LPCVD) a-Si at 545 $^\circ\text{C}$, implanted a suitable channel doping ($\sim 10^{15} \text{ cm}^{-2}$) and crystallized by means of excimer laser pulses ($\lambda=308 \text{ nm}$, $E=1200 \text{ mJ/cm}^2$).

Islands are patterned in this single-grain silicon and serve as the SG TFT active region. 30 nm thick inductively coupled pressure-enhanced chemical vapor deposition (ICPECVD) oxide is used as gate dielectric, deposited at 250 $^\circ\text{C}$. Next, a

250 nm a-Si is deposited and patterned as gate. Source, drain and gate are implanted ($\sim 10^{18} \text{ cm}^{-2}$) and activated by the excimer laser with energy density of 300 mJ/cm^2 . During this step, the a-Si gate is crystallized into 100 nm large grain poly silicon. Figure 3 shows the surface and the cross-section of a test structure, with an a-Si layer on top of an LPCVD p-silicon layer. After the dopant activation and the annealing step, the grain sizes of these two layers are of the same order of size. The bottom layer is then passivated by 2 μm thick PECVD oxide grown from a TEOS source at 350°C and planarized using CMP. The CMP consist of two major planarizing and smoothening steps in which Rodel ILD1300 with PH of 10.7 is used as a slurry.

Processing the second layer starts also with μ -Czochralski process and follows the same process flow as the bottom layer until planarization. As the planarity of this surface is less crucial, a two step deposition and etch-back of SiO_2 is enough to smooth the sharp steps. The vias connect the bottom layer to the pads and to the top layer contacts. For the common contacts, a part of the active region of the top layer transistor is etched together with its underlying oxide, all the way to the active region of the bottom layer transistor. The interconnects are formed by a 675 nm thick Al, sputtered at 350°C . The maximum process temperature is 350°C after the a-Si LPCVD step.

III. DISCUSSION & RESULTS

Figure 5 shows a TEM picture of a 3D inverter having an nMOS on top of a pMOS. The cross section is made along the gate width. The width of the pMOS is $4.2 \mu\text{m}$, twice of the nMOS. The gate length of both transistors is $1.5 \mu\text{m}$.

A. Electrical Characterization

The important characteristics of the transistors are shown in table I. Figure 8 shows the transfer characteristics of the top and bottom SG TFTs. The transistors have high mobilities, and threshold voltage variation of 0.1 V. A good matching between the characteristics of the top and bottom transistors is observed. The devices suffer from high leakage current ($I_{leakage}$). We believe that lack of Lightly Doped Drain (LDD) structure together with a poor gate patterning which caused over-etching of the islands are the main reasons for this high drain leakage. $I_{leakage}$ is measured at V_{gs} of 2 and -3 V for the p- and nMOS devices, respectively.

TABLE I
THE AVERAGE CHARACTERISTICS OF MOS DEVICES

Type	$\mu [\frac{\text{cm}^2}{\text{Vs}}]$	S [$\frac{\text{mV}}{\text{dec}}$]	V_{th} [V]	$I_{leakage}$ [A]
nMOS Top	565	245	-0.8	5.4×10^{-12}
pMOS Top	159	95	-2.4	2.8×10^{-13}
nMOS Bottom	393	280	-0.6	1.5×10^{-10}
pMOS Bottom	141	151	-2.0	9.2×10^{-13}

Using transistors on each layer, two different configuration of 3D inverters were fabricated: one with and nMOS stacked

on top of a pMOS and vice versa. Two types of 3D inverters are fabricated: n- on pMOS and vice versa. The channel width of the pMOS is chosen to be twice as large as the nMOS, which is roughly the inverse of their mobility relation. The output characteristics of both type are shown in Figure 9. There exist a slight difference in the output current magnitude. However, despite of this difference both inverters show good switching capabilities.

B. Area Advantage

Another important advantage of the 3D integration is the area advantage. There are different ways of integrating devices on top of each other. We have placed the top layer transistors directly on top of the bottom layer transistors. Figure 6 shows the masks of an inverter, which shows the common gate and common drain connection. Also it is clear that a 3D inverter is as big as one transistor and twice smaller than a conventional 2D inverters.

C. Thermal Damage Prediction

During the μ -Czochralski process we irradiate the a-Si with 24 ns long excimer-laser pulses with energies of the order of 1400 mJ/cm^2 . The energy of the laser is absorbed in the first few of nanometers of a-Si layer. This layer is then melted and the heat distributed equally through its hole depth. This film serves as the heat source in the heat simulation using FEM. The temperature of the film rises to 2200 K and decays to ambient during 400 ns. The coefficients used in the simulation are reported in [9]. Figure 7(a) shows the schematic of layers that includes the bottom layer transistor and ILD with 1.6 μm thickness and top layer a-Si with 250 nm thickness.

Figure 7(b) shows the temperature profile of the structure against time. The ambient temperature is 650 K, which is due to the heated chuck of the laser during the crystallization. It is shown that the maximum temperature of the bottom transistor (its gate) reaches to 1000 K at 1 μs after the irradiation. We can calculate the boron diffusion in this temperature using

$$L = \sqrt{D * t}$$

in which L is the length in cm, D the diffusivity coefficient and t is the time. Diffusivity is the conventional value as we do not melt the silicon. We assume that the bottom layer stayed for 100 μs at its maximum temperature of 1000 K. That will give a diffusion length of the order of 10^{-24} m. With other words, no thermal damage to the bottom layer devices are expected.

IV. SUMMARY

SG TFTs are suitable candidates for 3D monolithic stacking. They can be fabricated using temperatures below 350°C and have high mobilities of around $600 \text{ cm}^2/\text{Vs}$. The main issues regarding monolithic stacking are planarization of the first layer and processing in low temperature. One thermal critical step in the process flow is the crystallization of the active area of the top layer devices. With a heat simulation using FEM, we showed that there exists no thermal damage to the bottom layer transistors during the crystallization of the top layer devices.

The matching between the characteristics between devices in both layers confirms that. The characteristics of devices were shown. Top layer mobilities are 159 and 565 cm^2/Vs and bottom layer mobilities are 141 and 393 cm^2/Vs , for the pMOS and nMOS devices respectively. Two configurations of 3D inverters were fabricated using these high mobility devices. These Inverters showed good switching capabilities and an output voltage swing from 0 to 5 V.

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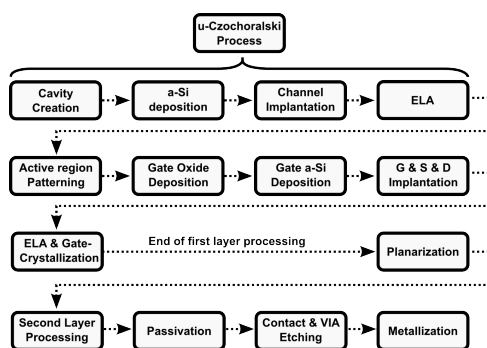


Fig. 1. This diagram shows the different steps of fabrication process flow

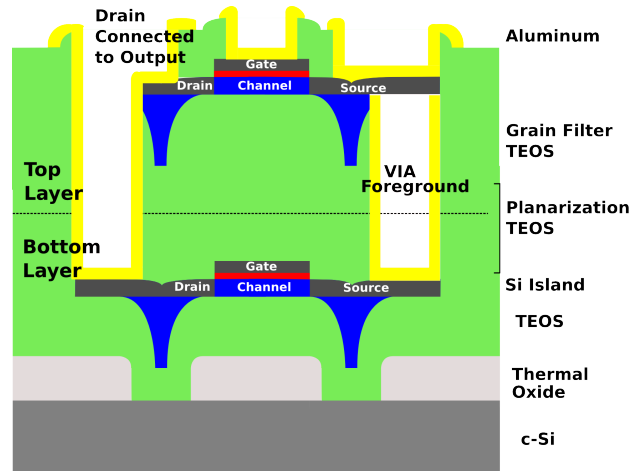
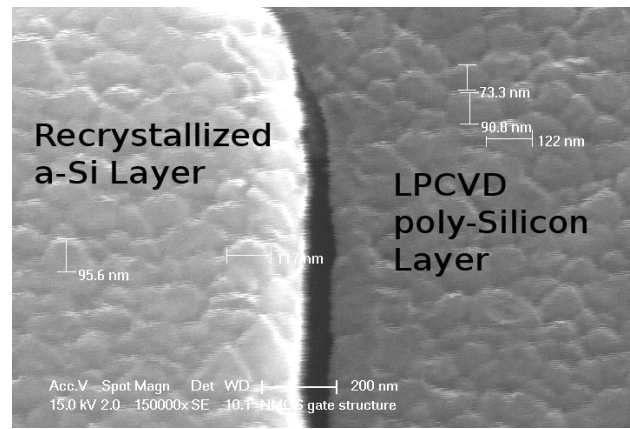
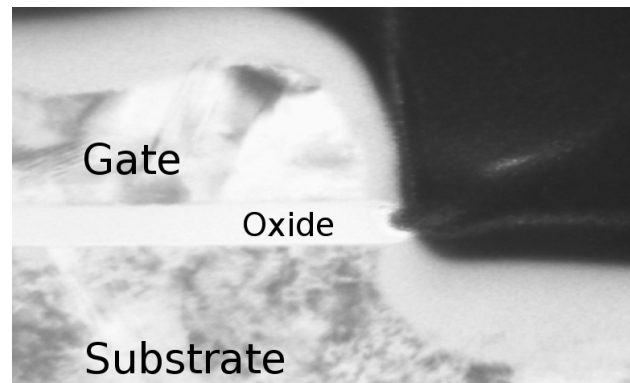


Fig. 2. The 2D schematics of a 3D inverter showing the stack of the layers, position of the grains and common connections between the drains of the transistors on each layer



(a)



(b)

Fig. 3. Figure 3(a) shows the SEM picture of the surface of a crystallized a-Si on top of a p-Si layer as means of comparison; Figure 3(b) shows the origin of the grains being the interface of SiO₂ and recrystallized a-Si

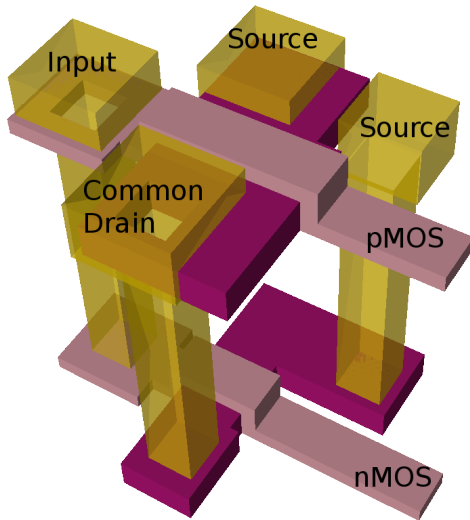


Fig. 4. The schematics of a 3D inverter with a pMOS on the top and an nMOS on the bottom layer

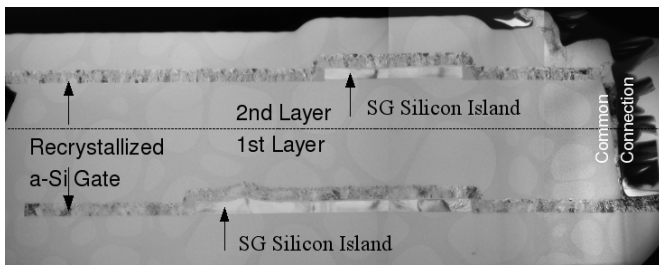


Fig. 5. The TEM picture of a 3D inverter with an nMOS on the top and a pMOS on the bottom layer

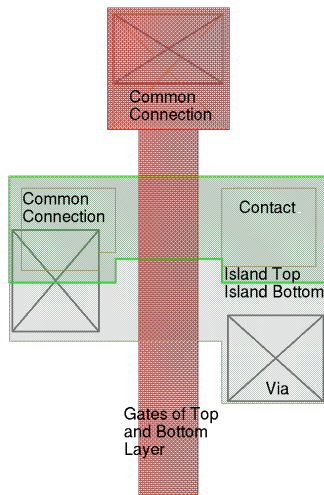
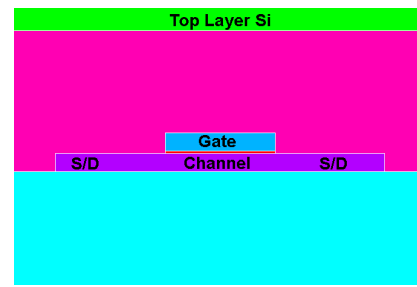
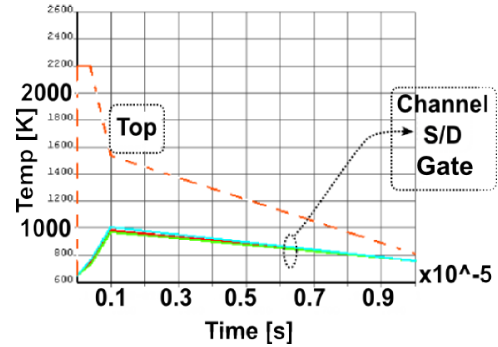


Fig. 6. The layout of a 3D inverter showing the area advantage obtained by stacking two transistors on top of each other

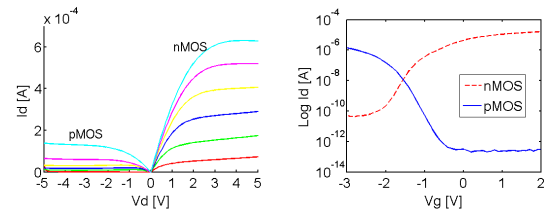


(a)



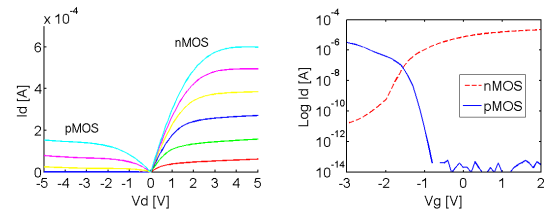
(b)

Fig. 7. 7(a) Shows the schematic structure of the simulated structure and 7(b) shows the temperature profile of the key points shown in 7(a)



(a)

(b)



(c)

(d)

Fig. 8. 8(a) and 8(b) show I_D-V_D and I_D-V_G characteristics of the bottom and 8(c) and 8(d) show I_D-V_D and I_D-V_G characteristics of the top layer transistors

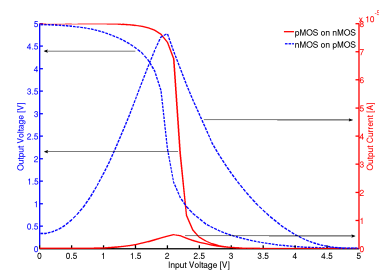


Fig. 9. The output characteristics of a p- on nMOS and an n- on pMOS inverters