

# Ultra-low Power Transmitters for UWB-FM Sensor Networks

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**Abstract**— Smart integrated systems for wireless sensor networks require ultra-low power transceivers integrated together with sensors, digital signal processing, and antennas. These sensor networks target low data rate applications of less than 100kbits/s over a distance of less than 100 m. The transmitter uses ultra-wideband FM modulation scheme for the 3.1 to 5.1 GHz range, in order to take advantage of the UWB low power transmit power requirements and ease design specifications. For such a transmitter, a total power consumption is in the order of  $\mu$ Ws. This paper studies different VCO topologies, such as the ring and LC oscillators to comply with the ultra-low power requirement. Performance comparisons are made and trade-offs between each architecture are highlighted.

**Index Terms**—ultra-low power, ultra-wideband transmitter, wideband-FM, VCO

## I. INTRODUCTION

Smart systems integration (SSI) targeting the wireless sensor networks (WSN) market have received a great deal of attention in recent years. These are highly integrated, ultra-low power, and low cost systems. Applications range from body area sensor networks (WBAN), such as for health monitoring using wearable biomedical implants, to environment, security and automotive monitoring, and wireless personal area networks (WPAN) or “smart dust” [1], [2]. These rely on a short range communication distance (less than 100 m) and low data rates (less than 100 kbits/s), as well as a light weight and a small size ( $< 1 \text{ cm}^3$ ). These smart systems have a long lifetime ( $> 5$  years) requiring an average power of a few  $\mu$ Ws, as sensor networks are mainly idle, using in the order of or less than 1% of duty cycling. Hence, the ultra-low power functionality enables the use of a one-time charged battery or energy scavenging [3].

These new market products require an embedded system design where integration of all functions of a wireless system, as shown in Fig. 1, includes the antenna, the radio transceiver, the digital circuitry for the processor, analog-to-digital converter (ADC), and memory storage, the sensor, power

management which includes the power generator and the power supply unit, and packaging. The radio circuitry consumes most of the system power.

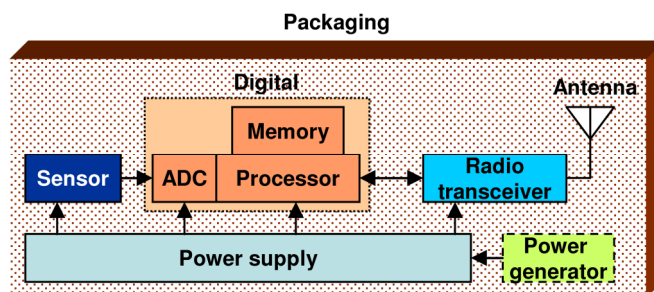


Fig. 1. Wireless sensor node system components.

In order to achieve a low power requirement, the ultra-wideband scheme was chosen, using an FM modulation (UWB-FM). The Federal Communications Commission (FCC) defined a UWB transmit power spectral density (PSD) of  $-41.3 \text{ dBm/MHz}$  over a band of 500 MHz or wider, in the 3.1 to 10.6 GHz frequency range [4]. This paper focuses on the 3.1 to 5.1 GHz frequency range with transmitter bands of 500 MHz. A sub-micron (90 nm) CMOS process technology is used, in order to lower the supply voltage to less than 1.2 V and taking the advantage of a 160 GHz transit frequency characteristic, thus maximizing the power efficiency.

In Section II, the advantages of the UWB-FM architecture are highlighted and a UWB-FM transmitter architecture is proposed. In Section III, the transmitter requirements are presented in terms of energy and transmitter specifications. Section III studies two different voltage-controlled oscillator (VCO) topologies: the ring and LC VCOs along with the antenna. Section IV compares the performance of these different topologies and discusses the trade-offs.

## II. UWB-FM ARCHITECTURE

### A. UWB-FM Characteristics

Originally, UWB started as an impulse radio, using a time-domain approach [5]. Instead of a continuous sinusoidal carrier, a sequence of short-duration pulses is used as the information carrier. The spectrum of such a pulse sequence

(usually Gaussian) has a single broad main lobe with slow spectral roll-off. An impulse radio may be able to provide a robust high data rate solution, but this comes at the expense of circuit complexity and power consumption.

The UWB-FM is based on a constant-envelope frequency domain approach, suitable for low and medium data rates (LDR and MDR) [6]. The UWB-FM system is easy to implement in silicon, provides robustness to interference compared to narrowband ISM solutions, and has been shown to be competitive in terms of power consumption. In this paper, we present a transmitter design suitable for WSN.

UWB-FM can be seen as an analog implementation of a spread-spectrum system with a spreading gain equal to the modulation index  $\beta$ . FM has the unique property that the RF bandwidth  $B_{RF}$  is not only related to the bandwidth  $f_m$  of the modulating signal, but also to the modulation index  $\beta$  that can be chosen freely, as approximated by Carson's rule:

$$B_{RF} \approx 2(\beta+1)f_m = 2(\Delta f + f_m) \quad (1)$$

where  $\Delta f$  is the frequency deviation defined by  $\beta = \Delta f / f_m$ .

This yields either a bandwidth-efficient narrowband FM signal ( $\beta < 1$ ) or a (ultra-) wideband signal ( $\beta \gg 1$ ) that can occupy any required bandwidth compatible with the RF oscillator's tuning range, where no carrier can be distinguished. Hence, the bandwidth of a wideband FM signal can be controlled by adapting  $\beta$ . The spectral roll-off of this UWB-FM signal is very steep. This strongly improves the coexistence of UWB-FM systems with other RF systems operating in adjacent frequency bands.

### B. UWB-FM Transmitter

Figure 2 shows the architecture block diagram of the proposed UWB-FM transmitter. The data signal coming from the sensor has been lowpass filtered and digitized by the ADC. It is then modulated by a frequency subcarrier using FSK techniques in the range of a few MHz. A triangular shape FSK modulated subcarrier then FM modulates the RF oscillator, which provides a flat spectrum across the frequency band, in the GHz range. This double FM scheme uses low modulation index FSK followed by high-modulation index analog FM to achieve the wide bandwidth. Different users distinguish themselves by different subcarrier frequencies. The FM output signal provided by the VCO is buffered or fed to a low power amplifier (PA) in order to isolate signals from the antenna and provide a low impedance match to an antenna. Since a specific UWB band must be selected, the VCO must be tuned

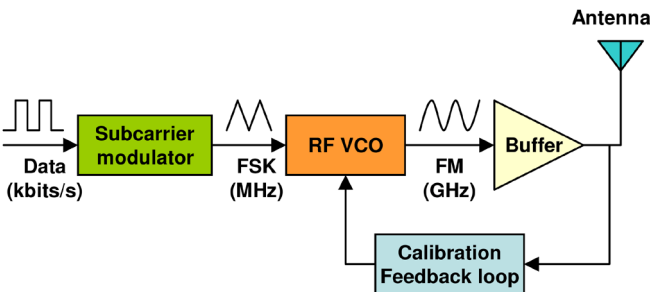


Fig. 2. UWB-FM transmitter architecture.

accordingly to provide the wanted frequency spectrum bandwidth. Hence, a calibration set-up is needed, such as a phase-lock loop. In this paper, only the front-end consisting of the RF VCO, buffer, and antenna are presented.

## III. TRANSMITTER REQUIREMENTS

### A. Energy per bit

Monitoring the energy consumed per transmitted bit is an important factor in the system design in order to use energy scavenging, solar energy, or low power batteries.

A wireless transmitter can be modeled as a PA or buffer, as in Fig. 2, and a pre-PA block that represents all the circuits prior to the PA. In WSN applications, the transmitter is duty cycled; it wakes up, transmits the data and then returns to sleep or an idle state before the next transmission. This is quantified by the energy per bit ( $E_{bit}$ ), assuming the PA is off just before transmitting:

$$E_{bit} = \frac{T_{up} \cdot P_{tx} + (P_{tx} + P_{out} / \eta_{PA}) \cdot T_{on}}{Bd} \quad (2)$$

where  $T_{up}$  is the start-up time required for the transmitter to power up,  $P_{tx}$ , the transmitter DC power consumption without a front-end power amplifier,  $P_{out}$ , the transmitted radiated output power,  $\eta_{PA}$ , the power amplifier efficiency,  $T_{on}$ , the time the transmitter is on for transmitting data, and  $Bd$ , the number of data bits in a packet. The average energy per bit is defined as:

$$E_{avg} = \frac{(E_{bit} + P_{sleep})}{T_{bt}} \quad (3)$$

where  $P_{sleep}$  is the power consumption when the transmitter is in sleep mode times the time during which it remains in sleep state, and  $T_{bt}$  is the time between two transmissions data packets.

For low data rates less than 100 kbits/s, the start-up time of the transmitter does not play a significant role in the energy consumption. Hence, the design must focus on minimizing the power consumption of the overall transmitter and maximizing the power efficiency. Moreover, for small packet sizes, the protocol must use a minimum of overhead bits.

Considering a button cell battery of 250 mWh of 1 cm diameter and with a 1% duty cycling, a maximum of 500  $\mu$ W of circuitry active power will ensure more than 5 years of battery lifetime. Hence, with a transmitter DC power consumption of less than 500  $\mu$ W, an  $E_{bit}$  of a few nJ/bit at a data rate of 100 kbits/s is required.

### B. Transmitter Specifications

The total transmitter power consumption must be less than 500  $\mu$ W, as defined previously. Digital circuits consume about 100  $\mu$ W. The main power contributors are the VCO and the calibration feedback loop circuits. If a PLL is used, the frequency divider is the most power-hungry device. Therefore, about 200  $\mu$ W is set for each RF circuit. The UWB defines a maximum PSD of -41.3 dBm/MHz, equivalent to a -14.3 dBm or 37  $\mu$ W radiated power signal over a 500 MHz band. This translates into a 120 mVpk-pk output voltage swing in a 50  $\Omega$

TABLE I  
RF TRANSMITTER SPECIFICATIONS

Parameter	Value
Operational bandwidth	3 – 5 GHz, 500 MHz min.
DC power	400 $\mu$ W, 200 – 300 $\mu$ W for VCO
Output radiated power	-14.3 dBm max. over 500 MHz
Amplitude response	Flat over band
VCO phase noise	-80 dBc/Hz at 1 MHz offset
Isolation from antenna	10 dB min.
Start-up time	< 100 $\mu$ s
Harmonic rejection	10 dB min.
Total size	< 1 cm <sup>3</sup>
Die area	< 1 mm x 1 mm
Voltage supply	< 1.2 V

load, if the antenna has 100% radiation efficiency. Since an FM signal is transmitted, phase noise requirements for the VCO are relaxed (typically -80 dBc/Hz at 1 MHz offset). The RF transmitter specifications are summarized in Table I.

#### IV. TRANSMITTER DESIGNS

Two different transmitter front-end topologies are proposed. One is based on a single-ended design using a ring oscillator, whereas the second relies on a differential circuit topology using an LC oscillator.

In order to minimize the power consumption, low power techniques may be used, such as lowering the transistor threshold voltage by increasing the gate length and varying the body biasing voltage, and using subthreshold operating devices. Operating the devices below the threshold voltage also lowers the operating frequency. For frequencies below 10 GHz, the subthreshold technique can be used.

##### A. Ring VCO Design

A ring oscillator consists of N-stage cascading identical CMOS inverters in a closed loop, requiring both positive and negative feedback to operate properly. Negative feedback is needed under DC conditions to allow the ring to self-bias, such that each inverter of the ring is being quiescent biased in its high gain region, i.e.  $\sim V_{DD}/2$ , where  $V_{DD}$  is the supply voltage. On the other hand, positive feedback occurs as the phase shift of each stage increases with frequency. When the total phase shift around the closed loop reaches  $360^\circ$  and if the gain is greater than unity, the circuit oscillates. The frequency of oscillation is given by:

$$f_{ring} = \frac{1}{2N\tau} \quad (4)$$

where  $\tau$  is the average propagation delay of the inverter, consisting of the sum of its switching rise and fall time.

Hence, the oscillation frequency becomes:

$$f_{ring} \approx \frac{W}{2L} \frac{\mu_{eff} C'_{ox} (V_{DD} - V_T)^2}{2NCV_{DD}} \quad (5)$$

where  $W$  and  $L$  are the gate width and length,  $\mu_{eff}$  the effective mobility of electrons or holes,  $C'_{ox}$  the gate oxide capacitance,  $V_T$ , the threshold voltage, and  $C$ , the total input and output capacitances seen by an inverter stage. The average

dynamic power consumption  $P$  of an inverter stage is:

$$P = C \cdot V_{DD}^2 \cdot f_{ring} \quad (6)$$

In order to obtain a frequency of oscillation as high as in the 5 GHz range, three inverter stages and the minimum gate length are chosen, and  $V_{DD}$  must be 1V minimum. On the other hand, to minimize the power consumption,  $V_{DD}$  must be kept as low as possible. In this 90 nm CMOS technology,  $V_T$  is around 500 mV. Biasing the inverter gate at 1 V implies that the MOSFETs are in the transition region between weak (triode) and strong inversion (saturation) modes.

The principle of tuning in this circuit is based on the current-starved technique, as shown in Fig. 3. NMOS & PMOS biasing gates are in deep triode region. The biasing circuit consists of a current mirror and a control voltage ( $V_{CTL}$ ) providing a gate bias for an NMOS in deep triode such that its resistance is varied. This results in a variation in the gate voltage biasing and current used for each inverter cell for varying the frequency of oscillation.

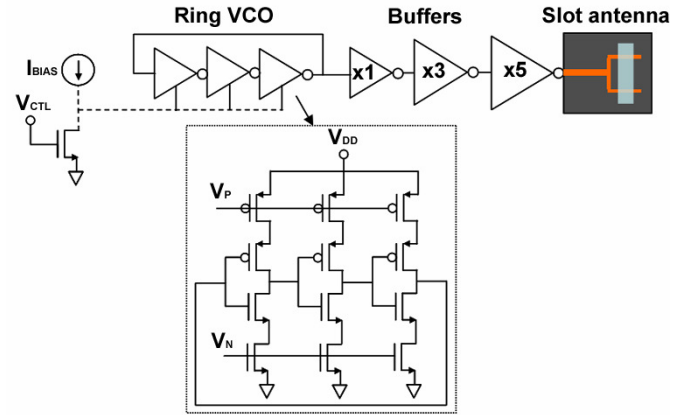


Fig. 3. Ring VCO schematic diagram.

Theoretically, a swing of  $V_{DD}$  is seen at the output of the VCO core, with a quasi-square signal shape. A three stage inverter buffer is chosen such that output loading due to the antenna is minimized. Moreover, the first inverter buffer adds another output capacitance, mainly  $C_{GS}$  of the NMOS. The resulting oscillation frequency decreases by several hundreds of MHz. In order to attain a transmit output power in the range of  $\mu$ Ws, a total buffer biasing power of 170  $\mu$ W is needed. These output buffers are the power bottleneck for the ring oscillator topology. The biasing circuitry is biased at 0.4 V and consumes a total of 5 to 37  $\mu$ W, whereas the VCO core consumes a total of 30 to 50  $\mu$ W, from 3.1 to 5.1 GHz. Hence, the maximum DC power consumption is 250  $\mu$ W.

The ring VCO is also prone to supply, temperature, and process variations. A 10% variation in VCO supply voltage gives about 1 GHz of frequency variation. The maximum phase noise is -80 dBc/Hz at 1 MHz, which is compliant with the specification. The oscillation frequency is shown in Fig. 4. It gives more than 2 GHz tuning range with a control voltage varying from 0.2 V to 0.4 V. The frequency curve is not a linear function since it actually follows the way the biasing circuit behaves. For  $V_{CTL}$  below 0.3 V, some MOSFETs in the

biasing circuit operate in the triode region, whereas above 0.4 V, they operate in the saturation region. This is reflected in the frequency behavior.

The antenna would be attached to the output buffer via flip chip. A broadband (3-5 GHz) antenna bandwidth is chosen, such as the one proposed by Klemm [7], which consists of a slot antenna backed by a reflector, presenting a real input impedance of about 50  $\Omega$ . The antenna has a front-to-back ratio of more than 10 dB, a radiation efficiency of 50 to 80%, and a gain of 7 to 8 dBi. An approximate model of the antenna is extracted in terms of transmission line equivalent circuit.

A resulting transmit output power seen at the antenna is obtained, ranging from 6  $\mu$ W (3.1 GHz) to 38  $\mu$ W (5.1 GHz). The output signal has a sinusoidal shape, having more than 15 dB harmonic rejection. A maximum of 15% efficiency is obtained at 5 GHz, as seen in Fig. 4. Further investigations are needed in order to apply a more efficient biasing network, output buffers, and antenna match. Since the ring VCO does not have any passive elements, its chip area remains very small (< 300  $\mu$ m x 300  $\mu$ m).

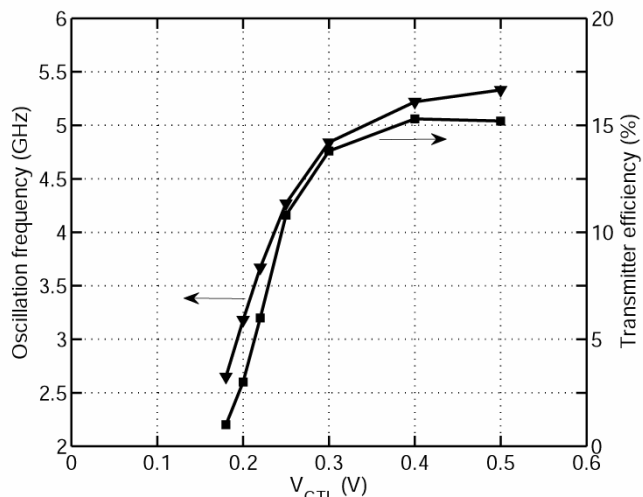


Fig. 4. Ring VCO oscillation frequency and efficiency vs.  $V_{CTL}$ .

### B. LC VCO Design

A differential LC oscillator, based on a Class-C operation, was chosen. The differential topology avoids common-mode noise and increases the output voltage swing, while providing a lower phase noise. The proposed LC VCO schematic diagram is shown in Fig. 5. It consists of a cross-coupled NMOS pair, M1 and M2, with a separate gate biasing voltage  $V_B$  that provides the bias switching needed in Class-C operation. The LC tank consists of the primary winding of transformer T1, NMOS varactor Cv1, and other parasitic capacitances. Common gate NMOS buffers M3 and M4 are in cascode with the core VCO, connected through the transformer RF ground connection, providing isolation from the antenna to the VCO LC tank. The transformer couples the VCO signal through its secondary winding. The supply voltage  $V_{DD}$  drives both M3 and M4 and the same current flows in a branch. This configuration minimizes the power consumption and

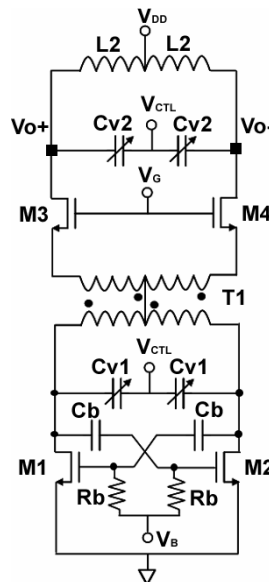


Fig. 5. LC VCO schematic diagram.

eliminates the need of a current source. L2 and Cv2 also form an LC tank used to tune the buffer output gain to the oscillation frequency. Both varactors Cv1 and Cv2 are tuned with the same control voltage  $V_{CTL}$ . In this paper, inductor L2 has been replaced by a small loop antenna, thus eliminating the need of a matching network to a lower impedance antenna. The VCO chip can then be directly flip chip bonded to the loop antenna ports.

In order to lower the supply voltage, NMOS gate lengths of 0.2  $\mu$ m are chosen. The threshold voltage decreases to about 350 mV. For the VCO transistors M1 and M2 to operate at the verge of threshold,  $V_B$  is chosen to be 330 mV, and  $V_G$ , 0.7 V. Regardless of the supply voltage  $V_{DD}$ , the biasing of the core transistors M1 and M2 are maintained about constant and does not affect the oscillation operation. Hence, a low  $V_{DD}$  of 0.4 V is selected. But, in this case, M3 and M4 buffers operate in the triode region, providing only 10 dB of isolation. A total current of 415  $\mu$ A is consumed, which translates in a 166  $\mu$ W total DC power consumption. Transformer T1 has a 4:3 turns ratio and measures 300  $\mu$ m x 300  $\mu$ m. The primary winding inductance is 3.8 nH and coupling factor K is 0.75. A differentially symmetric layout using thick top metal is used. A maximum differential quality factor of 8 is obtained at 5 GHz. An equivalent circuit of the transformer is extracted and used in the circuit simulator [8]. The NMOS varactor Cv1 is chosen such as to give a bandwidth of at least 500 MHz. The loop antenna is fabricated on an FR-4 substrate and measures 5 mm in diameter. Its equivalent circuit is extracted, resulting in an inductance of 5.1 nH. The radiation efficiency ranges from 10% to 45%, and its gain, from -15 dBi to 4dBi, at 3 GHz and 5 GHz, respectively.

The oscillation frequency is shown in Fig. 6. It gives more than 800 MHz tuning range with a control voltage varying from 0 V to 0.4 V. The frequency curve is almost a linear function for  $V_{CTL}$  up to 0.3 V. A resulting transmit output power seen at the antenna is obtained, ranging from 30  $\mu$ W

(3.6 GHz) to 41  $\mu$ W (4.1 GHz). The output signal has more than 40 dB harmonic rejection. The transmitter efficiency seen at the input of the antenna ranges from 18% to 25%, as seen in Fig. 6. Considering the small loop antenna low radiation efficiency, the total radiated power decreases and a total transmitter efficiency of 7.5% is obtained. Since the LC VCO uses a monolithic transformer, its chip area consumption is bigger ( $\geq 500 \mu\text{m} \times 500 \mu\text{m}$ ).

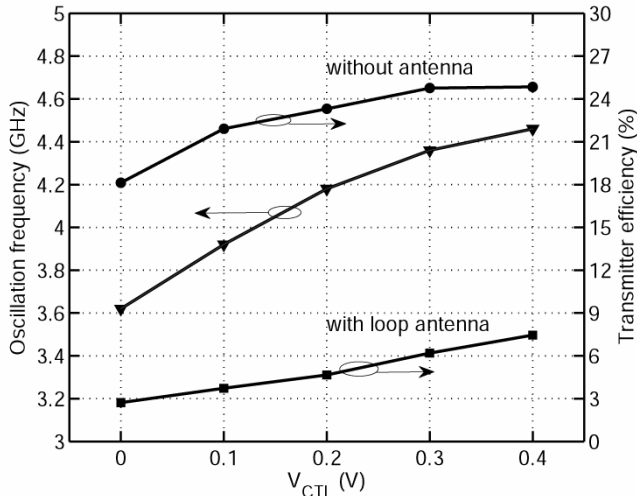


Fig. 6. LC VCO oscillation frequency and efficiency vs.  $V_{CTL}$ .

## V. TRANSMITTER COMPARISONS

The two RF VCO transmitter configurations are compared in Table II. The ring VCO provides a larger frequency bandwidth, but its efficiency is lower than for the LC VCO. For the ring VCO, a slot antenna with high gain and unidirectional radiation is used, but its physical size is in the order of 3 cm x 3 cm. The amplitude response over the frequency range is not flat, but increases with frequency. The ring VCO has a higher phase noise than the LC VCO, remaining compliant with the UWB-FM scheme. In the LC VCO configuration, a small loop antenna is used, but its radiation efficiency is too. Further studies are needed in order to optimize both VCO performances and antenna designs. A rough estimate of the *Ebit* at 100 kbits/s is given, lying in the nJ/bit range.

## VI. CONCLUSION

This paper studied two VCO topologies for ultra-low power UWB-FM sensor network transmitters, integrated with an antenna. For UWB-FM, the phase noise requirement is relaxed. Hence, the ring VCO is suitable for wide frequency ranges, whereas the LC VCO enables the use of low supply voltage and near subthreshold operation. Other antenna designs must be investigated for higher radiation efficiency while maintaining a small size.

TABLE II  
RF VCO TRANSMITTER COMPARISONS

Parameter	Ring VCO	LC VCO
Frequency (GHz)	2.6 – 5.3	3.6 – 4.4
Supply voltage (V)	1	0.4
DC power	200 - 250 $\mu$ W	166 $\mu$ W
Output radiated power	-15 dBm max.	-19 dBm max.
Transmitter efficiency	2 - 15%	18 – 24% (w/o ant.) 3 – 7.5% (loop ant.)
<i>Ebit</i> at 100 kbits/s	> 3.1 nJ/bit	> 2 nJ/bit
Amplitude response	Not flat	Not flat
VCO phase noise at 1 MHz offset	< -80 dBc/Hz	< -100 dBc/Hz
Isolation (dB)	> 10	10
Harmonic rejection	15 dB	40 dB
Die area	< 300 $\mu\text{m} \times 300 \mu\text{m}$	< 500 $\mu\text{m} \times 500 \mu\text{m}$
Total size	~3 cm x 3 cm x 1 cm	1 cm x 1 cm x 1 mm

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