

A 4 bit 10 GS/s Flash ADC frontend in SiGe technology with very low power consumption

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Abstract—The work on hand demonstrates the feasibility of high sampling frequency (10 GS/s), high input bandwidth (5 GHz) but yet low power consuming (50 mW from -2.5 V supply) flash ADC frontend in SiGe bipolar technology. This is accomplished by employing a differential emitter follower (EF) incorporating a resistor ladder (which supersedes a dedicated reference ladder) and by applying a new latch architecture with active load.

Index Terms—Flash ADC, SiGe technology, latch with active load, high speed, low power consumption.

I. INTRODUCTION

INTEGRATED circuits realized in SiGe-bipolar technologies have a reputation for operating at very high speed (e.g. 100 Gbit/s [1]) but being very power consuming whereas circuits in the latest CMOS technologies are expected to operate at only somewhat lower speed (e.g. 60 Gbit/s [2]) but to consume significantly less power. The low power consumption for CMOS technologies is true as long as the circuits apply a Complementary-MOS topology and the operation speed is low enough to benefit from the inherent negligible static power consumption.

However, at medium speeds (e.g. 10 Gbit/s) the Complementary-MOS topology has a poor electrical performance and, therefore, needs to be replaced by a differentially operated symmetrical circuit topology like the Current Mode Logic (CML). Such a topology offers a vast variety of advantages (e.g. virtual ground, TML matching, cell based design, [1, 3]) if the design strictly obeys the complex conjugate impedance mismatch concept at interfaces between adjacent transistor stages. Optimizing such CML circuits for speed requires improving the mismatch at the transistor stage interfaces. Here, the bipolar transistor benefits from its well known inherent advantage owing to his comparatively high transconductance (g_m). On the other hand, if operation at maximum speed is not required, the high speed potential can be traded for low power consumption. If this trade-off is applied to a state-of-the-art SiGe bipolar technology (f_T , f_{max} about 200 GHz), which can reach maximum operating speeds of about 100 Gbit/s, high performing circuits with moderate speed (e.g. 10 Gbit/s) and very low power consumption can be realized. This changes the paradigm of power consuming bipolar designs. The full low power potential of SiGe bipolar

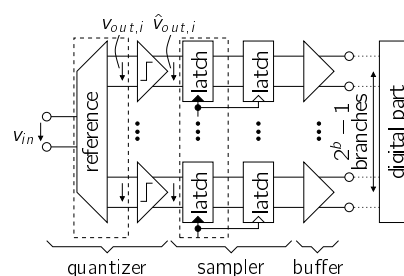


Fig. 1. Block diagram of $b = 4$ bit flash ADC frontend. Examined in detail are the quantizer (Sec. II)- and sampler (Sec. III) block.

technology can be further exhausted if transistor models (e.g. HICUM) are used in circuit simulation that allow for transistor optimization in the high current- and the V_{CE} saturation area.

The aforementioned low power potential is demonstrated by the simulation results of the low power 4 bit 10 GS/s flash ADC frontend in pure SiGe bipolar technology shown in the block diagram in Fig. 1. The ADC frontend employs a differential emitter follower (EF) stage followed by a resistor ladder which drives 15 comparator stages in parallel (quantizer block). This architecture, its advantages and performance limitations as signal delay along the ladder and load currents drawn from the ladder are identified, detailed, and assessed in Sec. II. In order to assess the performance of the latches (sampling block), new figures of merit are introduced and optimization-methods are proposed. These figures of merit incorporate both the eye opening and the polarity of the latch output signal. It is shown in Sec. III that the standard latch architecture comprising a tracking current switch pair (CS) and a cross coupled latching current switch pair mainly suffers from the RC time constant at the output node. The improvement with respect to the aforementioned figures of merit due to employing a transimpedance stage instead of the load resistors is presented. The simulation results of this ADC frontend are in Sec. IV compared with measurement results of an ADC realized in a state-of-the-art CMOS technology. This paper closes with the conclusion in Sec. V.

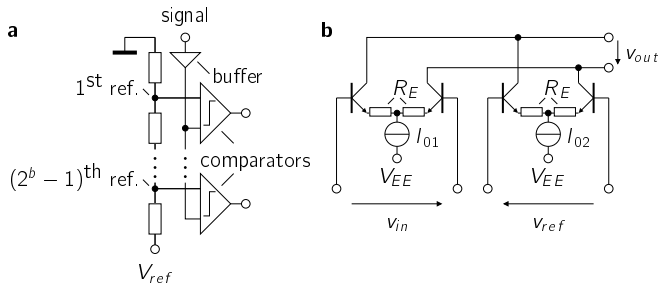


Fig. 2. a) Typical single ended b bit flash ADC topology with resistor ladder and signal buffer. b) Differential comparator consisting of two (linear) current switches with differential input voltage v_{in} and differential reference voltage v_{ref} .

II. LOW POWER QUANTIZER

A. Ordinary flash architecture

In typical (single ended) ADC flash topologies [4] following the principle shown in Fig. 2.a), each comparator is fed by a dedicated reference signal and a data signal common to all comparators. The buffer employed here distributes the data signal to all comparators and decouples their inputs from the signal source output. The reference voltage levels can for example be generated by a resistor ladder. This topology has the inherent disadvantage of requiring currents to generate the reference levels in the resistor ladder *and* currents for the input signal buffer(s). Moreover, if the ADC shall convert differential signals, not only the reference- and buffer currents double but also comparators have to consist of at least two current switches (one for the data signal, one for the reference level, see Fig. 2.b). The output currents of these current switches (CS) sum in the common collector branches and thus generate a *differential* output current. This differential output current must have the same sign as the difference $v_{sig} - v_{ref}$ of the signal voltage v_{sig} and the reference voltage v_{ref} in order to cause a voltage drop at a load (not shown in Fig. 2.b) representing the comparator decision. The output currents of both CS therefore have to linearly depend on their respective input voltage, which is accomplished by adjusting their linear range large enough to cover the entire input voltage dynamic range. The linear range of a CS is bounded by the *knee voltage* [5]

$$V_K = I_0 \cdot (R_E + r_E + r_B/\beta_0) + 2V_T, \quad (1)$$

where R_E is the emitter degeneration resistance, r_E is the emitter contact resistance, r_B is the base resistance, β_0 is the DC current gain and V_T is the temperature voltage of one transistor of the CS; I_0 is the tail current of the CS. For input voltages v_{in} above that threshold, the linearized transfer curve $i_{out}(v_{in})$ reaches saturation of the output current $i_{out} = I_0$. From (1) it becomes obvious that a large dynamic range demands for high comparator tail currents I_{01} , I_{02} as the emitter degeneration resistance R_E is limited by layout capacitances. As this increases the power consumption of the ADC frontend significantly ($2^b - 1$ comparators), a more power saving architecture is proposed in the following section.

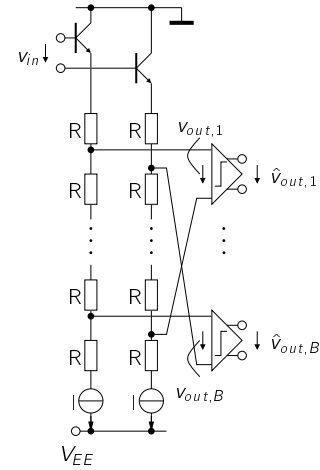


Fig. 3. Enhanced b bit quantizer which simultaneously buffers the input signal, performs the comparison with $B = 2^b - 1$ reference levels and distributes the result of the comparison to succeeding stages (e.g. latches).

B. Transfer characteristics of enhanced quantizer

In the enhanced architecture of Fig. 3, the differential output voltage $v_{out,i}$ at each tap of the ladder represents already the result of the comparison of the input voltage v_{in} with the i^{th} reference level:

$$v_{out,i} = v_{in} - (i - 2^{b-1}) \cdot V_{LSB}, \quad (2)$$

where $V_{LSB} = 2RI$ is the quantization step size given by the tap resistance R and the EF tail current I . Therefore, the comparators shown in Fig. 3 consist of ordinary current switches (CS) without requirement for linearity instead. Moreover, the emitter followers decouple and distribute the signal from the source to all comparators, which supersedes a dedicated buffer stage.

Because of capacitive loading C of the taps (resistor capacitance, input capacitance of comparators, layout capacitances of interconnects thereof), signals are delayed along the resistor ladder. As the signal and the complementary signal pass through different counts of RC lowpasses in that particular ladder architecture, they exhibit different phase shifts and are not opposite in phase. Hence, the differential amplitude of tap voltages $v_{out,i}$ is decreased with respect to the input voltage v_{in} . In order to estimate the influence thereof, an ideal AD-DA conversion simulation environment which takes propagation delays in the reference ladder into account is set up in the following. In step 1 the signal propagation delays are determined and used to compute the respective tap voltages. In step 2, the behavior of the comparators of Fig. 3 is modeled. In step 3, the thermometer code constituted by the comparator output voltages $\hat{v}_{out,i}$ is ideally DA converted. In step 4, commonly used performance metrics such as ENOB, THD, SFDR etc. are computed in order to assess the influence of propagation delay in the reference ladder.

- 1) Each emitter follower with resistor ladder is modeled by a chain of RC elements as shown in Fig. 4 (single ended voltages are marked with an apostrophe '). The input EF

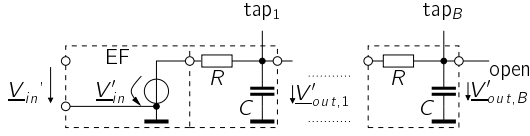


Fig. 4. Ideal voltage buffer and chain of B RC lowpasses as a simple model of input emitter follower (EF) with resistor ladder.

is modeled as an ideal unity voltage gain buffer, the EF bias current source I is considered as open circuit for signal frequencies. The input impedance of any tap is dominated by the capacitance as $|j2\pi fC|^{-1} \approx 300R$ at $f = 5$ GHz, $C = 20$ fF, and $R = 5 \Omega$. Therefore, the i^{th} tap is a lowpass with capacitance $(B - (i - 1))C$, where $B = 2^b - 1$ is the number of reference levels (taps), i.e. all taps to the right hand side of tap i are reduced to their capacitance. The voltage transfer function $\underline{H}_i = \frac{V'_{out,i}}{V'_{in}}$ from the input to the i^{th} tap is then given by the product of transfer functions of each of the first i taps:

$$\underline{H}_i \approx \prod_{k=1}^{B-(i-1)} \frac{1}{1 + j2\pi f(kC)R}. \quad (3)$$

(3) can be simplified further by neglecting all addends containing higher order powers of $2\pi fCR \approx 0.003$. It follows

$$\underline{H}_i \approx \frac{1}{1 + j2\pi i \left(B - \frac{i-1}{2}\right) CR}. \quad (4)$$

The signal propagation delay between the input of the EF and the i^{th} tap is then for monofrequent signals given by the phase $\text{arc}(\underline{H}_i)$. For a sinusoidal input voltage $v'_{in} = \frac{A}{2} \sin(2\pi f_{\text{sig}} t)$ of amplitude $A/2$ and frequency f_{sig} , the i^{th} tap voltage results in

$$v'_{out,i} = |\underline{H}_i(f_{\text{sig}})| \cdot \frac{A}{2} \sin(2\pi f_{\text{sig}} t - \text{arc}(\underline{H}_i)). \quad (5)$$

As this testbench shall only reveal performance degradation due to *delays*, the *amplitude* attenuation $|\underline{H}_i|$ is omitted here:

$$v'_{out,i} = \frac{A}{2} \sin(2\pi f_{\text{sig}} t - \text{arc}(\underline{H}_i)). \quad (6)$$

The i^{th} *differential* tap voltage then results (cf. (2) and Fig. 3) as the difference of the i^{th} tap in the positive EF branch and the $(B - (i - 1))^{\text{th}}$ tap of the complementary EF branch in

$$v_{out,i} = \frac{A}{2} \left[\sin(2\pi f_{\text{sig}} t - \text{arc}(\underline{H}_i)) + \sin(2\pi f_{\text{sig}} t - \text{arc}(\underline{H}_{B-(i-1)})) \right] - (i - 2^{b-1}) \cdot V_{\text{LSB}}. \quad (7)$$

- 2) The resistor ladder output voltages $v_{out,i}$ of (7) carry the result of the comparison of the input signal with the respective reference level in their signs (see (2)).

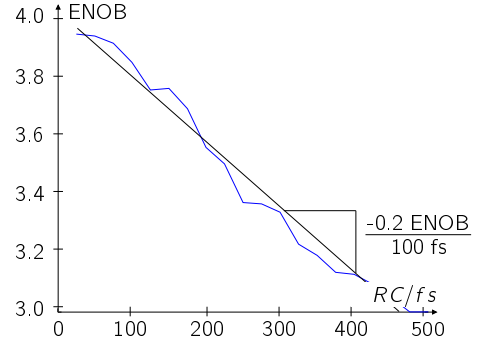


Fig. 5. ENOB degradation (solely) due to propagation delay in the quantizer in dependence of tap time constant RC .

Ideal comparators evaluate the sign and set their output voltages

$$\hat{v}_{out,i} := \text{sgn}(v_{out,i}) \quad (8)$$

to “1” or “-1” in dependence of the signs of their input voltages.

- 3) Ideal thermometer code ($\hat{v}_{out,i}$ of (8), where $i \in \{1 \dots B\}$) to analog conversion.
- 4) Computation of performance metrics of the analog signal obtained in the previous step. Fig. 5 shows the decrease in Effective Number Of Bits (ENOBs) in dependence of the RC time constant of one single tap. As the total capacitance (resistors, input cap. of comparator with Miller Effect, interconnects) of one tap is about $C = 20$ fF, the designer can expect a decrease of ≈ -0.2 ENOB if $R = 5 \Omega$, a decrease of ≈ -0.4 ENOB if $R = 10 \Omega$, and so on—solely due to the different propagation delays in both EF branches.

The tap resistance R is not only limited by the delay in the reference ladder but also by the load currents drawn from the comparators. Each current into a comparator connected to tap i causes a voltage drop at all taps above the i^{th} . If the input signal amplitude is half an LSB below positive fullscale, the bottommost (B^{th}) comparator has an input voltage of $v_{out,B} = \frac{1}{2} V_{\text{LSB}}$ (cf. (2)). All comparators at taps $i < B$ also have a positive input voltage, and base currents $i_{B,i,p}$ of the CS in the comparators are drawn from the positive EF branch of resistor ladder; the base currents $i_{B,i,n}$ drawn from the complementary EF branch can be neglected if the CS in the comparator is toggled completely (saturated). If the positive base currents $i_{B,i,p} = I_L$ are considered equal and constant, the distortion ΔV at the input of the B^{th} comparator is given by

$$\Delta V = B \cdot I_L R + \dots + 1 \cdot I_L R \stackrel{!}{<} \frac{1}{2} V_{\text{LSB}} \quad (9)$$

and must not exceed half the quantization step size V_{LSB} in order not to alter the polarity of the bottommost comparator. (9) can be rearranged to

$$R < \frac{V_{\text{LSB}}/2}{I_L \cdot (2^b - 1) \cdot 2^{b-1}} \quad (10)$$

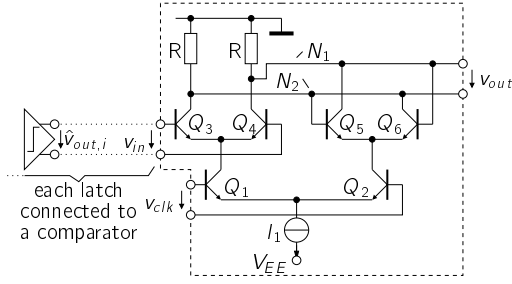


Fig. 6. CML latch in SiGe bipolar technology with load resistors.

and results in $R < 600 \Omega$ for static comparator base currents of $I_L = 200 \text{ nA}$, which is far too optimistic an upper bound for R . With *dynamic* load currents of $I_L = 10 \mu\text{A}$, the tap resistance is however already limited to $R < 12 \Omega$. (10) also shows, that this architecture is not suited for higher resolutions b because of the exponential dependency on b in both the nominator and the denominator (the quantization step size is given by $V_{\text{LSB}} = D/2^b$, where D is the input voltage dynamic range).

III. LATCH WITH ACTIVE LOAD

A. Ordinary CML latch architecture

An ordinary CML latch in SiGe bipolar technology with load resistors is depicted in Fig. 6 and has two operation modes referred to as tracking and latching, respectively. During tracking period, the tracking current switch Q_3, Q_4 sets the polarity of the output voltage v_{out} in accordance with the polarity of the input voltage v_{in} . During latching period, the latching current switch Q_5, Q_6 amplifies the voltage at output node pair N_1, N_2 because of the positive feedback [4]. Therefore, if the tracking current switch is not able to deliver the proper sign of the output voltage v_{out} by the end of the tracking period, the latching part generates an output voltage level of wrong sign during latching period. The circumstances under which the latch is not able to set the proper sign during tracking period is hence examined in further detail here.

Latch output nodes N_1, N_2 are heavily parasitically loaded by layout capacitances of load resistors R , by collector-base and collector-substrate capacitances of $Q_3 \dots Q_6$, by base-emitter capacitances of Q_5, Q_6 , as well as by the input capacitance of the following stage (not shown here) and the capacitance of the wires interconnecting all aforementioned components. The total capacitance at either node shall be referred to as C , and constitutes together with load resistors R a lowpass at each node. The difference of Kirchhoff's current laws at N_1 and N_2 , respectively, results (neglecting the feedback due to the Miller Effect) during tracking period in

$$C \cdot \frac{dv_{\text{out}}(t)}{dt} + \frac{v_{\text{out}}(t)}{R} = i_{\text{C3,4}}(t), \quad (11)$$

where $i_{\text{C3,4}}$ is the differential collector current of track current switch Q_3, Q_4 . The time domain solution of (11) results in

$$v_{\text{out}}(t) = v_{\text{out}}(0) \cdot e^{-\frac{t}{RC}} + \frac{1}{C} \int_0^t i_{\text{C3,4}}(t') \cdot e^{-\frac{t-t'}{RC}} dt' \quad (12)$$

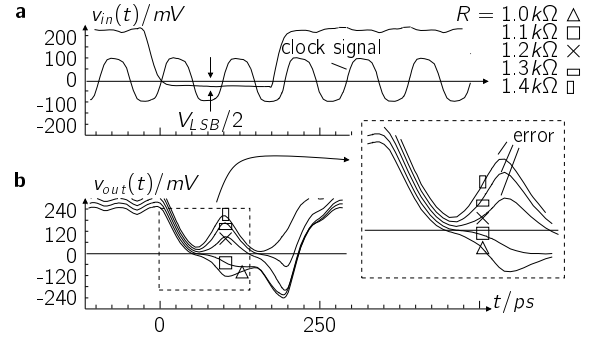


Fig. 7. a) Latch input voltage v_{in} and clock signal (sketched). b) Latch output voltage v_{out} in dependence of load resistance R .

(variation of constants, e.g. [6]). In order to evaluate (12), the worst-case scenario sketched in Fig. 7 is considered:

- 1) The input voltage $v_{\text{in}}(t < 0)$ of the previous tracking-latching-cycle is large enough to cause the output voltage at the end of the previous latching period ($t = 0$) to be (positive) fullscale. Therefore,

$$v_{\text{out}}(0) = I_1 \cdot R. \quad (13)$$

- 2) At $t = 0$, a tracking period (clock=high) starts and the input voltage toggles to half of the quantization step size $v_{\text{in}} = -\frac{V_{\text{LSB}}}{2}$ (minimum voltage the latch shall be able to digitize) of opposite (negative) sign. This input voltage level is held for an entire clock period.

- 3) The constant input voltage v_{in} causes a constant output current $i_{\text{C3,4}}$ of the tracking current switch. This output current is given by

$$i_{\text{C3,4}} = -\frac{V_{\text{LSB}}}{2} \cdot \frac{I_1}{V_K}, \quad (14)$$

where $\frac{I_1}{V_K}$ is the track current switch transadmittance linearized at $v_{\text{in}} = 0$. Again, the knee voltage V_K is the intersect of the linearized transfer function $i_{\text{C3,4}}(v_{\text{in}})$ with the saturation region $i_{\text{C3,4}} = I_1 = \text{const.}$ of the track current switch (c.f. (1)).

- 4) At the beginning of the succeeding latching period ($t = \frac{T_{\text{clk}}}{2}$, where T_{clk} is one clock period) the sign of the output voltage v_{out} must have been inverted (negative) at the latest. Then, the latching current switch generates an output level of proper polarity (negative) by means of its positive feedback. Therefore, it is essential that

$$v_{\text{out}}(t = \frac{T_{\text{clk}}}{2}) \stackrel{!}{<} 0. \quad (15)$$

With constraints (13) to (15), (12) can be evaluated and rearranged to

$$RC < \frac{T_{\text{clk}}/2}{\ln\left(\frac{V_K}{V_{\text{LSB}}/2} + 1\right)}, \quad (16)$$

which sets an upper bound to the load time constant RC of the latch. If RC exceeds that limit, the latch will not be able to track the aforementioned worst case input signal toggling properly.

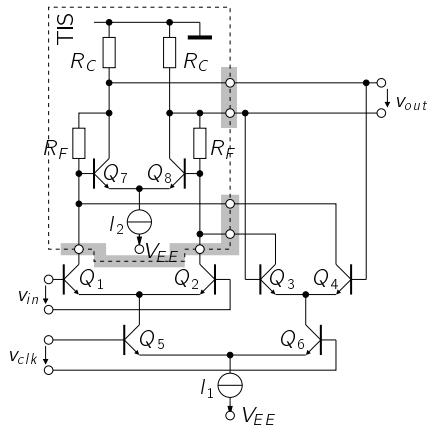


Fig. 8. Latch with transimpedance stage as active load within dashed area. $R_F = 3.5 \text{ k}\Omega$, $R_C = 5 \text{ k}\Omega$, $I_2 = 225 \mu\text{A}$, $V_{EE} = -2.5 \text{ V}$.

The maximum load resistance predicted by (16) results with a total parasitic capacitance $C = 20 \text{ fF}$, a quantization step size $V_{LSB} = 30 \text{ mV}$, a tailcurrent $I_1 = 300 \mu\text{A}$, a knee voltage $V_K = 70 \text{ mV}$, and an effective clock period $T_{clk} = 78 \text{ ps}$ (time in which collector current of Q_1 , Q_2 is greater than $I_1/2$) in $R < 1.1 \text{ k}\Omega$. The simulation result shown in Fig. 7 confirms that result: up to $R = 1.1 \text{ k}\Omega$ the output voltage is negative during latching period, above $R = 1.1 \text{ k}\Omega$ the latch can not deliver the proper (negative) sign. This would cause the next stage to acquire a wrong bit.

B. CML latch with active load

The output voltage swing of the ordinary CML latch architecture shown in Fig. 6 is determined by the output currents of the track- and latching current switch which cause voltage drops at the load resistors R . In order to save power, the tail current is adjusted low and the resistance has to be close to the upper bound given by (16) in order to obtain a high output voltage swing. Large load resistors however violates the impedance mismatch concept [1], which demands that high ohmic sources drive low ohmic loads and vice versa, as the high ohmic output impedance of the CS faces the high ohmic load resistor. By replacing the load resistors by a transimpedance stage (TIS) as shown in Fig. 8, additional degrees of freedom are introduced in order to simultaneously provide a low input (800Ω)- and output (100Ω) impedance, and a high transimpedance ($-2.5 \text{ k}\Omega$). This latch with the transimpedance stage as load will in the following referred to as *TIS-latch*, the load resistor topology of Fig. 6 as *R-latch*. In order to compare latch architectures automatically and quantitatively, the following assessment method is used.

C. Output signal quality assessment

In order for the stage succeeding the latch to acquire its input data properly, the latch output signal has to comply with the setup conditions of the succeeding stage. During latching period (shaded in Fig. 9), the latch output voltage must not fall below a certain threshold V_S during a setup time T_S .

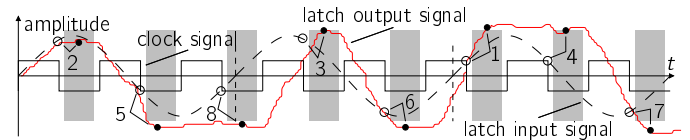


Fig. 9. Transient dependency of latch output signal on latch input signal if signal- and clock frequency are slightly offset (coherent sampling). *Circles*: Input signal amplitude sampled by the latch. *Dots*: Latch output amplitude stored for further analysis. *Numbers*: Reordering of samples as if latch had sampled one single low frequency signal amplitude.

Voltages below that threshold are in the following referred to as metastable states. Whether these conditions are met by the latch can be inspected visually by means of eye diagrams. As visual inspection only allows for qualitative conclusions, the following method is proposed.

- 1) At latch input a fullscale sinewave of frequency f_{sig} is applied. The clock frequency is set to f_{clk} . Both frequencies have to meet $N/f_{clk} = T_{sim} = M/f_{sig}$, where N is the number of samples (circles in Fig. 9) taken by the latch and M is the number of signal cycles during one transient simulation of duration T_{sim} . N and M have to be mutually prime in order to avoid repetitive sampling patterns.
- 2) The output voltage of the latch is stored in the middle of each latching period (dots in shaded regions in Fig. 9), which results in N values. The following steps are also performed for storing not in the middle of latching periods but at points in time slightly offset ($-T_{clk}/4 \dots T_{clk}/4$) with respect to the middle of latching periods (shaded regions in Fig. 9). The deviation of the sampling time from the middle of the latching periods is in the following referred to as *storing phase offset*. The samples taken at different storing phase offsets allow for an assessment of the invariance of sampling point deviations of the succeeding stage.
- 3) Because of the frequency offset between data- and clock-signal, the latch samples over the whole amplitude range of the input signal (circles of step 1); each input voltage amplitude is sampled twice (falling and rising edge of input signal). The samples taken in the previous step (dots) can be reordered (according to the numbers in Fig. 9), which results in samples in the same order as if the latch had sampled just one single signal period of duration T_{sim} .
- 4) Since the latch generates logic levels during latching period, the reordered samples (dots) constitute a rectangular output pattern representing 1 bit quantization of the single signal period mentioned in the previous step. The area under the rectangular output pattern is a figure of merit for the latch output voltage amplitude and hence directly related to the setup conditions of the succeeding stage. The area could on the one hand be computed by taking the absolute value of all negative parts and integration, which would however neglect any misdetermination of the proper sign by the latch (e.g.

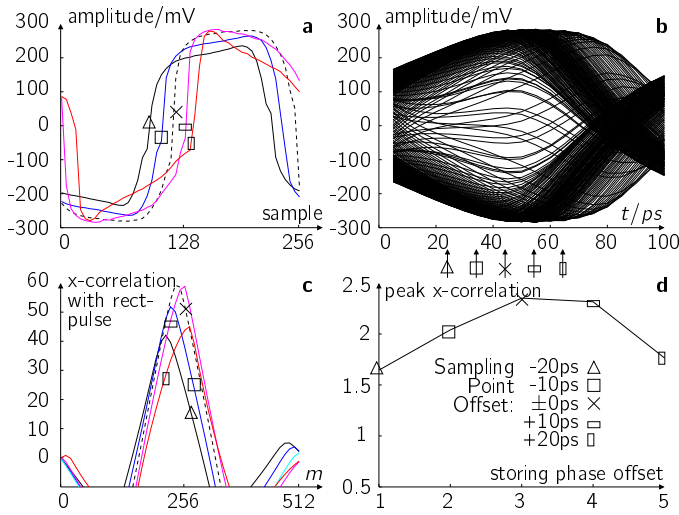


Fig. 10. Simulation results for TIS-latch with $I_1 = 80 \mu\text{A}$, $I_2 = 225 \mu\text{A}$, $R_F = 3.5 \text{ k}\Omega$, $R_C = 5 \text{ k}\Omega$. **a)** Reconstructed data signal. **b)** Output eye diagram of latch. **c)** Correlation with ideal rectangular pulse. **d)** Maximum of correlation in c) in dependence of samplingpoint (normalized by $V_S \cdot N$).

if the track part of the latch was not able to change the polarity within the available track time, misdetermination due to noise or because of offsets). In contrast, crosscorrelating that pulse with a rectangular pulse of unity amplitude ($N/2$ times “1”, $N/2$ times “-1”) yields the area under the rectangular output pattern as well. This particular correlation pattern has however the advantage of computing the area taking the correct sign of the respective halfwave into account. With the proposed crosscorrelation, the absolute value is only taken in that half of the period in which the output signal is known to be negative. The offset between the the correlation pattern and the latch output pattern is in the following referred to as $m \in \{1 \dots 2N\}$, where at $m = 1$ the last sample of the correlation pattern and the first sample of the output pattern coincide and at $m = 2N$ the first sample of the correlation pattern and the last sample of the output pattern coincide.

The rectangular output pattern obtained by reordering the samples taken from the TIS-latch output (visualized by the eye diagram in Fig. 10.b) is shown in Fig. 10.a). The result of the correlation (Fig. 10.c) and the dependency of the peak values on the storing phase offset (Fig. 10.d) characterize the eye opening. The flatter the peak crosscorrelation curve (Fig. 10.d), the higher is the horizontal eye opening. The higher the amplitude of the peak crosscorrelations, the higher is the output voltage amplitude of the latch during latching period. The peak crosscorrelations are normalized by the area $V_S \cdot N$ under an ideal rectangular pattern of height V_S .

Comparing the eye diagrams of the R-latch in Fig. 11.b) with TIS-latch in Fig. 10.b), the R-latch seems to be superior because of less metastable states and a higher opening in the middle of the eye. However, in terms of the quality of the reconstructed signal, the TIS-latch is superior. Firstly, the

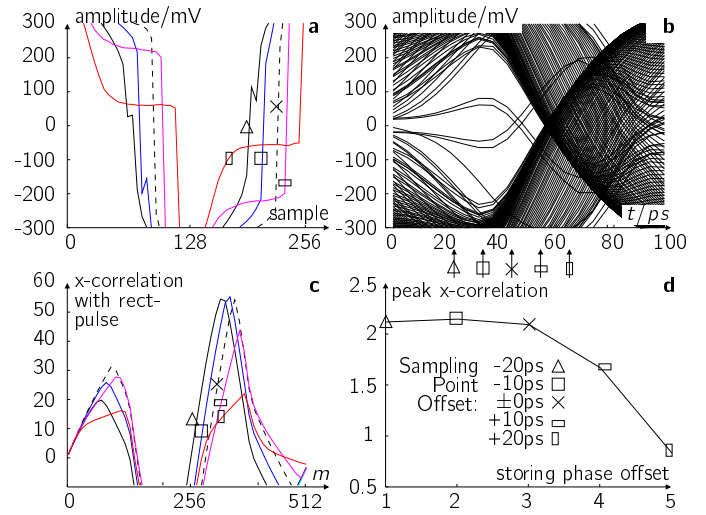


Fig. 11. Simulation results for latch with load resistors, $I_1 = 400 \mu\text{A}$, $R_L = 1 \text{ k}\Omega$. **a)** Reconstructed data signal. **b)** Output eye diagram of latch. **c)** Correlation with ideal rectangular pulse. **d)** Maximum of correlation in c) in dependence of samplingpoint (normalized by $V_S \cdot N$).

output pattern of the TIS-latch (Fig. 10.a) are rectangular for all phase offsets except for +20 ps, the curves of the R-latch (Fig. 11.a) only in the middle of the eye at ± 0 ps. This indicates that sampling point deviations of the succeeding stage have more impact in the R-latch architecture. Secondly, also the correlation functions (Fig. 10.c for the TIS-latch, Fig. 11.c for the R-latch) only reveal the typical W-shape resulting from correlation of two rectangular $[1, \dots, 1, -1, \dots, -1]$ pulses in the TIS-latch diagram. As the rectangular correlation pattern is constant, this indicates that the latch output pattern of the R-latch does not have the desired rectangular shape. Thirdly, the peak correlation is for the R-latch (Fig. 11.d) except for a phase offset of -20 ps below the peak correlation of the TIS-latch (Fig. 10.d). This also indicates that the succeeding stage is provided less phase margin in the R-latch architecture. As the TIS-latch consumes moreover $100 \mu\text{A}$ less than the R-latch, the TIS-latch was employed in the ADC.

IV. ADC FRONTEND PERFORMANCE SUMMARY

The simulated power dissipation of the ADC frontend (quantizer, 15 comparators, 2×15 latches, 15 output buffers, 15 clock buffer) is about $P = 50 \text{ mW}$ from a -2.5 V supply. The frontend has at Nyquist conditions (clock frequency $f_{\text{clk}} = 10 \text{ GHz}$, slightly less than $f_{\text{sig}} = 5 \text{ GHz}$ input signal frequency) an effective number of bits of $\text{ENOB} = 3$ bit, a signal to noise ratio of $\text{SNR} = 25 \text{ dB}$, and a total harmonic distortion of $\text{THD} = 22 \text{ dB}$. The minimum differential input voltage is $\text{LSB} = 31 \text{ mV}$ which corresponds to a dynamic input signal range $D = \pm 250 \text{ mVpp}$. Compared with measurement results of an ADC in a recent CMOS technology [7] with $\text{ENOB} = 1.8$ bit at $D = \pm 460 \text{ mVpp}$, $f_{\text{sig}} = 1.7 \text{ GHz}$, $f_{\text{clk}} = 3.4 \text{ GHz}$, and $P = 78 \text{ mW}$, the architecture proposed is more sensitive (smaller LSB), faster, and less power consuming. These figures are summarized in Tab. I.

	P	f_{sig}	f_{clk}	D
A	50 mW	5.0 GHz	10 GHz	± 250 mVpp
B	78 mW	1.7 GHz	4 GHz	± 460 mVpp

	ENOB	THD	SNR	LSB
A	3.0 bit	22 dB	25 dB	31 mV
B	1.9 bit	-	12 dB	57 mV

TABLE I
PERFORMANCE METRICS OF SiGe BIPOLAR DESIGN (**A**, SIMULATION) WITH AN ADC IN
A RECENT CMOS TECHNOLOGY [7] (**B**, MEASUREMENT).

V. CONCLUSION

New analyzation methods for both the quantization- and sampling stages facilitated optimization and resulted in straightforward approaches for the design of the high speed but yet low power ADC frontend. Performance limiting components were identified and vanquished by introducing additional degrees of freedom. The new CML latch architecture with a transimpedance stage as load complies (for low power designs in contrast to the load resistor approach) with the impedance mismatch concept, and was proven to be superior to the commonly used latch with load resistors. In a next step, the ADC frontend will be layouted, manufactured, and tested in order to obtain precious insights for future research concerning general decision guidance for the usage of either CMOS, BiCMOS, or bipolar only technologies.

ACKNOWLEDGMENT

The authors would like to thank Stéphane Le Tual, Sebastien Pruvost, and Didier Celi (all are with STMicroelectronics, Crolles) for valuable inspirations and precious feedback.

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