

An integrated PLL circuitry for very low reference frequencies

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Abstract — Here, a fully integrated phase-locked-loop circuitry is presented to generate an oscillator-frequency out of an extremely low-frequency external reference source. The PLL consists of a digital phase-frequency-detector, so it is sure that it can lock at the specified frequency from any starting point. A charge pump converts the high frequency digital control signals into currents, which are smoothed out in a first order analog low pass filter. The VCO is formed of a regenerative inverter chain, where the currents in the branches are controlled by the value-continuous input voltage level to obtain a voltage controlled output frequency. At power-on the capacitances of the analog filter are discharged, so this has to represent a high frequency for the VCO. With the transient phenomenon fading away the input voltage is controlled up via the feedback-loop, thus the assigned output frequency is descending. This PLL was built in a standard $0.35\mu\text{m}$ CMOS-technology line and uses the mains frequency as an inexpensive substitution for an external reference source.

Keywords— PLL; mains frequency; analog filter; fully integrated in standard CMOS

I. INTRODUCTION

This contribution presents an integrated frequency synthesizer circuitry, which is designed for generating an appropriate clock signal to feed an onchip standard serial interface (RS-232) for receiving and sending data words. As the carrier frequency for the serial interface is defined to 9600 Hz , a 16 times higher clock signal of 153.6 kHz is required for this PLL due to internal synchronisation within the digital interface.

In MOS-technology unfortunately there is no way to design a completely independent integrated PLL with sufficient requirements to the precision of the oscillation frequency without any external reference triggering. This is due to transistor-mismatching and unknown

parameter variations during operation e.g. depending on temperature, supply voltage etc. Therefore there has to be a kind of external reference to ensure an appropriate clock frequency. In contrast, because of the low cost character of the total system in [3] where this PLL has to be implemented, any additional external reference devices should be omitted, which is a very explicit demand. But as the system in [3] generates its own supply voltage from the mains, there is an alternative option to use the 50 Hz frequency of the mains voltage for external triggering because a subcircuitry already exists, which detects the zero-crossings of the mains.

The transmission of a single data word on the serial bus defines the minimum frequency requirements of the PLL. Here, the generated clock signal should not have a greater drift than 4.86% . These weak requirements are accomplished for the serial transmission by using the mains frequency as the reference source for this PLL, which parameters are regulated by the European norm no. 50160 [4]. Figure 1 shows how the 153.6 kHz clock signal is generated out of the 50 Hz reference.

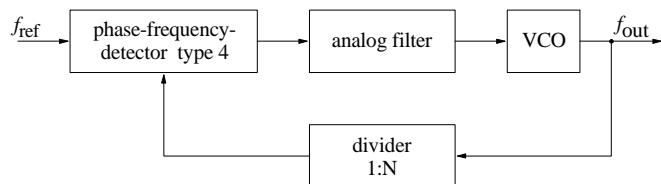


Figure 1: block diagram of the PLL

II. PHASE-FREQUENCY DETECTOR

This PLL can be concepted as a simple digital one, because there is only a symmetric clock signal needed as the circuit output. So, here we can use a logic block to detect the actual phase-error between the reference and

the divided VCO-output. Publications on this topic propose to use the ‘type-4 phase-frequency detector’ (PFD) because it is able to detect phase-errors as well as frequency-errors, so the pull-in range $\Delta\omega_p$ for this PLL is unlimited. By using the subcircuit from figure 2 it is ensured, that the PLL can lock on its target frequency from any starting point. The pulsed UP & DOWN-signals indicate, whether the working frequency of the VCO has to be raised up or scaled down.

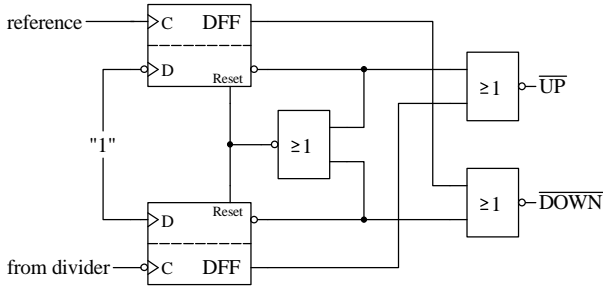


Figure 2: logic of the PFD

III. ANALOG FILTER

The frequency-information from the UP & DOWN-signals have to be converted into a value-continuous voltage level which is done with this analog filter block. All high-frequency shares have to be smoothed out so that the VCO can reach its intended output frequency asymptotically. In other words the filter has to apply a low-pass characteristic for the pulsed signals from the PFD. But these signals only show the *direction* of the voltage-modification for the new VCO frequency, so it is necessary to have the actual voltage level stored e.g. in a capacitance. This is realized in a first order RC-stage, where the dimensions of R and C define the behaviour how strong the VCO will respond to the UP & DOWN-commands.

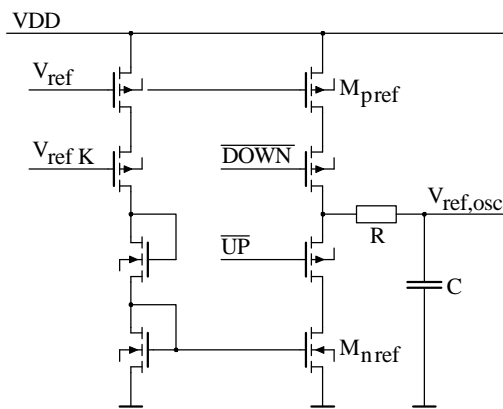


Figure 3: charge-pump & RC-filter

These logical signals act as switches to load/unload the capacitance with the same current. An active phase of both signals UP *and* DOWN is excluded in the logic of the PFD, so the output voltage will directly change depending on the amount and lengths of the UP & DOWN-signals. To achieve a maximum RC-constant the area of the capacitance was chosen at its maximum value of 30 pF . A bigger area is not suggestive for an integrated capacitor for the applied technology line. In combination the currents that feed the filter through the P- and N-channel current sources were set to a reasonable minimum of $0.5\ \mu\text{A}$. Further, smaller currents will have an unproportional rising impact on the transistor mismatching. In figure 4 you can see the filter as a single realization.

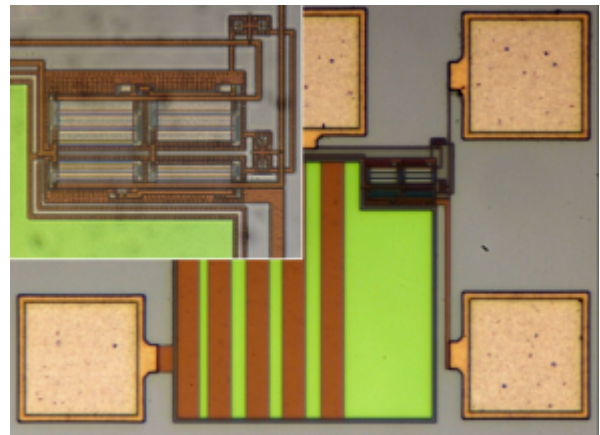


Figure 4: chip-foto of the analog filter

The figure indicates impressively that the active devices allocate 6% of the total area only, the rest is required by the integrated capacitor. In the top left corner you can see the active part magnified.

IV. VOLTAGE CONTROLLED OSCILLATOR

The VCO has to generate a on/off-symmetric square-waveform. The frequency of this signal has to depend directly on the value-continuous input voltage-level, preferably linearly dependent. When the VCO is in steady state, its target frequency is defined to be 153.6 kHz . Therefore this frequency should be mapped about in the middle of the associated input-voltage range. In addition, it has to be ensured, that at power-on the frequency is selected to a controllable value in order to ensure that this starting-frequency can be definitely captured to its intended target range. In figure 5 the schematic of the VCO is depicted. The oscillator consists of a feedback inverter chain with 5 stages. Due

to noise the status of the chain is automatically driven into one of the two stable operating points and as a result of the regenerative feedback an oscillating square wave is formed.

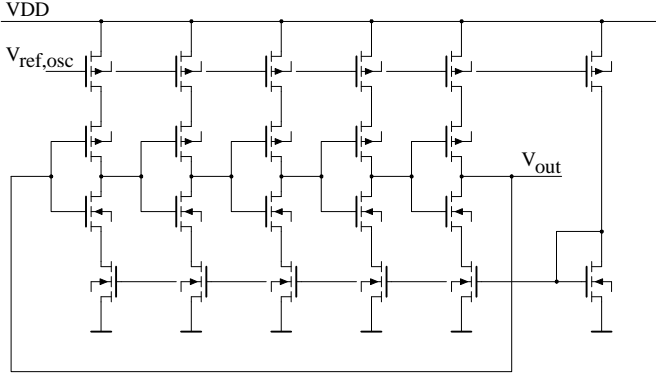


Figure 5: schematic of the VCO

In the figure the upper and lower rows represent transistors which act as ‘constant’ current sources for the inner push-pull array. Thus the load & unload-speed for the nodes can be adjusted in dependence on the current sources. To obtain only one voltage-level for both n-channel & p-channel current-adjustments the upper right branch of figure 5 generates an appropriate voltage for the lower row out of the variable voltage-level of the upper row, which is used as the input for the VCO.

The p-channel threshold voltage $V_{T,P}$ of 900 mV from the applied $0.35\text{ }\mu\text{m}$ technology line limits the upper edge of the valid input range. Here, high input-potentials cause low branch currents and thus low output frequencies, in contrast, decreasing the input-potential results in a faster oscillation. For the target frequency of 153.6 kHz a voltage-level of about 3 V was designed at a V_{DD} of 5 V .

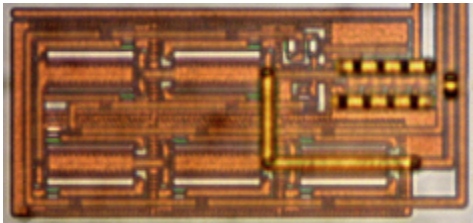


Figure 6: chip-foto of the VCO

V. DIVIDER

The control loop is closed by the digital divider circuitry, where the VCO-output is scaled down in the order of frequencies near to the reference frequency.

This signal can be used in the PFD for phase & frequency comparisons with the reference source. On this way the output frequency is being controlled as a result of the external reference frequency and the integrated factor of the divider. Due to the feedback loop the circuit permanently tries to compensate the phase error.

Looking at the specified target frequency of 153.6 kHz and the reference source of only 50 Hz there is an extremely huge ratio between these frequencies of 3072 . It is not well using such a big multiplier because there are very few edges of the reference clock for comparison so that decisions of the PFD tend to be too strong. On this account unfortunately there will be still a little ripple left at the output clock (see figure 7).

VI. STARTUP BEHAVIOUR

At power-on it takes some time for the PLL to reach its target frequency. The VCO was designed to generate a high frequency output when the input voltage-level is low. Thus, it is ensured, that the oscillator is definitely running, because at startup the integrated capacitance is completely unloaded. The period of time until the frequency is locked is depending on the RC -constant of the analog filter. In figure 7 the startup behaviour is shown.

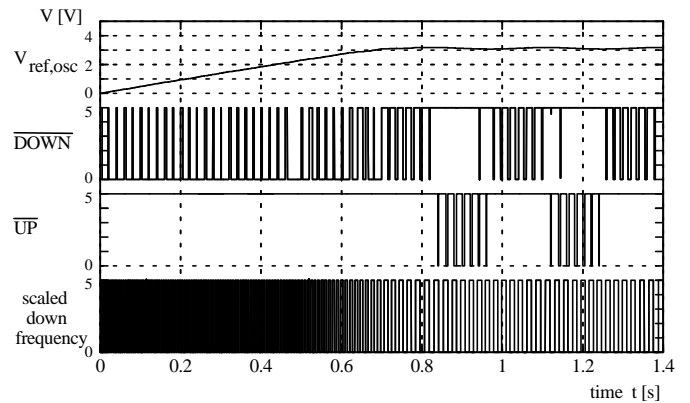


Figure 7: startup behaviour of the PLL

Due to the big frequency difference relating to the reference at power-on, the PFD is signalling with many and continuous (low-active) DOWN-pulses to rise the terminal voltage of the integrated capacitor. This is leading to a slow decrease of the output frequency. After about 0.6 s the oscillator is slowed down sufficiently that the PFD can control to match phasing of both frequencies. This cannot be exactly managed as a result of the huge divider factor. Therefore the PFD

permanently attempts to over-compensate the remaining phase error, which can be seen in figure 7 at the alternating UP & DOWN conditions when the PLL is in steady state ($t > 0.7\text{ s}$). This over-compensation is also illustrated by the progress of the VCO's input voltage level, which shows a remaining low-frequency ripple with a period of about 2.5 Hz . In figure 8 the active area of the total PLL is depicted.



Figure 8: active area of the PLL

This realization of a digital PLL has an absolute maximum frequency drift below 5.4% related to the specified target frequency¹ which is quite a little bit to high for the attended application [3]. Fortunately the period of the low-frequency ripple is long enough, that it is very likely to get a time frame where the requirements are within the specifications for about 100 ms . In addition the system in [3] has an error detection, so the data transmission can be repeated, if an error occurs due to an invalid frequency drift. In practical implementation this method is working very well.

An approach to improve the frequency-characteristics of the PLL could be e.g. to revise the concept of the VCO. The observed frequency-jitter is not effected by a too big divider factor only, but also due to the functional principle of the VCO. Here, too many active devices are used that all cause noise in the form of a phase error. The challenge is to find out an oscillating circuitry for extremely low frequencies that utilizes very few active devices. Further improvements could be obtained by applying an active *SC*-filter in stead of the first order *RC*-filter. This will be implemented in future realizations of the PLL.

VII. CONCLUSION

The circuit presented here shows a design of a completely integrated PLL used as a clock generator for an onchip serial interface. Its reference source is generated out of the mains frequency. For this purpose only one additional external resistor is needed which is already implemented in the system in [3]. It could be proven, that the concept to employ a reference frequency

out of the mains for an integrated PLL can be used for the given application although it has its limitations in respect of phase noise. All components could be integrated together with other part of the system in [3] to build an integrated microsystem.

REFERENCES

- [1] U. L. Rohde "Digital PLL Frequency Synthesizers – Theory and Design", Prentice-Hall 1983, ISBN 0-13-214239-2
- [2] L. v. Wangenheim „Aktive Filter in RC- und SC-Technik – Grundlagen, Berechnungsverfahren, Schaltungstechnik“, Hüthig Verlag 1991, ISBN 3-7785-1894-1
- [3] D. Batas, J. Oehm, K. Schumacher : "A Low Cost Solution For Programmable Analog Parametric Fields", *IEEE Conference on Electronics, Circuits and Systems* 1999, Vol. II, p. 1035-1038, ISBN 0-7803-5682-9
- [4] European Norm, CENELEC 1999, Ref. No. EN 50160 : 1999 D

¹ maximum frequency: 161.4 kHz , minimum frequency: 145.3 kHz