Dielectric properties of Hot Wire CVD silicon nitride applied in a-Si TFTs

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Abstract—**A high density amorphous silicon nitride (SiN_x) film, deposited at 3 nm/s, has been integrated in a-Si TFTs to study its performance as gate dielectric. Using HWCVD for both the SiN_x gate dielectric and the a-Si channel, leads for this stack to a total deposition time of less than 4 minutes. Analysis of these "all hot wire" TFTs shows an initial threshold voltage of 1.7 V, an on/off ratio of 10^6 and a mobility of 0.4 cm^2/Vs after a forming gas anneal. A threshold voltage shift is observed after bias stressing however, this is likely caused by charge trapping in the SiN_x.**

SiN_x films with various compositions (1.1 < N/Si < 1.6) have been incorporated in metal-insulator-semiconductor (MIS) structures. Current-voltage (I-V) and capacitance-voltage (C-V) measurements have been performed. In addition the root-mean-square (*rms*) roughness and mechanical stress was measured. For N-rich films (N/Si >1.33) the trapped and fixed charges are up to ten times smaller than for more Si-rich films (N/Si < 1.33). The static dielectric constant appeared to be independent of the composition ($\varepsilon = 6.3$). For N-rich films breakdown fields exceed 6 MV/cm. The mechanical stress is below 300 MPa and the *rms* roughness decreases with N/Si ratio. Thus, rapidly deposited "all hot wire" TFTs already show good performance, although more N-rich SiN_x as gate dielectric is expected to improve both the mobility and stability.

Index Terms— **Dielectric properties, Hot wire CVD, Mechanical stress, Silicon nitride, Thin Film Transistors.**

I. Introduction

Thin film amorphous silicon nitride (SiN_x) is an insulating material of increasing interest to photovoltaic (PV) technology and integrated circuit (IC) technology. Thin film SiN_x has been shown to be an excellent defect passivating anti-reflection coating and encapsulation layer in crystalline silicon (c-Si) solar cells [1-5], plastic electronics [6,7] and organic light emitting diodes (OLEDs) [8]. SiN_x is also applied as moisture resistant barrier coating [9] in electronic circuitry [10,11] and as insulating gate dielectric in Si thin film transistors (TFTs) [12-15].

A conventional way to deposit thin films of SiN_x at a large scale is by using a plasma deposition method such as plasma enhanced chemical vapor deposition (PECVD). However, a method like PECVD has a number of limitations such as film damage and dust formation due to the use of a plasma [16]. A plasma-free and thus fundamentally different deposition technique is available and has been attracting much interest. This technique is the hot wire chemical vapor deposition (HWCVD) technique, also known as Hot Filament (HF) CVD or Cat-CVD.

The HWCVD technique uses the catalytic decomposition of source gasses on 2D catalyst metallic filaments. HWCVD is plasma-free and thus does not share the plasma related limitations and furthermore it is an ultra fast deposition technique [17] with high gas utilization efficiencies [18]. HWCVD holds straightforward scalability to large area deposition without the need for additional frequency generators as in methods that use a plasma.

The HWCVD technique for thin film deposition of a-Si and SiN_x is well suitable for thin film transistor (TFT) fabrication because for economic production of TFTs for active matrix applications, it is highly desirable to have high deposition rates and good gas utilization. It has been reported that TFTs with thermally grown SiO_2 on c-Si as gate dielectric and HWCVD a-Si as conducting channel, are electronically more stable than when the a-Si is made with PECVD [19,20]. Because the a-Si conducting channel can be made with HWCVD, a suitable alternative for the gate dielectric layer is SiN_x which can also be made with HWCVD. The application of this very fast and easy scalable technique for all layers decreases processing time greatly. A disadvantage of PECVD is that it leads to SiN_x materials that are too porous and too H-rich at high N concentration [21]. Furthermore it has been shown that in HWCVD SiN_x the hydrogen is mainly bonded to nitrogen atoms and only a small amount is present in the Si-H configuration [22]. This low amount of Si-H bonds is an advantage for the use as sidewall and liner material in ultra large-scale integrated circuits p-type metal-insulator-semiconductor (p-MIS ULSI) transistors. This is the case because H, coming from the SiN_x at the sidewalls, can create defects at the gate/gate-insulator interface [23].

TFTs exclusively made with HWCVD have been investigated in the past and showed good performance and stability [24,25]. In this paper we report on "all hot wire TFTs" with amorphous hydrogenated SiN_x as gate dielectric made at a very fast rate of 3 nm/s

Nishizaki *et al.*[15] showed that a-Si TFTs made with HWCVD, show high stability upon bias stressing and that the threshold voltage shift is due to charge trapping in the SiN_x only. To quantify trapped charges and to optimize the HWCVD SiN_x deposited at high deposition rates (~3 nm/s), we have determined the mechanical stress, the root-mean-square (*rms*) roughness and the dielectric properties including

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fixed and trapped charges of HWCVD SiN_x for various compositions.

II. Experimental details

Depositions

The depositions described in this paper are performed in a four-filament hot wire reactor that is part of an ultra high vacuum multi chamber system (PASTA) [26]. A schematic drawing of the reactor is shown in figure 1.

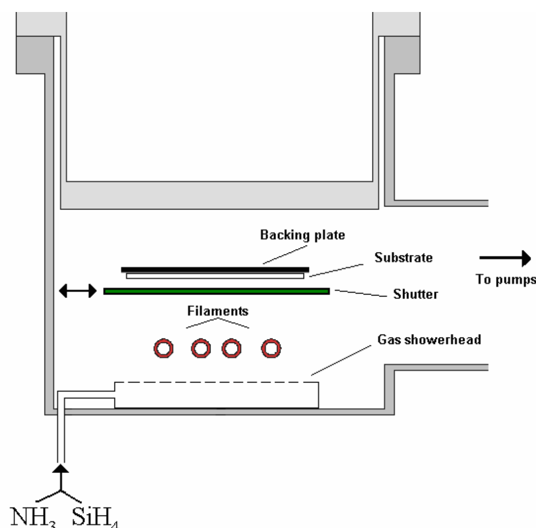

Fig. 1 Schematic drawing of the hot wire CVD reactor. Precursor gases for SiN_x deposition are ammonia (NH_3) and silane (SiH_4).

As source gasses, pure silane (SiH_4) and ammonia (NH_3) are used for SiN_x deposition. For a-Si:H only pure SiH_4 is used. Thus, for both types of materials no hydrogen dilution is used. The source gasses are catalytically decomposed at tantalum filaments held at 2100°C for a-SiN_x:H and 1850°C for a-Si:H. The substrate is heated by radiation from the filaments only, to a temperature of about 450°C for SiN_x and 250°C for a-Si:H. The filaments are placed 3 cm above the substrate. In this laboratory system, a shutter is situated between the sample and the wires to control the duration of the deposition. A square showerhead gas inlet was used, which creates a uniform deposition area of 5×5 cm^2.

Measurements

The composition of the HWCVD SiN_x films is represented by the atomic N/Si ratio, for which the x in SiN_x stands. The atomic N/Si ratio has been determined by Elastic Recoil Detection (ERD) analysis [27], which has recently been carefully calibrated by Rutherford Back Scattering (RBS) [28]. A value of N/Si = 1.33 represents stoichiometric silicon nitride (Si_3N_4). Due to intrinsic stress in a SiN_x film, the film-substrate structure shows curvature. When the film-substrate structure cools down after deposition, the difference in thermal expansion coefficient of the film and the substrate, causes additional thermal stress. To quantify the total stress from the curvature of the film-substrate structure, we follow the approach given by Glang et al. [29], for HWCVD SiN_x films this method is explained in more detail in [30].

To investigate the dielectric properties of SiN_x films with structural composition of $1.1 < N/Si < 1.6$, metal-insulator-semiconductor (MIS) structures are made. n-Type c-Si Czochralski wafers ($\varepsilon_s = 11.9$) are used with resistivities of 1-5 Ωcm. Aluminum (Al) is evaporated on the backside of the wafer as Ohmic contact. Al dots (0.16 cm^2), are evaporated as front contact. Current-voltage (I-V) measurements were performed to determine the electric breakdown field, which is defined as the field when the current density is $J_{break} = 10^{-6}$ A/cm^2. Capacitance-voltage (C-V) measurements are performed with a voltage sweep speed of 0.4 - 0.9 V/s, a signal frequency of 1 MHz and a bias voltage that is swept between –40 V and +40 V. The small signal capacitance is measured using a differential voltage with an amplitude of 20 mV, which is superimposed on the bias voltage that sweeps from inversion to accumulation and back. Quantities are determined from the C-V curves following the treatment of Sze [31].

III. Results and discussion

TFTs with HWCVD SiN_x and HWCVD a-Si

Thin film amorphous SiN_x made with HWCVD has a maximum in mass density and a minimum in hydrogen concentration at an atomic N/Si ratio of 1.3 [17]. For this reason this material is tested in TFTs. Trilayer TFT structures in bottom gate staggered configuration have been made, the structure is shown in figure 2. The structure consists of HWCVD $SiN_{1.3}$ (made at 3 nm/s), HWCVD a-Si:H (made at 1 nm/s) [32] and μc-Si:H highly doped n-layers. For the SiN_x/a-Si:H stack this leads to a total deposition time of less than 4 minutes.

We maintained a high SiH_4 utilization efficiency of 77%, despite the much higher flow rates that are necessary to obtain the high SiN_x deposition rate [16]. The utilization efficiency for the less expensive ammonia is under these conditions 7%. The depositions were performed at Utrecht Solar Energy Laboratory (USEL) on Corning 1737 glass with pre-patterned Cr gates as provided by Japan Institute of Advanced Science and Technology (JAIST). After deposition of the HWCVD films, the photolithographic structuring was performed at JAIST. Unfortunately, it was necessary to introduce an air break between the SiN_x deposition and the a-Si:H deposition, which most likely puts an upper limit on the achievable mobility. In these first experiments, the SiN_x gate insulation was made thick (400 nm) to avoid electrical breakdown of SiN_x. The result is that no pinholes have been found within the matrix made (86 TFTs) but the S-value is rather large. Analysis shows that these “all hot wire” TFTs have an on/off ratio of 10^6 and a mobility of 0.4 cm^2/Vs after a forming gas anneal, the transfer characteristics of the TFTs were measured three times [14].

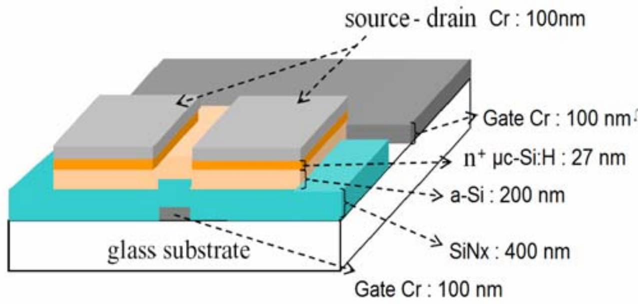

Fig. 2 Schematic diagram of the tri layer structure made by USEL and JAIST.

The threshold voltage is slightly increased in the direction of more positive gate voltage after each measurement and amounts to V_{th} = 1.7 – 2.4 V. The V_{th} shift can be caused by charge trapping and is dependent on the composition of the SiN_x dielectric in the case of plasma-deposited films [33]. A study of the defect density and bond structure specifically for hot wire deposited SiN_x was performed at JAIST [15]. The present TFTs show that the HWCVD $SiN_{1.3}$, deposited at 3 nm/s, is already suitable for application in TFTs. To determine whether N/Si = 1.3 is the optimal N/Si ratio, stress, *rms* roughness and electrical measurements are performed.

Mechanical stress and rms roughness in HWCVD SiN_x

For our HWCVD SiN_x films the intrinsic stress is tensile for SiN_x depositions with 1.2 < N/Si < 1.6. The thermal stress in a SiN_x film is constant with stoichiometry and amounts to -240 MPa (compressive) for films deposited at 450ºC. Figure 3 shows the total stress as a function of HWCVD SiN_x composition.

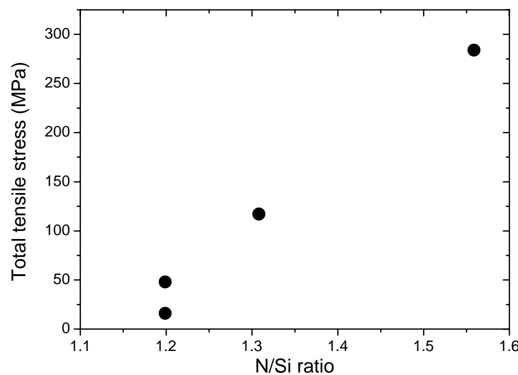

Fig. 3 Total mechanical stress as a function of atomic N/Si ratio. For the investigated range of compositions the stress is tensile.

A linear dependence is found with for the most N-rich samples the highest amount of total stress. For layers with N/Si = 1.2, the tensile stress becomes as low as 16 MPa. This stress is much lower than reported for near stoichiometric PECVD SiN_x coatings [34-37]. Low stress in thin films is also important in micro-electro-mechanical (MEMS) applications, plastic electronics and when TFTs are deposited on thin polymer foil.

The root-mean-square (rms) roughness measured on 300 nm thick $SiN_{1.3}$ layers is about 1 nm, which is necessary for high field-effect mobility in thin film transistors, for more N-rich layers (N/Si >1.4) even lower *rms* values of 0.5 nm are found.

Dielectric properties of HWCVD SiN_x

In Figure 4, the results of the C-V measurements as a function of the layer composition are shown for a range of films with 1.1 < N/Si < 1.6. In the top graph the static dielectric constant (ε) is shown, it is deduced from the accumulation capacitances of the MIS structures.

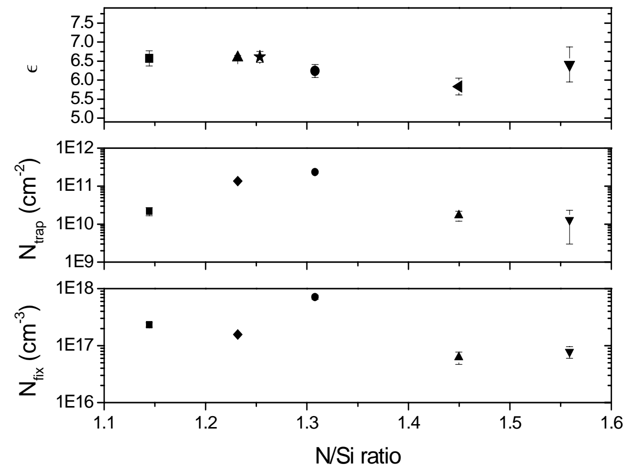

Fig. 4 Static dielectric constant, number of trapped charges and total fixed charges as a function of atomic N/Si ratio.

The middle graph shows the behavior of N_{traps}, which is the number of shallow interface traps (trapped charges) as is determined from the backward sweep in the hysteresis in the C-V characteristics. The bottom graph shows N_{fix}, which is the number of fixed charges, which includes fixed, mobile and surface state charges. N_{fix} is determined from the flat band voltage and is assumed to be homogeneously distributed in the SiN_x film. We deduced a lowest fixed silicon nitride charge density of 6.2 x 10^{16} cm^{-3} and a lowest fast trapped charge density of 1.3 x 10^{10} cm^{-2} for N-rich films with N/Si ≥ 1.45. For N/Si = 1.3 the fixed charges and trapped charges appear to have a maximum and for N/Si < 1.3 the charges decrease again but are still ten times as large as for the N-rich films.

I-V measurements were performed on the MIS structures. The normalized currents ($J_{break} = 10^{-6}$ A/cm^2) versus the breakdown fields are shown in Figure 5. The MIS structures show no breakdown for SiN_x films with N/Si ≥ 1.45 and d > 174 nm. For films thinner than 174 nm the structures always seem to show shunting. Also for MIS structures with $SiN_{1.25}$ and d = 400 nm there is no electrical breakdown observed.

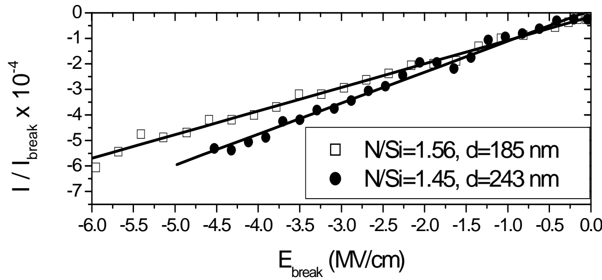

Fig. 5 Normalized current versus electric breakdown field for two MIS structures.

The breakdown fields obtained hence exceed 5.9 MV/cm. Other groups also report that SiN_x films with higher N/Si have higher breakdown fields but also report higher static dielectric constants as the layers become more N-rich [38,39], while we report a roughly constant value for the static dielectric constant. Breakdown fields for PECVD or HWCVD SiN_x of 2-6 MV/cm have been reported [38,40,41]. In order to meet the requirements for a good gate dielectric, the SiN_x material has to withstand electric fields of ≥ 2 MV/cm [38], and thus the HWCVD SiN_x films also qualify for TFT applications in this respect.

IV. CONCLUSIONS

It has been demonstrated that HWCVD SiN_x layers, deposited at 3 nm/s, can be applied in TFTs. Combined with hot wire deposited a-Si:H at 1 nm/s, this leads to a total deposition time of less than 4 minutes for the SiN_x/a-Si:H stack. The silane gas utilization shows a high value of 77%. No pinholes have been found within the TFT matrix made (86 TFTs). The mobility of these a-Si:H TFTs is 0.4 cm^2/Vs after a forming gas anneal. The TFTs have a V_{th} of 1.7 – 2.4 V and an on/off ratio of 10^6.

Stress measurements reveal that with the HWCVD method, SiN_x can be deposited possessing very low mechanical stress. The stress is 16 MPa (tensile) for layers with N/Si = 1.2 and up to a still low value of ~300 MPa (tensile) for very N-rich layers (N/Si = 1.56). The *rms* roughness is smaller for N-rich films than for Si-rich films. In this respect, SiN_x in the range of 1.2 < N/Si < 1.6 meets the requirements for electro-mechanical (MEMS) applications, plastic electronics, and TFT deposition on thin polymer foil.

For films with N/Si < 1.3 both the number of trapped and fixed charges are ten times as large as for the N-rich films with N/Si ≥ 1.45. A dielectric constant of ε = 6.3 and high dielectric breakdown fields exceeding 5.9 MV/cm show the potential for SiN_x to be incorporated in electronic circuitry.

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