Effects of Manufacturing Variability on Integrated Passive Components

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***Abstract*—Manufacturing variability in IC fabrication processes is gaining more and more attention as the technology dimensions continue to shrink, the operation frequencies continue to go up and the fabrication complexity keeps increasing. The effects of the resulting process-induced variations can no longer be simply neglected in advanced design flows. For electrical verification and simulation purposes after (or during) completion of the physical design, designers usually employ models or equivalent circuits. In view of the increasing variability in general, the need arises to study their effects on integrated passive components and eventually to develop parameterized models so that the effect of the variability can be more effectively analyzed. Such parameterized models can be represented in various ways, one way is using polynomial expansions around the nominal value. Since the order of these expansions determines the complexity and the accuracy of the model, it is necessary to find a good balance between the efficiency and the accuracy, which is a major task of this paper.**

For that purpose, we have studied a system with two coupled transmission lines using the 3D EM simulator Sonnet10.53, as well as a variety of integrated planar inductors using the compact model LSIM3.1 by Philips Electronics. A large amount of simulation experiments has been conducted to study the effects of process-induced variations in a statistical perspective. For integrated inductors, we have shown which geometric parameters can contribute most to the variability of their inductance L and quality factor Q and also that the order of magnitude of Q-variability can be around 10% for typical manufacturing tolerances with the variability of L being smaller. Furthermore, we have also shown that the variability of L and Q can be accurately and efficiently captured by first-order polynomial expansions of the component values in a lumped equivalent circuit model.

***Index Terms*—manufacturing variability, microstrips, integrated inductors, lumped element models, polynomial expansion.**

I. Introduction

Manufacturing variations can be divided into two major groups, the inter-die and the intra-die variations. We concentrate on studying the intra-die (also called within-die) variation which is playing an important role and is gaining interest in deep submicron technologies. As its name implies, intra-die variations are deviations existing within a die.

The intra-die variations can be further categorized into device variations, dynamic variations and interconnect variations [7]. Device variations mainly refer to the fluctuations in active device parameters, including the threshold voltage, the gate oxide, the thickness of the gate oxide and the drain/source region parasitic resistance. Device variations are caused by patterning (photo lithography), thin film deposition and etching in the manufacturing process.

Dynamic variations are variations due to the operation fluctuations of the system, such as supply voltage variations due to loading of power supply grid and voltage drooping, and temperature variations which vary with the location of highly active blocks throughout the die.

Our study concentrates on interconnect variations. The effects of manufacturing variabilities on interconnects and integrated inductors have been studied in some papers [1] - [6], but there still lack of a systematic method to study and model the effects for passive components.

This paper will start with a general review of some primary mechanisms of interconnect variations. In section III, we analyse and present the effects of manufacturing variations on coupled transmission lines based on a lumped element model. An illustrative example of a parametric model is given at the end. Section IV studies the manufacturing variability of integrated inductors based on a compact model. A detailed case study is presented to give a clear idea of a variation-aware model, which is followed by a statistical analysis. Some conclusions are given in Section V.

II. Interconnect Variations

In this section, we will introduce several major process steps that contribute to interconnect variations; to what extent can they influence the geometry and electrical parameters of the interconnects and the current compensation approaches as well.

Lithography Lithography-induced variations usually occur at the corners of interconnect structures and influenced by surrounding geometries and the process environment. Variations in the metal width and the spacing between conductors

can extend out to a few microns due to the lithography effects [8]. Optical proximity correction (OPC) is a technique that is commonly used to compensate for such pattern transfer non-idealities by making modifications to mask geometries.

Etching Besides lithography, the etching process can also contribute to variations in the metal width. This is known as *etch bias* which is mainly due to the isotropic property of the chemical ingredient within the etching process.

Chemical Mechanical Polishing The chemical mechanical polishing (CMP) process for meeting planarization requirements in deep submicron technology has strong effects on the thicknesses of metal layers and inter-layer dielectrics. The CMP effect is highly layout dependent, which is due to the difference in polishing rate of different materials, to be specific, the metal and the oxide. This effect can be greatly reduced by metal-fill patterning [9].

Above, we have briefly discussed the causes of manufacturing variations in three main geometry parameters, namely the width of conductors, the thickness of metal layers and the thickness of inter-layer dielectrics. In our study, these parameters are considered to vary independently from each other. We should notice that the spacing between conductors is not one of them because the pitch is usually well controlled in fabrication process and assumed to be constant in our simulation experiments.

III. Coupled Transmission Lines

Based on a lumped model, we analyze the effects of manufacturing variations on coupled microstrips in terms of the behaviors of relevant lumped elements in the model with respect to random parameter variations. We then utilize 0th, 1st and 2nd order polynomial expansion approximations to model these behaviors and compare the results to the designed values. Finally, an illustrative example is given.

A. Simulation Setup

Two coupled microstrips are utilized for our study as shown in Fig.1. This is the schematic from Sonnet10.53 where the microstrips are enclosed in a six-sided metal box which serves as the electrical ground. The four ends of the two conductors touch the box with four ports, meaning they are connected to the ground with ports whose impedance are by definition 50Ω. Two conductors, above which locates the air layer, are separated from the bottom ground plane by a dielectric layer. The conductors are $3\mu m$ in width and $1\mu m$ in thickness. The space between them is $1\mu m$. The dielectric layer is $2\mu m$ thick with a relative permittivity of 3.9.

From the transmission line theory, we know that the electric and magnetic fields behave like waves in the dielectric layer. In order to generate a lumped element model, the transmission line is divided into small pieces whose lengths are much smaller than the wavelength λ (less than $1/20$ of λ). Each piece is treated as a lumped element sub-network, referred to as a *lumped line segment*. The whole transmission line can then be obtained by cascading a integer number of these lumped line segments. The length of the coupled microstrips shown

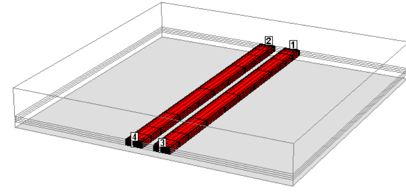


Fig. 1: Sonnet schematic: target coupled microtrips.

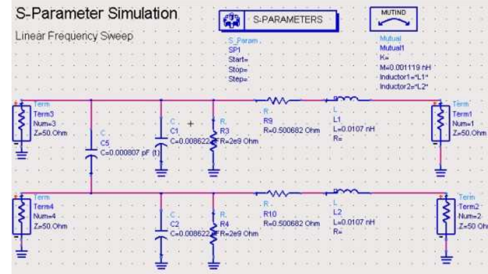


Fig. 2: Scheme of lumped element model of two coupled microstrips.

in Fig.1 is $50\mu m$, which is much smaller than wavelengths in our study in which the simulation frequency range is from 1GHz to 60GHz. The coupled microstrips can thus be treated as two parallel lumped line segments as shown in Fig.2.

We analyze the effects of process-induced variations on coupled microstrips by studying the behavior of each relevant lumped element in the lumped model while applying different variation values in three process-related parameters:

- w: the width of the conductor;
- t_m: the thickness of the metal layer;
- t_{ox}: the thickness of the dielectric/oxide layer.

There are five relevant lumped elements, including:

- L: the self-inductance of one conductor;
- M: the mutual-inductance between two conductor;
- R: the series resistance;
- C: the capacitance between one conductor and the ground;
- C_p: the capacitance between two conductors.
- G: the conductance between one conductor and the ground.

Notice that the manufacturing variations will be applied to only one of the conductors. This is because the coupled microstrips are originally symmetrical when 0% variation is applied.

B. Simulation Results

Next, we will give some conclusions drawn from our simulation results. A large amount of simulation experiments have been conducted. We will take one of them as an example: the series resistance R.

There is a group of four plots (Fig.3) where Fig.3a is its absolute value as a function of the frequency and the parameter variation; Fig.3b shows a cluster of its normalized values at all simulation frequencies with respect to the variation in percentage; Fig.3c compares the simulation result with its 1st and 2nd order approximations at 30GHz and Fig.3d shows its sensitivity at the designed value of the parameter, i.e., 0% parameter variations, over the frequency range.

We should note that the calculation of the 1st order approximation in practice should depend on the distribution of errors with respect to parameter variations so as to obtain an optimum approximation. For instance, if the distribution is uniform, a *least square fit line* over the target range of parameter variations is a better choice while a weighted *least square fit* may be used for a non-uniform error distribution. In the last plot, the sensitivity refers to the slope of the 1st order approximation.

In summary, the following conclusions can be drawn from the simulation results:

1) The series resistance R increases while the frequency goes up as shown in Fig.3b where the curves spread around the design value. This is due to the skin effects and the current crowding;
2) The inductances, both self-inductance L and mutual inductance M become smaller when the frequency goes up, as expected;
3) Oppositely, the capacitance is not a function of frequency as expected;
4) We can see in Fig.3c a perfect agreement between simulation results and the 2nd order approximation;
5) Simulation results can be linearly approximated. Slight deviations are observed;
6) Obviously, we can see from 3) that the sensitivity of capacitances is independent of the frequency. While for other lumped elements, their sensitivities to variations are all clear functions of frequency; thus when we incorporate the variation sensitivities in our parametric model description (as will be introduced in the next section), their frequency dependency should be considered as well.

C. A Simple Example

Finally, we would like to show an illustrative example of a parametric model of coupled microstrips. The output of the model in this example is only the self-inductance (L) for simplicity reason. The model aims at capturing the behavior of L versus process-induced variations and the frequency. There are four inputs, namely the frequency (f) and variations in the conductor width (Δw), the metal thickness (Δt_m) and the oxide thickness (Δt_{ox}):

The model of L is:

$$L = L_0(f) + L'(f, \Delta w, \Delta t_m, \Delta t_{ox}) \tag{1}$$

where L' is the sensitivity of L as a function of parameter variations as well as the frequency (Fig.4). In this example, we assume the variations in three parameters are all -10% and the simulation frequency is $30GHz$.

TABLE I: Comparison of L obtained from the 1st order model and the simulation, i.e., 0th order.

Designed L	simulated L	Modeled L	Deviations	
L_0	L_{sim}	L_{model}	0th order	1st order
$0.01010327nH$	$0.010723nH$	$0.010693nH$	6.14%	2.75%

Thus we can obtain a model (2) utilizing a 1st order approximation to capture the effects of parameter variations whose behavior with respect to frequencies is followed with a least square fit line. This model description can be written as,

$$\begin{aligned} L_{model} &= L_0(f) + L'(f, \Delta w, \Delta t_m, \Delta t_{ox}) \\ &= L_0(f) + L'_{\Delta w}(f)\Delta w + L'_{\Delta t_m}(f)\Delta t_m \\ &\quad + L'_{\Delta t_{ox}}(f)\Delta t_{ox} \end{aligned} \tag{2}$$

where

$$\begin{aligned} L'_{\Delta w}(f) &= L'_{\Delta w}(0) + L''_{\Delta w}(f)f; \\ L'_{\Delta t_m}(f) &= L'_{\Delta t_m}(0) + L''_{\Delta t_m}(f)f; \\ L'_{\Delta t_{ox}}(f) &= L'_{\Delta t_{ox}}(0) + L''_{\Delta t_{ox}}(f)f. \end{aligned} \tag{3}$$

Table-I compares the self-inductance L given by the model (L_{model}) with the simulation result (L_{sim}) at $30GHz$ with -10% variation in three parameters.

IV. Integrated Inductors

A. Simulation Setup

In order to study the effects of process-induced parameter variations for integrated inductors, a parameterized compact model LSIM3.1 (Fig.5) which has been verified by measurement results is utilized. The LSIM3.1 model was developed for spiral inductors with a few parallel current paths for Q-factor modeling improvement and symmetrical layouts with a center tap for differential use [10].

We have conducted a great amount of simulation experiments on three common types of spiral inductors, namely circle, octagonal and square inductors with various geometries and several typical processes. Specifically, simulation processes include QuBIC4, C90LP, C65LP and CMOS18. Inductor geometries vary in several design parameters, such as the number of turns, inductor diameters, the thickness of dielectric layers, the space between neighboring tracks, the width of conductor tracks, the thickness of metal layers and the thickness of substrate where the last three are the manufacturing variation parameters studied in the paper.

B. Simulation Results

The influence of variations on two key design factors (i.e. the maximum quality factor (Q_{max}) and the effective inductance (L_{Qmax}) at the frequency where Q_{max} lies) of integrated inductors are extracted from the simulation results. Table-II and III display the ranges of variabilities (in percentage) of Q_{max} and L_{Qmax} respectively for some geometric variations,

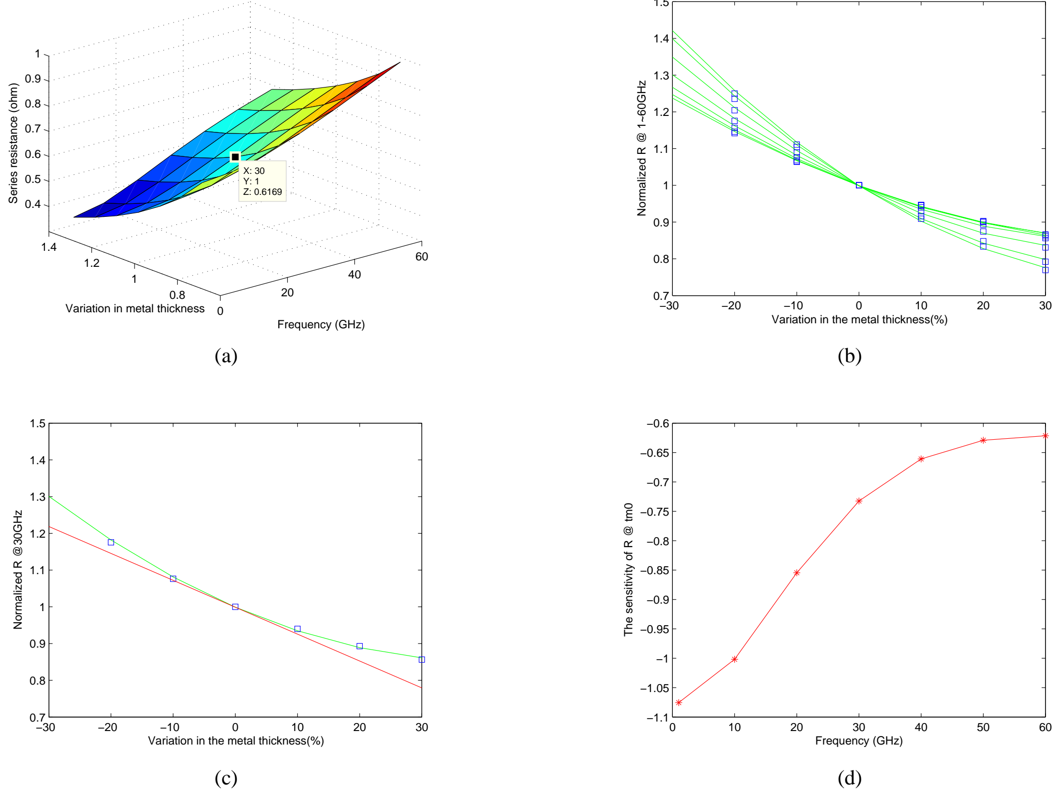


Fig. 3: Simulation results. Blue squares: simulation results; Green lines: 2nd order approximation; Red lines: 1st order approximation.

namely the width of conductor tracks (w), the thickness of metal layers (t_m) and the thickness of substrate (t_{sub}).

From Table-II we can observe that some manufacturing variations have strong impacts on the maximum Q-factor. The variability of Q_{max} caused by variations in w can be almost 20% while the variations in t_m may induce a variability up to 17.31%. In other words, the mismatch in Q_{max} due to manufacturing variations should not simply be neglected. Circuit designers should be able to be aware of these mismatches and decide whether they need to be considered or modeled under specific circumstances. On the other hand, manufacturing variations have much less influence on the effective inductance L_{Qmax} at the Q_{max} frequency. Within all simulation experiments, a maximum mismatch of nearly 6% in L_{Qmax} is caused by variations in w or t_m. The ground shielding successfully isolates on-chip inductors and the substrate, so that the substrate thickness t_{sub} does not play a role in influencing neither Q_{max} nor L.

C. Case Study

An octagonal planar spiral inductor with a Q_{max} around 15 at 2.5GHz is simulated in the case study. This 5-turns inductor has a typical dimension of $300\mu m$ in the outer-diameter and $176\mu m$ in the inner-diameter as well as a typical set of geometric parameters of $10\mu m$ in the track width and $3\mu m$ in track spaces. Such a symmetrical inductor with a center tap for differential use is commonly used in RF circuits like voltage control oscillators (VCO). This particular inductor

TABLE II: Variabilities of Q_{max} in three process-induced parameter variations

Parameter Variation(%)			Variability of Max. Quality Factor(%)		
w	t_m	t_{sub}	Circle Inductors	Octagonal Ind.	Square Ind.
-20	0	0	6.24 $\sim$ 19.21	6.31 $\sim$ 19.21	6.29 $\sim$ 17.13
+20	0	0	-13.33 $\sim$ -6.78	-13.16 $\sim$ -6.82	-13.11 $\sim$ -6.84
0	-20	0	-17.01 $\sim$ -10.41	-17.06 $\sim$ -10.46	-17.31 $\sim$ -11.43
0	+20	0	8.66 $\sim$ 15.45	8.70 $\sim$ 15.55	9.51 $\sim$ 16.33
0	0	$\pm$20	0 $\sim$ 0.032	0 $\sim$ 0.030	0 $\sim$ 0.033

TABLE III: Variabilities of L_{Qmax} in three process-induced parameter variations

Parameter Variation(%)			Variability of Effective Inductance(%)		
w	t_m	t_{sub}	Circle Inductors	Octagonal Ind.	Square Ind.
-20	0	0	3.33 $\sim$ 5.23	3.34 $\sim$ 5.62	3.48 $\sim$ 5.89
+20	0	0	-4.13 $\sim$ -2.75	-4.2 $\sim$ -2.74	-4.95 $\sim$ -2.76
0	-20	0	0.72 $\sim$ 1.84	0.74 $\sim$ 1.94	0.67 $\sim$ 2.05
0	+20	0	-4.95 $\sim$ -0.75	-6.28 $\sim$ -0.82	-5.63 $\sim$ -0.76
0	0	$\pm$20	0.028 $\sim$ 0.076	0.036 $\sim$ 0.073	0.040 $\sim$ 0.072

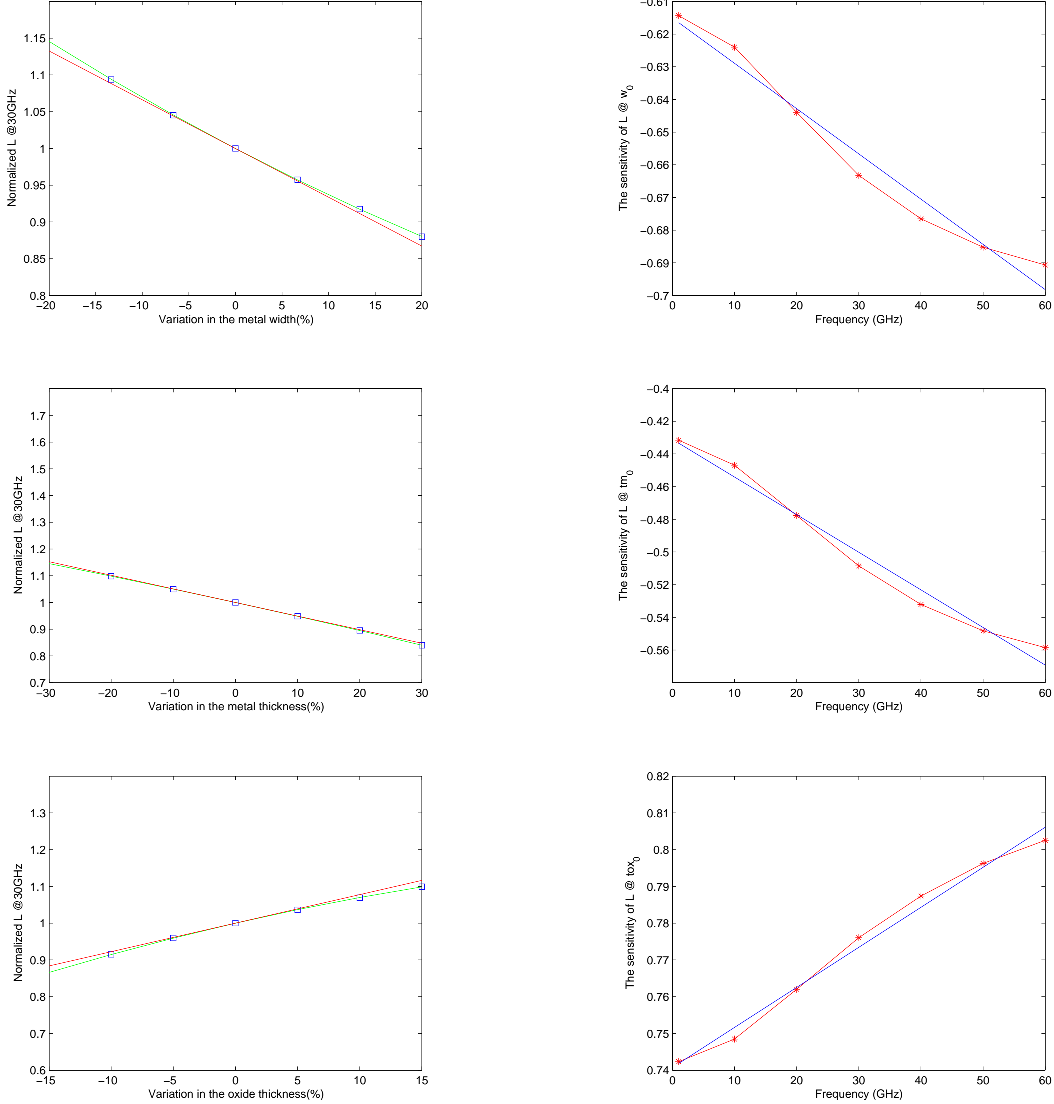


Fig. 4: Left column: Approximation plots of normalized L versus parameter variations at $30GHz$. Blue squares: simulation results; Green lines: 2nd order approximation; Red lines: 1st order approximation. Right column: Sensitivity plots of L versus the frequency. Red stars: simulation results. Blue lines: 1st order approximation.

structure was compared to the measurement results in process QuBIC4M6 (the thickness of ML6 is $3.05\mu m$) with medium resistivity substrates [10].

We know from Table-II and III that the process-induced variations in w and t_m are the major factors affecting Q_{max} and L_{Qmax} while the substrate thickness has a tiny impact. Therefore we only consider w-variation (Δw) and t_m-variation (Δt_m) as the parameters of the model in the case study. Based on practical considerations, we assume a process-induced variation of -5% in w and -20% in t_m.

Table-IV gives an overview of the inductor structure under study, manufacturing variations and the induced property variabilities. There is nearly 10% deviation of Q_{max} from the designed value of 14.4304, from which we can see the necessity of bringing manufacturing variabilities into circuit simulations.

TABLE IV: Geometric parameters and design criteria of the case inductor.

Target Geometric Parameters		Parameters Variations(%)	
w_0	t_{m0}	Δw	Δt_m
$10\mu m$	$3.05\mu m$	-5%	-20%
Designed Criterion Factors		Deviations	
Q_{max}	$L_{Qmax}(nH)$	ΔQ_{max}	ΔL_{Qmax}
14.4304	11.011	-9.3%	2.3%

Based on the simulation results, we study the behaviors of design criterion factors with respect to parame-

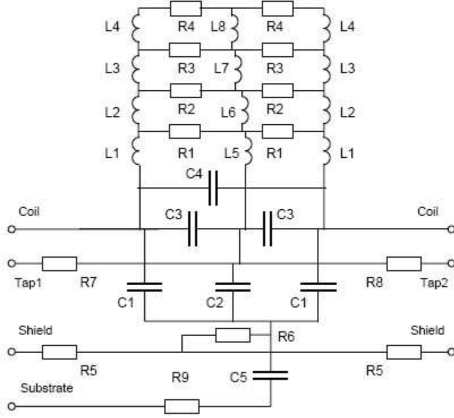


Fig. 5: LSIM3.1 equivalent circuit. [10]

ter variations and find out an appropriate order approximation. We intend to use variation-aware lumped elements in the compact model (Fig.5) to capture the effects of manufacturing variations, resulting in a model description as $Q_{max}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m))$ and $L_{Qmax}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m))$.

To achieve it, we analyse the behaviors of the three groups of lumped elements (R, L and C) with respect to process-induced parameter variations respectively. But here we will only present R as an example.

D. Resistance: $R(\Delta w, \Delta t_m)$

The behavior of resistances with respect to parameter variation Δw is shown in Fig.6a, from which we can see that variations in metal width have no effects on resistances. This is because of a combined effort of the current crowding and the skin effect where the current crowding is the dominant factor [11] [12].

Metal thickness variations, on the other hand, should be a key factor as indicated in Fig.6b where $R_1 - R_4$ represent for the resistances of inductor tracks. The maximum deviation of $1^{st}-$order approximations from simulation results is 3.93% in the case study where the parameter variation Δt_m is -20%. $R_5 - R_9$ are not functions of variations in this metal layer (ML6 of QuBIC4 in the case study) because they stand for other resistances in the ground shielding, the center tap which are not on the same metal layer as the inductor.

The 1st-order variation-aware model description of resistance can be written as,

$$\begin{aligned} R(\Delta w, \Delta t_m) &= R_0 + R_w \Delta w + R_{tm} \Delta t_m \quad (4) \\ &= R_0 \times [1 + \Delta R_w \Delta w + \Delta R_{tm} \Delta t_m] \end{aligned}$$

Similarly, we can derive the 1st-order variation-aware model description of capacitance and inductance:

$$\begin{aligned} C(\Delta w, \Delta t_m) &= C_0 + C_w \Delta w + C_{t_m} \Delta t_m \quad (5) \\ &= C_0 \times [1 + \Delta C_w \Delta w + \Delta C_{t_m} \Delta t_m] \end{aligned}$$

TABLE V: Design criterion factors' designed values, process/manufacturing values, approximated values from the 1st-order model and its deviation from process values

Design Factor	Designed Value	Process Val.	Approx. Val.	Deviation
Q_{max}	14.4304	13.0900	13.32	1.76%
$L_{Qmax}(nH)$	11.011	11.259	11.26	0.0089%

$$\begin{aligned} L(\Delta w, \Delta t_m) &= L_0 + L_w \Delta w + L_{t_m} \Delta t_m \quad (6) \\ &= L_0 \times [1 + \Delta L_w \Delta w + \Delta L_{t_m} \Delta t_m] \end{aligned}$$

Based on (5), (6) and (7), the design criterion factors Q_{max} and L_{Qmax} as functions of variation-aware lumped elements can be derived as, $Q_{max}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m))$ and $L_{Qmax}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m))$.

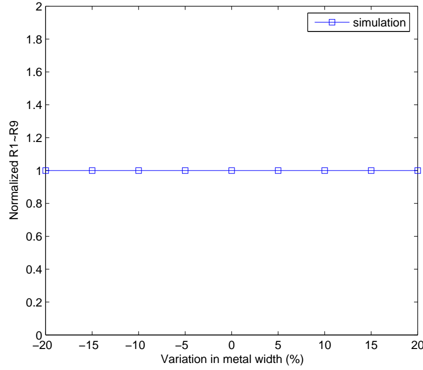
For the case study, we have

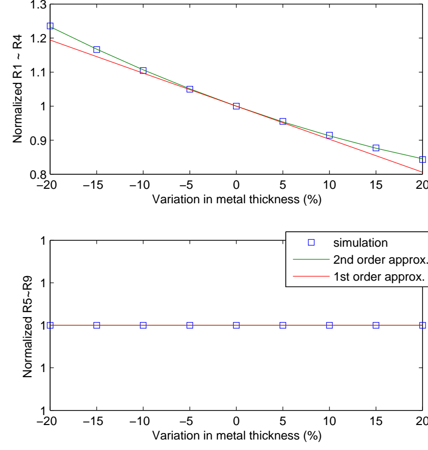
$$\begin{aligned} & Q_{max}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m)) \\ =\ & Q_{max}(R(-0.5\%, -20\%), C(-0.5\%, -20\%), \quad (7) \\ & L(-0.5\%, -20\%) \\ =\ & 13.32 \quad (8) \\ & L_{Qmax}(R(\Delta w, \Delta t_m), C(\Delta w, \Delta t_m), L(\Delta w, \Delta t_m)) \\ =\ & L_{Qmax}(R(-0.5\%, -20\%), C(-0.5\%, -20\%), \quad (9) \\ & L(-0.5\%, -20\%) \\ =\ & 11.26nH \quad (10) \end{aligned}$$

Table-V compares the values of Q_{max} and L_{Qmax} obtained from the 1st-order model to simulation results (i.e., values after manufacturing process). We read a small deviation of less than 2% in Q_{max} and a tiny deviation around 0.009% in L_{Qmax}, which, together with the modeling process described in this section, demonstrates the possibility and the effectiveness of describing variation-aware Q_{max} and L_{Qmax} based on $1^{st}-$order approximation.

E. Statistical Study

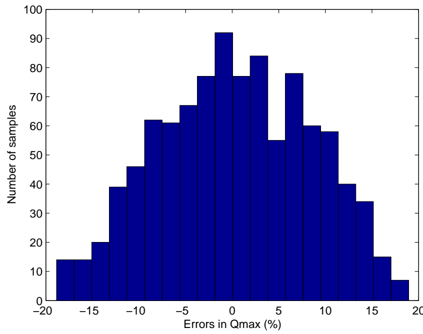
A statistical study on the deviations of Q_{max} and L_{Qmax} due to a 0th-order approximation and a 1st-order approximation was conducted by randomly varying two most influencing parameters, w and t_m by $\pm 10\%$ and $\pm 20\%$ respectively (using a uniform distribution). The total number of samples is 1000 and the results are shown in Fig.7. The average deviation (absolute values) of Q_{max} using 0th order approximation is 6.81% and drops down to 0.23039% using the 1st order approximation. While 0th order approximation is utilized, there are 41.4% of the samples with a mismatch smaller than 5% and 75% samples with a mismatch smaller than 10%. With 1st order approximation, more than 50% samples have a mismatch smaller than 0.2% and 80% have a mismatch smaller than 0.4%. As to L_{Qmax}, the average deviations using 0th and 1st order approximation are 1.1085% and 0.064532% respectively. Around 50% samples have a mismatch smaller than 1% using 0th order approximation and 80% samples have a mismatch smaller than 0.1% using 1st order approximation.

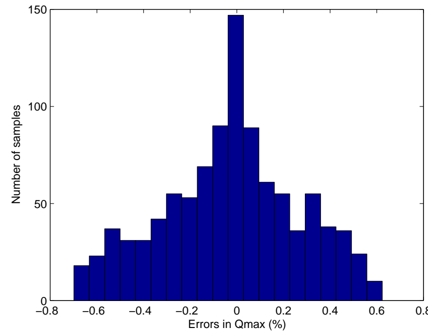


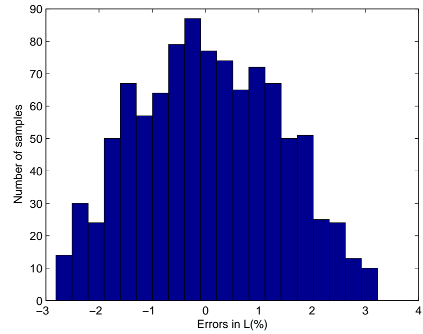


(a) (b)

Fig. 6: Plot of resistances R1-R4 and R5-R9 versus parameter variations Δw and Δt_m. Blue squares: simulation results. Green lines: $2^{nd}-$order approximations. Red lines: $1^{st}-$order approximations.







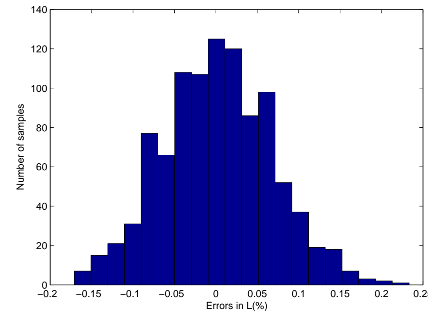


Fig. 7: A comparison between the deviations in Q_{max} and L_{Qmax} caused by a 0th order approximation (the upper histogram) and a 1st order approximation (the bottom histogram). The x-axis indicates the mismatch in percentage, and the vertical axis shows the number of samples.

V. Conclusion

In this paper, we studied the effects of process-induced variations on two integrated passive components, namely two coupled transmission lines and integrated inductors, utilizing 3d em simulations and a compact model respectively. We have conducted a large amount of simulation experiments and a few examples to indicate the necessity and possibility of modeling these manufacturing variabilities. For inductors, we have shown that the mismatch in Q-factor while neglecting process-induced variations can be in the order of 10% for

typical manufacturing tolerances, which will drop down to around 2% if a 1st-order approximation is applied.

REFERENCES

[1] A. Labun, *"Rapid Method to Account for Process Variation in Full-chip Capacitance Extraction"*, *IEEE Trans. CAD of Integrated Circuits and Systems*, vol.23, pp.941-951, 2004.

[2] Y. Liu, L.T. Pileggi, E. Acar, S. Nassif, *"Assessment of True Worst Case Circuit Performance under Interconnect"*, *Quality Electronic Design*, pp.431-436, 2001.

[3] J.K. White, L. Daniel, *"Numerical Techniques for Extracting Geometrically Parameterized Reduced Order Interconnect Models from Full-wave Electromagnetic Analysis"*, *Antennas and Propagation Society International Symposium*, vol.3, pp.20-25, 2004.

[4] W. Burleson, V. Venkatraman, *"Impact of Process Variations on Multi-level Signaling for On-chip Interconnects"*, *"Proceedings of the 18th International Conference on VLSI Design"*, pp.362-367, 2005.

[5] E. Demircan, *"Effects of Interconnect Process Variations on Signal Integrity"*, *International SOC Conference*, pp.281-284, 2006.

[6] A. Nieuwoudt, Y. Massoud, *"Variability-aware Multi-level Integrated Spiral Inductor Synthesis"*, *IEEE Trans. on CAD of Integrated Circuits and Systems*, vol.25, pp.2613-2625, 2006.

[7] V. Venkatraman and W. Burleson, *"Impact of Process Variations on Multi-level Signaling for On-Chip Interconnects"*, *Proceedings of the 18th International Conference on VLSI Design*, pp.362-367, 2005.

[8] L. Scheffer, *"Overview of On-Chip Interconnect Variation"*, *SLIP*, pp.761-764, 2006.

[9] B.E. Stine, D.S. Boning, J.E. Chung, L. Camilletti, F. Kruppa, E.R. Equi, W. Loh, S. Prasad, M. Muthukrishnan, D. Towery, M. Berman and A. Kapoor, *"The Physical and Electrical Effects of Metal-Fill Patterning Practices for Oxide Chemical-Mechanical Polishing Processes"*, *IEEE Trans. Electron Devices*, vol.45, pp.665-679, 1998.

[10] L.F. Tiemeijer, R.J. Havens, Y. Bouttement and H.J. Pranger, *"Physics-Based Wideband Predictive Compact Model for Inductors With High Amounts of Dummy Metal Fill"*, *IEEE Trans. Microwave Theory and Techniques*, vol.54, pp.3378-3386, 2006.

[11] R. Faraji-Dana and Y.L. Chow, *"The Current Distribution and AC Resistance of a Microstrip Structure"*, *IEEE Trans. Microwave Theory and Techniques*, vol.38, pp.1268-1277, 1990.

[12] L.T. Hwang and I. Turlik, *"A Review of the Skin Effect as Applied to Thin Film Interconnections"*, *IEEE Trans. Components, Hybrid, and Manufacturing Technology*, vol.15, pp.43-55, 1992.