

Optimum Segmentation for High Speed Current Steering Digital-to-Analog Converters

P.C.W. van Beek¹, K. Doris², J.A. Hegt¹ and A.H.M. van Roermund¹

¹ Technische Universiteit Eindhoven, Mixed-signal Microelectronics Group, EH 5.05

P.O.Box 513, 5600 MB Eindhoven, The Netherlands

Phone: +31 40 247 5131, email: p.c.w.v.beek@tue.nl

² Philips Research Laboratories, Prof. Holstlaan 4, 5656 AA Eindhoven, The Netherlands

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Abstract— When designing a Current Steering Digital to Analog Converter, a major architectural parameter is the number of bits in the partitioning between thermometer and binary segments. This is called segmentation. The DAC designer has to choose the optimum amount of segmentation taking into account the physical problems associated with the segmentation. Current steering DACs with a low amount of segmentation have the advantage that they are simple. They only need a few current sources and switches. A disadvantage of low segmentation is the possible larger DNL compared to the converters with larger segmentation. Converters with larger segmentation have a lower DNL, but the problems associated with the output conductance, capacitance and synchronization increase and also the area and power that is needed increases.

I. INTRODUCTION

When designing a high speed digital-to-analog converter (DAC) many tradeoffs have to be taken into account. These include the type of the DAC (current steering or a voltage output DAC), the number of bits and required speed. For high speed DACs usually a current steering converter is selected because of the speed advantages of this converter type with respect to the voltage output DAC. In most current steering DAC designs a combination of binary and thermometer code weighting is used. The thermometer code is used for the Most Significant Bits (MSBs), while binary code for the Least Significant Bits (LSBs) is used. This is called segmentation: 0% segmentation means a fully binary converter and 100% segmentation means a full thermometer code converter. The DAC designer has to choose the optimum amount of segmentation taking into account the physical problems associated with the segmentation. Current steering DACs with a low amount of segmentation have the advantage that they are simple. They only need a few current sources and switches. The disadvantage of low segmentation is the possible larger DNL compared to the convert-

ers with larger segmentation. Converters with larger segmentation result in a lower DNL, but the problems associated with the output conductance, capacitance and charge feedthrough increase and also the area and power that is needed increases. In addition, due to the larger area required and the larger difference in output impedance between the lowest output code and the highest output code, the timing errors become more dominant[1]. Therefore an optimum segmentation has to be found by the designer.

II. CURRENT STEERING D/A CONVERTER

The basic principle of current steering DACs is the summation of currents according to the input. The special case of a binary current steering converter is shown in figure 1. The current sources are connected parallel to each other. These current sources are connected to switches; the switches connect the current source to the output node. The switches are controlled by the input code of the DAC. The output current of the DAC is therefore proportional to the input code word. The output node of the DAC is connected to a resistor. This resistor converts the output current of the DAC into a voltage.

A. Binary weighted current steering D/A Converters

In the binary weighted current steering DAC the current sources, as shown in figure 1, are scaled according to the binary principle. This means that output current of the i^{th} current source is equal to $2^i \cdot I_{LSB}$, where I_{LSB} is the current of the Least-Significant Bit (LSB). The output of an ideal N -bit binary weighted current steering DAC is given by

$$\begin{aligned} I_{out(w)} &= 2^{(N-1)} I_{LSB} \cdot b_{N-1} + \dots & (1) \\ &+ 2 I_{LSB} \cdot b_1 + I_{LSB} \cdot b_0 \\ &= I_{LSB} \cdot w, \end{aligned}$$

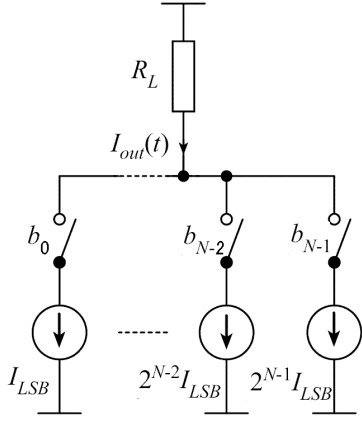


Fig. 1. Circuit diagram of a basic binary current steering Digital-to-Analog converter

where w is the digital input given by

$$w = 2^{(N-1)} \cdot b_{N-1} + \dots + 2 \cdot b_1 + b_0 = \sum_{m=0}^{N-1} 2^m \cdot b_m, \quad (2)$$

where b is the input code applied to the converter.

The advantage of this topology is that it is simple, for a 12-bit converter there are only 12 current sources needed and an equal number of switches. In addition there is no need for decoding logic, all switches are controlled directly by the input bits.

There are a number of disadvantages with this topology [2]. One disadvantage is the required matching. For a binary scaled converter the Most-Significant Bit (MSB) has to be matched within $\frac{1}{2}$ Least-Significant Bit (LSB) to the sum of all other bits. This is difficult to achieve, because of the spread, such matching cannot be guaranteed for a converter with 12 bits or more. Therefore this architecture does not guarantee monotonicity. When a converter is non-monotonic a local sign change of the transfer characteristic slope occurs. Monotonicity may be paraphrased as 'a larger input results in a larger output'. Another disadvantage is because of the large ratio between the LSB and the MSB, it is difficult to synchronize the switching. Matching is an issue for all bit transitions, but the severity of the problem is proportional to the weight of the bit, resulting in a typical differential nonlinearity (DNL) plot, as shown in figure 2a. Another main disadvantage is the mid-code transition (0 111 111 111 \rightarrow 1 000 000 000). Due to the dynamic behavior of the switches, and the large difference between the switches, the binary weighted DAC can create glitches, as those shown in figure 2b. At the half scale transition the most significant current source is

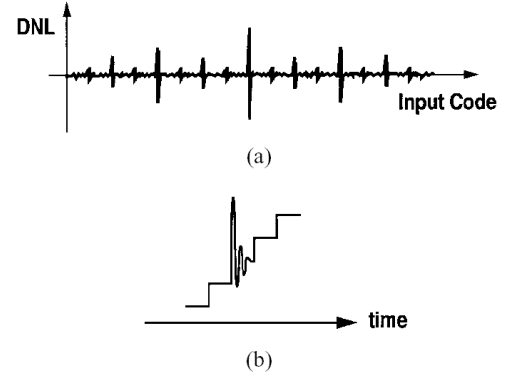


Fig. 2. Matching and glitch problems of a binary-weighted DAC

switched on / off and the other $N-1$ current sources are switched off / on. The current sources are constructed with unit current cells, each switching a current of I_{LSB} . Assuming a normal distribution for each current source with a standard deviation of $\sigma(I)$ then the mid scale step $\sigma(\Delta I)$ is determined by [3]

$$\sigma(\Delta I) = \sqrt{2^N - 1} \frac{\sigma(I)}{I}, \quad (3)$$

where I is the current switched by each current source and N is the number of bits. This $\sigma(\Delta I)$ gives an approximation for the DNL.

Generally fully binary scaled converters do not exceed ten bits of resolution, due to mismatches in the reference scales. Higher resolutions require laser trimming or self-calibration techniques [4].

B. Thermometer code D/A Converters

Another topology is used by thermometer coded DACs. In this topology all the current sources draw the same current. The binary input code is first converted into a thermometer code. The thermometer code then controls the switches of the current sources. For a N -bit converter $2^N - 1$ current sources are needed. This topology has several advantages compared with the binary weighted topology. One of the advantages is that the converter is guaranteed monotonic. Because, assuming that all current sources are positive, the analog output is always increased as the digital input increases. Another advantage is that glitches are non-existent. At the mid-code transition (0 111 111 111 \rightarrow 1 000 000 000), only one current source has to switch as the digital input only increases by one. Also the matching requirement is less strict: 50% matching of the unit current source is good enough for DNL of 0.5 LSB.

Performing similar calculations as in equation (3) the thermometer code architecture gives the following results,

$$\sigma(\Delta I) = \frac{\sigma(I)}{I}, \quad (4)$$

where I is the current of each current source. The error between two consecutive codes is the deviation of the additional current sources.

Thermometer code topology also has several disadvantages. One of the disadvantages is the complexity of the design. For a full single ended thermometer code DAC with 12 bits, 4095 current sources and switches are needed. This results in a large IC layout, which possibly results in matching problems, and a larger timing uncertainty of the switches.

C. Thermometer/Binary code D/A Converters

In most designs a combination of binary and thermometer code weighted DACs are used. The thermometer code is used for the MSBs and the binary code for the LSBs. This is called segmentation, 0% segmentation means a fully binary converter and 100% segmentation means a full thermometer-code converter. An important question is the optimal choice for the number of binary bits and the number of thermometer code bits.

A thermometer code current source is called a unit current source. In this text the current of this unit is equal to $I_T = 2^B \cdot I_{LSB}$, where B is the number of binary sources. The current of the smallest binary current source is equal to I_{LSB} .

The advantages of the binary and the thermometer code DAC can be combined by choosing the segmentation. The DAC can then be optimized with respect to the performance, area, power and other issues.

If the segmentation decreases then the area and power needed is reduced when the same components are used such as the drivers and latches, but the glitches will increase.

If on the other hand the segmentation is increased then the power and the area increases also and the glitches decrease, if all components are kept the same. Other effects such as dynamics and timing uncertainty are also influenced by the segmentation. The question is the amount of influence on the performance of the DAC with respect to the segmentation.

III. MSB-LSB GLITCHES

Especially historically the MSB-LSB glitch at the mid-code transition determined the optimum segmentation, see II-A. In [5] a segmentation is chosen

for a 10 bit converter. The MSB-LSB glitches and DNL versus the required area and power determined the segmentation choice. The optimum segmentation, which can be found in the above mentioned publication, can be found in figure 3. The strategy of this article is to maximize the segmentation as far as the area and power allows. Several authors follow this guideline.

The approximation of the DNL of the segmented architecture is similar to the binary architecture. The result for the most critical transition is

$$\sigma(\Delta I) = \sqrt{2^{B+1} - 1} \frac{\sigma(I)}{I}, \quad (5)$$

where B is the segmentation. For $B = 0$ the DAC is full thermometer code DAC, for $B = N - 1$ the DAC is the full binary implementation.

This MSB-LSB glitch is important in the determina-

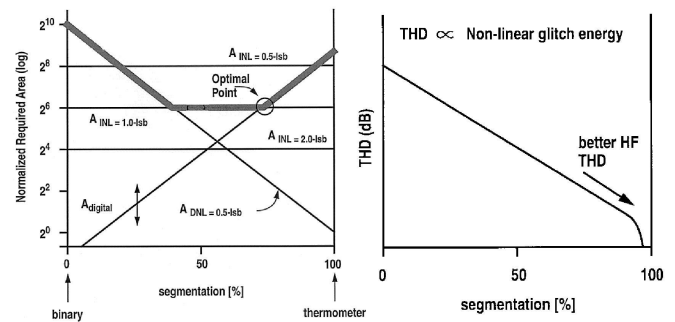


Fig. 3. Normalized required area versus percentage of segmentation in [5]

tion of the optimal segmentation, but there are other sources of errors, which also determine the optimal segmentation. Others argue that this is not the dominant error for high frequency DACs and also because adopting this strategy creates other problems which can be more dominant. It can be concluded that if one sees the problem independently of other problems, the maximized segmentation is always the best option. In comparison to the other problems that are dependent of the segmentation, this method is not always the best solution. The maximized segmentation can cause other problems such as increased switching activity, hence more power supply problems can occur. One can conclude that things are not that clear. For example, timing errors caused in the identical thermometer unit current cells are not taken into account.

IV. OUTPUT CONDUCTANCE

When the current source is made with transistors the output conductance of the current source is not

zero. This non-zero output conductance contributes to a non-linear error. This is because the output impedance of the DAC is not constant anymore, but a function of the code applied to the DAC, see figure 4. The performance of the DAC depends on the conductance ratio [6]

$$\rho_G = \frac{G_S}{G_L} = G_S R_L, \quad (6)$$

where G_S is the output conductance of the current source and $G_L = 1/R_L$ is the load conductance. The

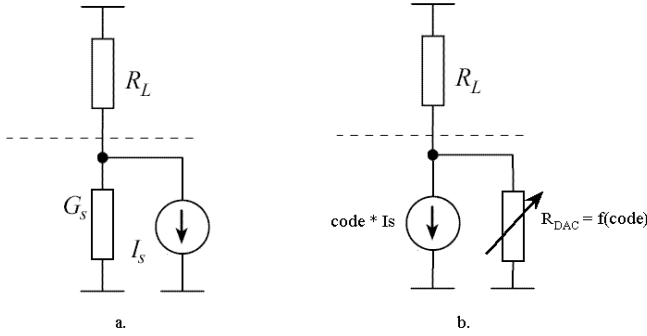


Fig. 4. a. Linearized Model of the Unit Current source with non-zero output conductance, b. Combination of more current source gives a code dependant output conductance

error caused by the non ideal output conductance can be compensated by the use of an amplifier, as illustrated in figure 5. This amplifier creates a virtual ground node. The load resistance R_L is then approximately zero, as a result ρ_G becomes zero and the output impedance no longer contributes to a non-linear error. Unfortunately the amplifier has a number of drawbacks such as limited speed, linearity, output voltage swing and driving capability.

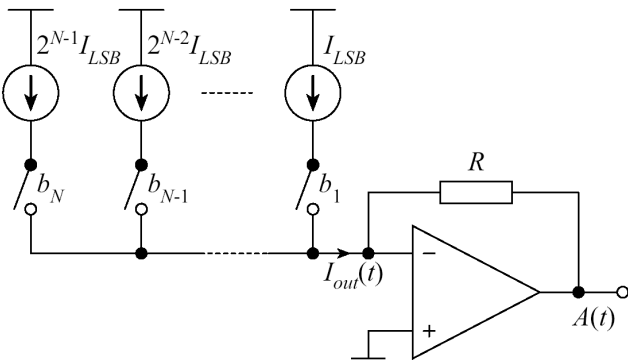


Fig. 5. Use of an amplifier to create a virtual ground

In the DAC the output conductance depends on

the number of current sources connected to the output and is therefore signal dependent. The output conductance of the unit current source has to be low enough so that its influence on the INL is negligible. The output voltage [7] is given by

$$V_{out}(n) = \frac{nR_L}{1 + nR_L G_S} I_{unit}, \quad (7)$$

where I_{unit} is the current of the current source, G_S is the output conductance of the unit current source and n is the number of current sources turned on. The relation between the output conductance of the current source and the INL error due to the conductance of the current source [8], is given by

$$INL = \frac{I_{unit} R_L^2 N^2}{4R_S}, \quad (8)$$

where I_{unit} is the LSB current, $R_S = 1/G_S$ is the output resistance of the unit current source and N the total number of current sources.

The SNDR can also be expressed as a function of the conductance ratio. The SNDR does not depend on the segmentation that is used in the DAC. The SNDR [9] for a full scale sinusoid input can approximated by

$$SNDR = \frac{1}{6\rho_G \cdot \left(2^{2N+1} \cdot \left(1 + \frac{1}{8}\right)\right)}, \quad (9)$$

in dB this is equal to

$$SNDR = -6(N - 0.4) - 20 \cdot \log_{10} \rho_G \text{ dB}, \quad (10)$$

where ρ_G is given by equation (6). The SFDR of the DAC with limited output resistance is equal to

$$SFDR = \left[1 + \frac{1}{\rho_G \cdot 2^{N-1}} \cdot \left(1 + \sqrt{1 + 2^N \cdot \rho_G}\right)\right]^2, \quad (11)$$

If we assume that ρ_G is small, the SFDR can be approximated by

$$SFDR = -20 \cdot \log_{10} \rho_G - 6(N - 2) \text{ dB}. \quad (12)$$

Equation (12) shows that with the doubling of the load resistance, the conductance ratio is doubled and the SFDR is decreased by 6 dB. In addition, when the segmentation increases the output conductance decreases, which can result in a lower performance of the DAC.

The output conductance calculated in this section does not take the output capacitance of each current source into account. The analysis given here is valid only for low frequencies.

V. OUTPUT CAPACITANCE

The output capacitance is just like the output resistance dependent on the input code. If the code is changing then also the output capacitance changes. In this section the capacitance problem is viewed with respect to the time-domain effects during switching. The output capacitance and the output resistance determine the settling time of the DAC.

The settling time is the time required for the output of the DAC to reach the final value within the accuracy of the DAC. If the capacitance is changed then also the settling time is changed.

The output capacitance is a function of the input

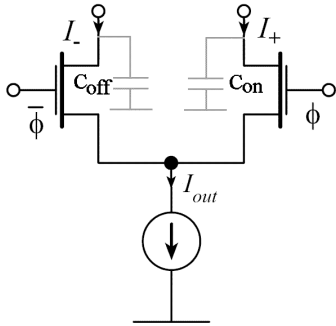


Fig. 6. The capacitance changes with the settling of the switch in the unit current cell

code. The reason for this is that the capacitance at the output of the unit current cell changes when the switch is turned on and off. Simulations of a specific unit current cell showed that its output capacitance was 3fF when it was switched off and 4fF when it was on..

This capacitance change can be modelled by the following figure. The output capacitance as function of

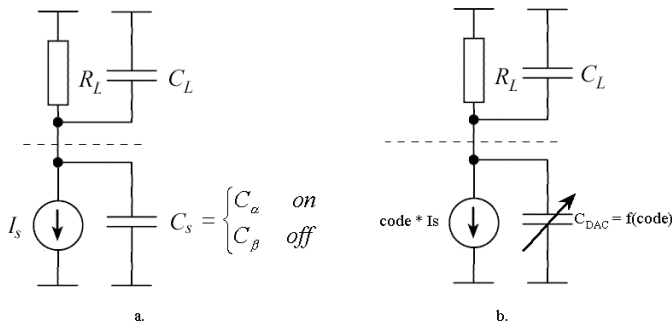


Fig. 7. a. Linearized Model of the Unit Current cell with non-zero output capacitance, b. Combination of more current source gives variable output capacitance

the input code is plotted in figure 8. The output capacitance is calculated with a 7 bit thermometer code

DAC as is given by

$$\begin{aligned} C_{out} &= f(w) \\ &= C_L + C_\alpha \cdot w + (2^B - 1) \cdot C_\beta, \end{aligned} \quad (13)$$

where

$$\begin{aligned} w &= \text{the code applied to the DAC}, \\ C_\alpha &= C_{on} - C_{off}, \\ C_\beta &= C_{off}. \end{aligned} \quad (14)$$

and B is the number of thermometer code bits. Only the difference in the capacitance (C_α) is important. The constant output capacitance $(2^B - 1) \cdot C_\beta$ loads the DAC, but since it is not signal dependent it does not induce distortion.

There are a number of problems caused by the fact that the capacitance is a function of the input signal. The first problem is the signal dependent rise and fall times. The second is its influence on other effects, such as charge feedthrough.

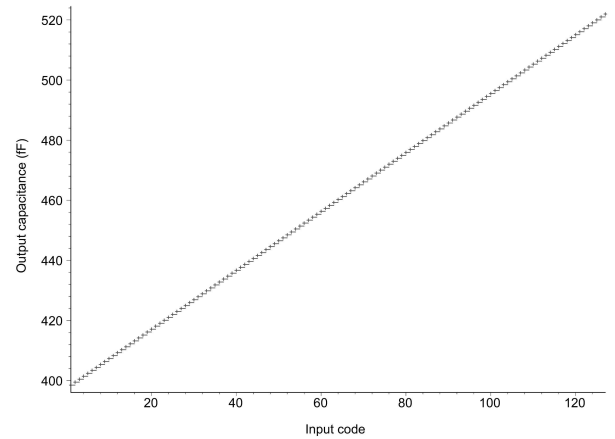


Fig. 8. The output capacitance as function of the input code

A. Signal dependent rise / fall time

The capacitance at the output of the DAC is equal to the sum the capacitance of the load C_L and the sum of unit current cells C_s capacitances. The last capacitance is not constant but changes by the input code. The total output capacitance is therefore equal to equation (13). The output resistance of the DAC, which also changes by the signal is $R_{out} \cong R_s/w$. The settling time can be approximately by

$$\begin{aligned} \tau(w) &= R_L C_\alpha \cdot w + C_{out} R_L \\ &= \tau_s \cdot w + \tau_0, \end{aligned} \quad (15)$$

Only the delay $\tau_s \cdot w$ is important because τ_0 is constant. With a sinusoidal input of $x(t) = A + A\sin(2\pi f_1 t)$, the second order harmonic distortion is given by [10]

$$SDR_2 = 20 \log_{10} \frac{1}{\sqrt{2} J_1(2\pi f_1 \tau_s 2^{B-1})}, \quad (16)$$

where the function $J_q(x)$ defines the Bessel function of the first kind, and B is the number of thermometer current cells.

To obtain useful insight, consider a 7 bit DAC and with an update rate of $f_s = 800 \text{ MS/s}$, i.e. $T_s = 1.25 \text{ nsec}$. The DAC drives an external capacitance of $C_L = 5 \text{ pF}$ and a resistance of $R_L = 25 \Omega$. Assuming that each of the 127 unit current cells adds a capacitance of 1 fF when it goes from the off state to the on state, then $\tau_s = 0.1 \text{ psec}$ then the SDR_2 is equal to 77 dB for a input signal of 20 MHz.

Figure 9 shows the signal to second harmonic distortion as function of the unit delay. For a small output

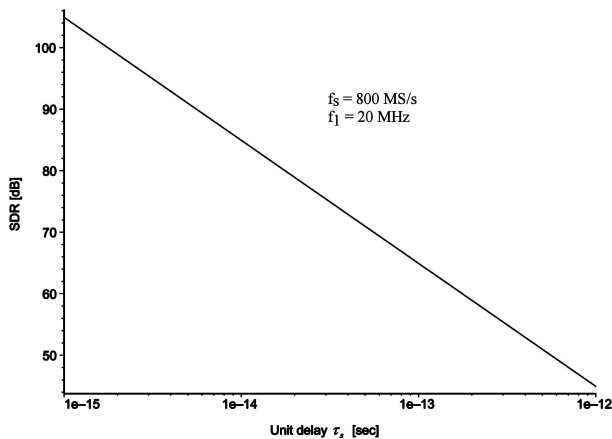


Fig. 9. Signal to second order harmonic distortion as function of the unit delay

capacitance the switching transistors at the output node should be small. On the other hand small transistors have a negative influence on timing accuracy as will be discussed in section VII-B. The use of an amplifier to create a virtual ground reduces the effect of the output capacitance, but the use of an amplifier limits the DAC signal and clock frequency. At higher frequencies the effect of the output capacitance is dominant over the output conductance. When the segmentation is increased also the effect of the output capacitance increases. When the segmentation increases by one bit the number of thermometer cells doubles, while the number of binary cells is reduced by only one. If the elements stays therefore the same

and the segmentation is increased by one bit the output capacitance nearly doubles.

VI. CHARGE FEEDTHROUGH

Charge feedthrough is another physical problem which affects the performance of the DAC. The charge feedthrough is correlated with the input signal. The charge injected into the output node is proportional to the number of current cells that switch.

The concept of charge feedthrough can be illustrated by figure 10. In this figure a unit current cell is shown with the two switches, implemented with transistors. To switch the unit current cell a switching signal is applied as shown in the above mentioned figure. Due to the capacitance between the gate and the drain an amount of charge is injected into the output node.

Two capacitances are responsible for the charge feedthrough. One is the overlap capacitance at the gate to drain, and the other is the channel charge [11]. The overlap capacitance is equal to

$$C_{ov} = W \cdot L_{ov} \cdot C_{ov}, \quad (17)$$

where W is the width of the switch and L_{ov} is the length of the overlap region between the gate and the drain. The charge in the channel is approximated by

$$Q_{ch} = W L C_{ox} V_{out}. \quad (18)$$

Approximately half of this channel charge will be injected into the output node.

This charge injected into the output node will create an initial voltage step of

$$\Delta V \approx \frac{\Delta N \cdot C_{gd}}{C_L + C_{gd} + C_{out}} \Delta V_{in}, \quad (19)$$

where C_{out} is the output capacitance of the DAC which changes by the applied code word and ΔN are the number of current sources, that are changing. C_L is the output capacitance connected to the DAC, and ΔV_{in} is the voltage swing of the signal that is driving the switches. This initial voltage converges to zero after some time.

The capacitance C_{out} depends on the input code as given in section V.

$$C_{out} = f(\text{Code}) = C_\alpha \cdot w + (2^B - 1) \cdot C_\beta, \quad (20)$$

where B is the number of thermometer code bits. The constant capacitance $(2^B - 1) \cdot C_\beta$ does not give any problem and can be treated as an additional output

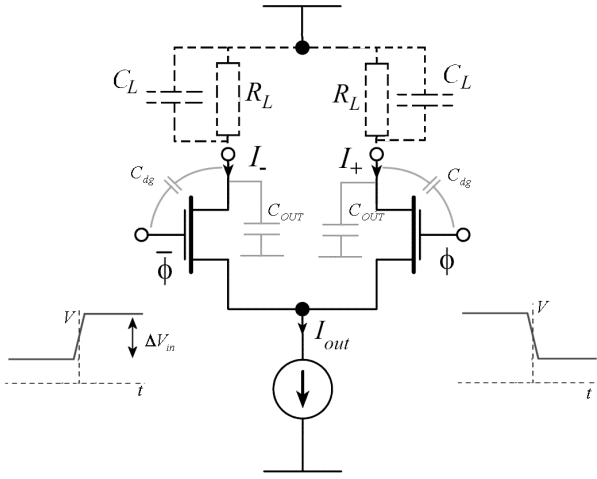


Fig. 10. Illustration for the charge feedthrough

capacitance, but the capacitance $C_\alpha \cdot Code$ does.

Assuming C_α is zero, then the output capacitance of the unit current cell would not depend on the code input word applied to the DAC. The switching signals applied to the gates of the unit current cell are opposite to each other, if one signal rises then the other will fall. The charge injected into one output node is the opposite to the charge injected into the other node. When the capacitance C_α is not assumed zero, as is the case in a design, then the effect of the charge feedthrough depends on the input code applied to the DAC.

Based on equation (19) the charge injected into the output node is in first order proportional to

$$Q_{load} \propto C_{gd} \cdot \Delta V_{in}, \quad (21)$$

where ΔV_{in} is the voltage swing of the signal that is driving the switches, and C_{gd} is the total capacitance between the gate and the drain. The charge feedthrough can be reduced by decreasing C_{gd} , and/or by decreasing ΔV_{in} .

To reduce C_{gd} requires that the size of the switches is reduced. The size of the switches is mainly determined by other limitations. One of the reasons not to reduce the size of the switches is the timing spread, which can increase if the size of the switch is decreased.

The charge feedthrough is also proportional to the voltage swing applied to the transistor. When the control voltage is decreased then the amount of charge injected into the output node also decreases. But the voltage swing is limited by the robustness of the DAC against mismatch and the speed of the DAC.

To compare the influence of the segmentation the assumption is made that the latches, drivers, etc. are identical with increasing segmentation. When the segmentation increases by one bit, then the change in the capacitance at the output node nearly doubles, due to the almost double amount of elements at the output node. Also the number of elements that are switched increases, because for the same input code transition nearly twice as many blocks switch, hence the charge injected into the output node is doubled. Due to the larger number of elements that are switched the effect of the charge feedthrough also increases. Especially due to the code dependent output capacitance of the DAC the charge feedthrough affects the performance of the DAC. Therefore the influence of the charge feedthrough on the performance of the DAC increases when the segmentation increases.

VII. TIMING ERRORS

In this section the effect of the timing errors on the performance of the DAC will be analyzed. Timing errors can be classified in two groups. One type of timing errors are the global errors. The other type of timing errors are local errors.

A. Global Timing errors

The global errors are mainly caused by electrical coupling between different elements. Global timing errors are the same for all elements. Examples of this type of timing errors are clock jitter and supply bounce. All switching chains behave in the same way but in a different manner for each code [1].

B. Local timing errors

The DAC is built with a large number of identical parallel chains, see figure 11. A chain consists of a latch, driver and unit current cell connected to each other. Each chain is located at a different position on the chip, and shows a different behavior than another chain located at another location. Each chain behaves differently because of the limited device matching. If the same signal is applied to these chains then they show different behavior. Timing delays, switch resistance and charge injection are relative to the chains position [1].

Consequently, timing errors are caused by mismatches between the different elements. The local spatial errors again can be divided in two groups, deterministic and stochastic. Examples of deterministic timing errors are timing errors created by the clock network

or by the effect of correlated load on the switches. Stochastic errors are created by stochastic mismatches of the process parameters, such as V_t and β .

In this design of the DAC the data are synchro-

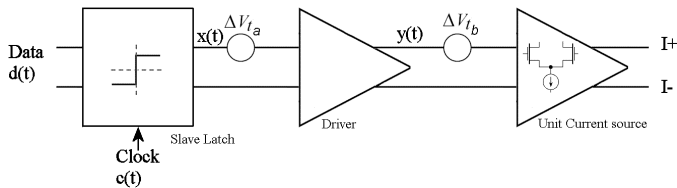


Fig. 11. Local timing errors

nized by the latches. The drivers are placed after the latches, which control the transistors at the output of the DAC. Due to stochastic mismatch between the different elements the data does not arrive at the output at the same time. If this spread in time is too large then the performance of the DAC will be reduced.

The relationship between the performance of the DAC and the timing uncertainty for a full scale sinusoid is given by [1]

$$SDR = 3(N - 1) - 10 \log_{10} (\sigma^2 f_s f_i) - 9.03dB, \quad (22)$$

where σ is the timing spread of the DAC, f_i is the signal frequency, f_s is the sample frequency, and N is the number of thermometer bits. The SDR drops with 20dB/dec with a timing spread σ and with 10dB/dec with the signal frequency and sample rate. For a 7 bit thermometer code converter with a sample frequency of 800 MHz, a signal frequency of 150 MHz and an accuracy of 74 dB the maximum allowable timing spread is about 1.6 psec.

In [5] it is stated that the Total Harmonic Distortion reduces by 6dB with every binary bit which is translated into a thermometer bit. However, this only holds if the timing accuracy of the increased number of thermometer bits stays the same. This is difficult to achieve because every binary bit which is translated into a thermometer bit doubles the amount of thermometer bits. If for example that every time the segmentation increases by one bit, the timing error per element increases as well. For example by

$$\sigma(N) = \sigma \sqrt{2^N}, \quad (23)$$

then equation (22) becomes

$$SDR = -3(N - 1) - 10 \log_{10} (\sigma^2 f_s f_i) - 9.03dB. \quad (24)$$

Instead of gaining 3dB in SDR with every extra thermometer bit, there is a penalty of 3dB. This simple example shows that in order to determine the optimal segmentation the timing error should first be related to the architectural and process parameters.

VIII. CONCLUSION

When the segmentation is increased with one bit then the code dependent output conductance and capacitance will become nearly two times as large, assuming that the same elements are used. The increased segmentation however has a positive influence on the performance of the DAC with respect to the MSB-LSB glitch. In addition, the DNL will decrease when the segmentation increases.

The influence of the conductance of the current sources are only observable at low frequencies. The influence of the output capacitance is for low frequencies less important. At higher frequencies however, the effect of the output capacitance will dominate the effect of the output conductance.

If the timing accuracy stays constant with increased segmentation the performance of the DAC will increase by increasing the segmentation. To know the influence of the increased segmentation on the timing accuracy, information is needed about the circuit mechanisms that generate these errors, and the links of the timing errors with the process parameters, circuit topologies, and architectural parameters. Also the relation with other problems is needed such as the output conductance, capacitance and settling time.

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