

Channel Length and Oxide Thickness Scaling Effects on Low Frequency (1/f) Noise in Metal/High- κ sub-micron MOSFETs

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Abstract - This paper discusses the impact on low-frequency (1/f) noise due to scaling of the channel length and the thickness of the gate oxide in n- and p-MOSFETs. The gate oxide scaling impact is studied as a function of both the SiO₂ interfacial layer and the high- κ gate dielectric thickness. While the scaling is seen to be a strong function of the interfacial layer (IL) thickness, a much weaker dependence is noticed of 1/f noise due to the high- κ layer thickness. Variation of the Equivalent Oxide Thickness (EOT) due to a varying interfacial layer has a stronger impact on 1/f noise in both n- and p-MOSFETs than varying the high- κ layer thickness. Deviations from the classical 1/f noise theory are noticed for short channel lengths (L) in n- and p-MOSFETs, whereby the normalized noise S_{id}/I_d^2 is no longer found to be proportional to 1/L, mainly due to short channel effects at lower L. The observed behavior is quite different from observations in SiO₂ devices and needs to be taken into account for future high- κ 1/f noise modeling.

Index Terms— Device Scaling, Semiconductor Device Noise, MOSFETs, High-K Dielectrics.

I. INTRODUCTION

HIGH- κ dielectric materials will replace conventional silicon dioxide (SiO₂) as gate oxides in MOSFETs for applications below 45 nm nodes. Devices fabricated with Hf-based dielectric materials show promising results, in reducing the gate leakage current [1], though the reliability remains still a cause of concern. Metal gate electrode materials like TiN/TaN are considered in parallel [2] as a replacement for poly-Si gate electrodes due to their significant advantages of lower resistivity, work function (WF) tuning and no poly-depletion issues.

For analog low-power applications of these high- κ devices, one of the important parameters to be considered is the low frequency (LF) noise. LF noise is a cause of concern, as it has

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to be within the critical limits to meet the ITRS roadmap requirement. At the same time, noise analysis can be used as a diagnostic tool [3] to study the quality of gate dielectrics and its interface with silicon. Several studies have pointed out that the noise spectral density is higher for the high- κ devices [4], [5], [6] due to its sensitive nature to gate stack processing resulting in degraded interface quality and an increased defect density.

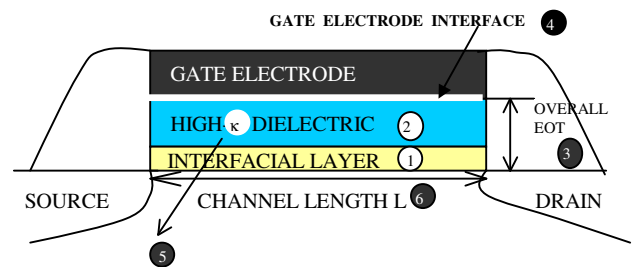


Fig. 1. A typical high- κ MOSFET structure showing the influence of various scaling elements affecting the 1/f noise performance. Six major technological parameters are identified which can have a significant impact on the noise properties of the device.

This work focuses on the impact of scaling high- κ dielectric devices on 1/f noise performance. Figure 1 shows the typical scaling elements that may affect the 1/f noise. These factors are (1) interfacial layer (SiO₂) oxide thickness - t_{IL} (2) high- κ gate dielectric thickness - $t_{high-\kappa}$ (3) Overall Equivalent Oxide Thickness (EOT) (4) Gate Electrode/High- κ interface (5) κ -value of the high- κ oxide layer, and (6) Width -W and Length -L of the device.

The impact of scaling the gate channel length (L), the high- κ dielectric thickness ($t_{high-\kappa}$) and the interfacial layer (SiO₂) oxide thickness - t_{IL} on the low-frequency (1/f) noise in n- and p-MOSFET devices keeping the other factors constant, are studied here in more detail. Hafnium silicate (HfSiON) as high- κ oxide layer and metal (TiN/TaN) as gate electrode are used for this purpose.

II. EXPERIMENTAL

Noise results are reported for both n- and p-channel devices and all the wafers received a chemical oxidation based on

ozone chemistry. The interfacial layer thickness was either ~0.4 nm or ~0.8 nm of SiO₂. The high-κ gate oxides of various thickness were deposited by a Metal-Organic Chemical Vapor Deposition (MOCVD) process.

N- and p-channel transistors with a W = 10 μm mask width and a L = 1 μm mask length have been measured in linear operation for a drain voltage of |V_{ds}| = 0.05 V, though the electrical and effective channel lengths and width are lower. The gate voltage was varied typically between 1 and 2 V, in steps of 50 mV. To study the L dependence, the channel mask lengths were varied from L = 1 μm to 0.1 μm.

On-wafer noise measurements were performed under the control of BTA9812 pre-amplifier with noise analyzer and with HP35665A spectrum analyzer as hardware and NoisePro from Cadence as software.

III. THEORY

A. Length dependence of 1/f noise:

The noise parameter dependences for n- and p-MOSFETs in the linear region have been studied in detail by Vandamme *et al.* [7] and are summarized in Table 1.

Table 1 shows the dependence of various parameters viz. gate length (L), width (W), oxide thickness (t_{ox}), gate voltage overdrive (V_{gs} - V_t) on the noise parameters namely normalized drain current noise spectra (S_{id}/I_d²), drain current noise (S_{id}) and input-referred noise (S_{vg}). These dependences vary based on the involved noise mechanism - ΔN number fluctuations theory [8] when the channel carriers are the origin of noise, and the Δμ mobility theory [9] claiming that scattering effects as the source of noise. In reality, it is often observed that a correlated function of these two noise mechanisms – correlated mobility-number fluctuation (ΔN-Δμ) theory exists in most devices.

These expressions are also applicable for devices with high-κ dielectric oxides, except that CET values would be more appropriate than C_{ox} values.

	ΔN α ~ t _{ox} /[V _{gs} - V _t]	Δμ α = constant
S _{id} /I _d ²	[t _{ox}] ² [V _{gs} - V _t] ² [1/WL]	[t _{ox}] [V _{gs} - V _t] [1/WL]
S _{id,sat}	[V _{gs} -V _t] ² [W/L ³]	[V _{gs} -V _t] ³ [1/t _{ox}] [W/L ³]
S _{vg}	[t _{ox}] ² [1/WL]	[t _{ox}] ² [V _{gs} -V _t] [1/WL]

Table. 1. The dependence of various noise parameters on gate length, oxide thickness and gate voltage overdrive. Different dependences exist for number and mobility fluctuation theory, after [7].

It should also be noted that scaling the gate length not only increases the normalized noise magnitude but also gives rise to two other phenomena. One is that it enhances the device-to-device spread among the devices [10] and second is that the noise spectrum changes its character from 1/f-like into a

Lorentzian (1/f²) one [11], typical for a Generation-Recombination (GR) type of spectrum.

B. Oxide thickness dependence of 1/f noise:

The expected proportionalities of 1/f noise on oxide thickness depend on the noise mechanism that the devices support.

It has been shown earlier that n-MOSFETs support the theory on number fluctuations, while p-MOSFETs support mobility fluctuations [12]. It has also been reported that in dealing with silicon dioxide thickness scaling, a number of phenomena occur in parallel other than the noise magnitude increase, in particular for n-MOSFETs. The first one is the gate voltage dependence of the LF noise. For thicker oxides [13] the input-referred noise is independent on the gate voltage, while it becomes quadratically dependent on the gate voltage for thinner oxides.

The proximity of the gate electrode is another important factor, which can induce a so-called 1/f^{1.7} noise [14]. This additional component has been ascribed to the existence of a different trap profile near the gate electrode.

IV. RESULTS

A. Drain current spectral density

1) Length dependence of 1/f noise characteristics

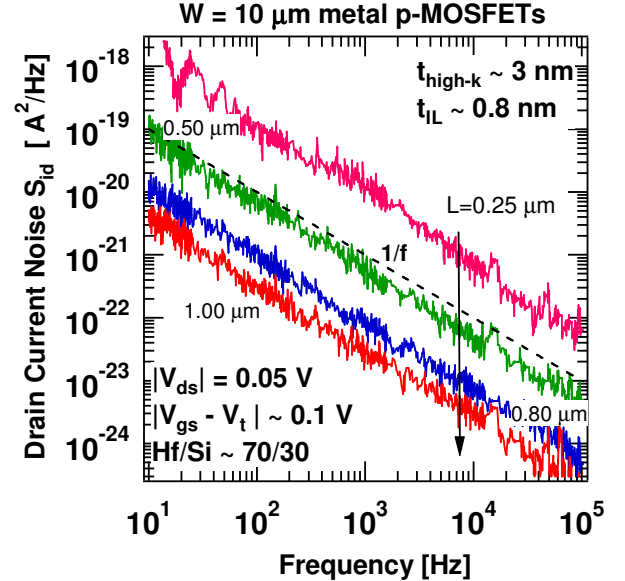


Fig. 2. Drain current spectral density S_{id} versus Frequency f for p-channel Hf-silicate devices with a high-κ thickness of 3 nm. The interfacial layer thickness was 0.8 nm for all the devices studied.

Fig. 2 shows the drain current spectra S_{id} for W=10 μm metal gate p-MOSFETs with a 3 nm high-κ dielectric as function of the channel length for |V_{gs}-V_t| ~ 0.1 V and |V_{ds}| = 50 mV. The L values compared here are 1.0, 0.8, 0.5 and 0.25 μm. Clearly, the spectra look 1/f^γ like for all the cases, with a frequency exponent γ between 0.9 ~ 1.05. It is seen that the 1/f noise decreases as the channel length increases. The increase

in S_{id} values is not linear as shorter channel lengths have comparatively a higher increase in noise. This non-linear increase in noise is mainly due to short channel effects, where these effects play a very significant role at lower mask lengths.

The effect of width- W also has a significant impact on the $1/f$ noise, where a similar behavior can be expected for p-MOSFET devices.

2) High- κ oxide thickness dependence of the $1/f$ noise characteristics

Figure 3 shows the drain current spectra S_{id} for a high- κ layer thickness of 1, 2 and 3 nm respectively. The high- κ layer is a 70% Hf-silicate gate dielectric. The interfacial layer is ~ 0.8 nm for all the cases. The increase in $1/f$ noise with decrease in high- κ dielectric layer thickness is found to be marginal as the variations in CET due to studied high- κ layers are negligible.

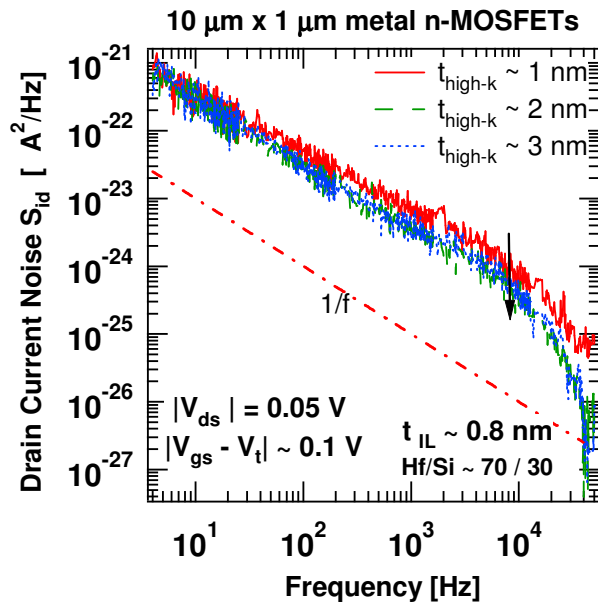


Fig. 3. Drain current spectral density S_{id} versus Frequency f for n-channel devices with various high- κ layer thicknesses. The interfacial layer (IL) oxide is SiO_2 and has a thickness of ~ 0.8 nm.

B. Normalized noise spectral density and gate voltage dependence

1) Gate length dependence of $1/f$ noise in high- κ dielectrics

The gate length and the oxide thickness dependences are also studied for normalized noise S_{id} / I_d^2 values. Figure 4 shows the normalized noise spectral density S_{id} / I_d^2 Vs gate voltage overdrive $|V_{gs} - V_t|$ for the studied channel lengths in p-MOSFETs with 70% Hf-silicates. Clearly, the normalized noise decreases with increase in channel length. On accurate terms, the comparison needs to be performed for effective channel lengths ($L - \Delta L$) [second order effects], but for first

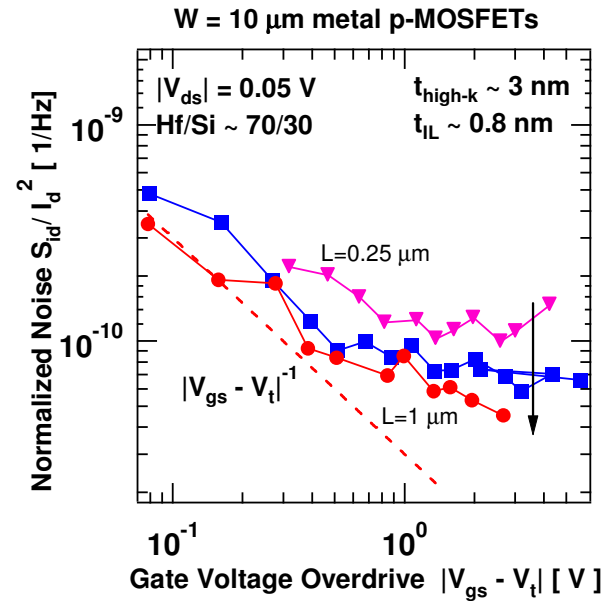


Fig. 4. Normalized noise spectral density S_{id} versus gate voltage overdrive ($V_{gs} - V_t$) for p-channel devices with various channel length L .

order approximation, they are not considered in this discussion. The curves run almost parallel to each other, indicating a similar decrease for the whole gate voltage overdrive range.

One can expect a similar trend for n-MOSFETs devices also.

2) High- κ oxide thickness dependence of the $1/f$ noise characteristics

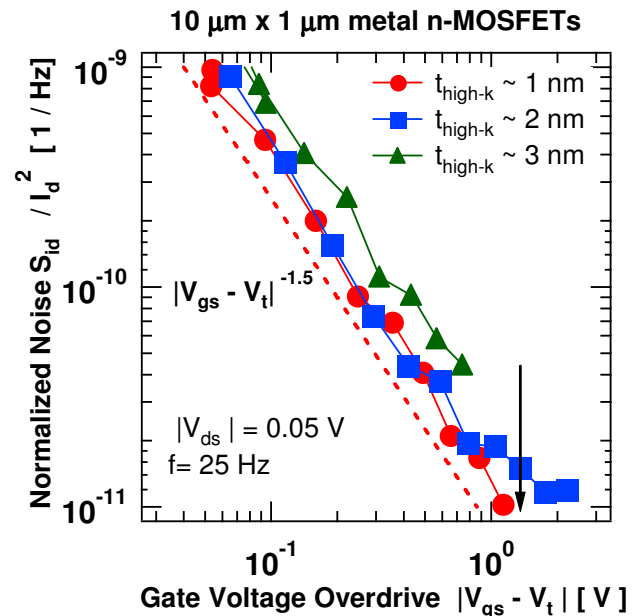


Fig. 5. Normalized noise spectral density S_{id} versus gate voltage overdrive ($V_{gs} - V_t$) for n-channel devices with various high- κ layer thicknesses. The interfacial layer (IL) oxide is SiO_2 and has a thickness of ~ 0.8 nm.

Figure 5 shows the normalized noise spectral density S_{id}/I_d^2 for various gate voltage overdrives ($V_{gs} - V_t$) for metal n-

MOSFETs. From Table 1, it can be inferred that the normalized noise should be either proportional to $|V_{gs}-V_t|^2$ if number fluctuations is the dominant mechanism, or $|V_{gs}-V_t|$ if mobility fluctuations exist. But, clearly in this case, it is seen that the normalized noise is proportional to a factor of 1.5, which is in between these two values. This shows that the dominant mechanism may be closely related to the correlated number and mobility fluctuations ($\Delta N-\Delta\mu$) theory. The normalized noise values increase as the high- κ dielectric thickness reduces for all studied gate voltage overdrives, but this variation is only found to be marginal and does not exactly support the theory. A similar behavior was found in p-MOSFETs.

V. DISCUSSION

A. Gate length dependence of the $1/f$ noise for high- κ gate oxides

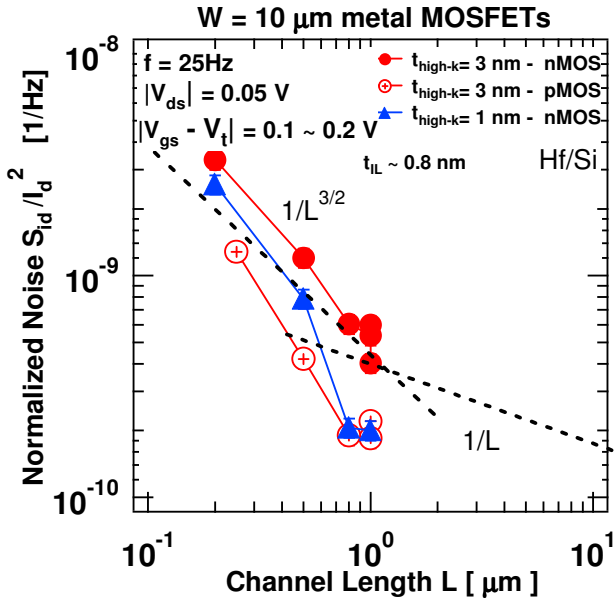


Fig. 6. Normalized drain current spectral density S_{id}/I_d^2 versus channel length L for n- and p-MOSFETs with different Hafnium silicate thicknesses.

The input-referred noise for all n- and p-MOSFETs were estimated based on the formula $S_{vg} = S_{id}/g_m^2$, where g_m is the transconductance of the device. Figures 6 and 7 shows the normalized noise values and input referred noise as a function of channel length L for both n- and p-MOSFETs for different $t_{high-\kappa}$ thickness, with the same 0.8 nm interfacial layer.

The data for n- and p-MOSFETs clearly shows a deviation from $1/L$ for both S_{vg} and S_{id}/I_d^2 values, where a stronger dependence on the channel length is observed ($1/L^{3/2}$) at lower L values. Since the measurements and the analyses are limited to the linear region, we expect a reduced series resistance in all these devices and therefore the noise due to series resistance is neglected in this analysis. In addition, it should be remarked that instead of the mask length the effective channel length should be used.

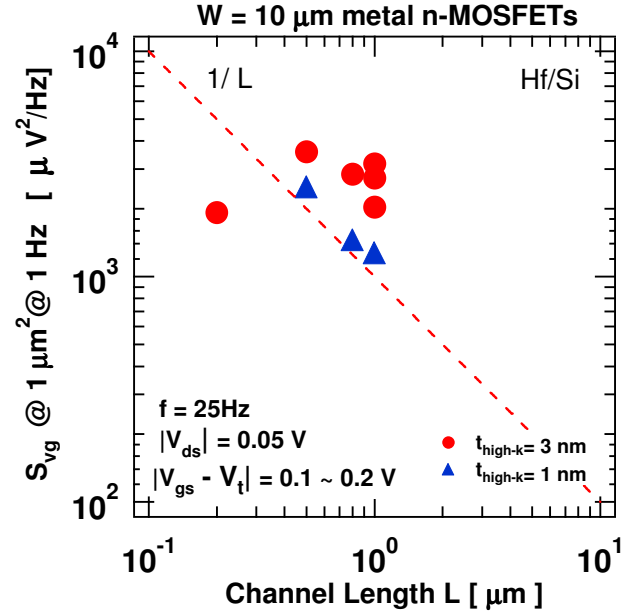


Fig. 7. Normalized drain current spectral density S_{id}/I_d^2 versus channel length L for n- and p-MOSFETs with different Hafnium silicate thicknesses.

Such a deviation from a $1/L$ behavior for lower L was also observed in SiO_2 based devices and was earlier reported by the group of Celik-Butler *et al.* [15],[16]. They proposed a modified $1/f$ noise model to explain the SiO_2 based devices, whereby a non-uniform distribution of the threshold voltage was used. Due to non-uniformity in the surface band-bending conditions, it is possible that the conduction channel has two distinct regions with different threshold voltages. This factor was taken into account in their modified $1/f$ noise model.

Compared to a SiO_2 layer, also other observations apart from the above ones are noticed. First of all, no G-R spectrum is seen at shorter channel lengths, where at $L=0.25 \mu\text{m}$ the S_{id} spectra are $1/f$ like, though the device-to-device spread may be considerable.

These additional factors may explain the deviation observed at shorter channel lengths.

B. High- κ oxide thickness dependence of the $1/f$ noise characteristics

Figures 8 and 9 show the normalized noise values S_{id}/I_d^2 and the input referred noise S_{vg} as a function of the high- κ dielectric layer thickness $t_{high-\kappa}$ for n- and p-MOSFETs at $|V_{ds}| \sim 0.05\text{V}$ and $|V_{gs}-V_t| \sim 0.1\text{V}$, with the same 0.8 nm interfacial layer. The noise values are seen to be lower for p- than for n-MOSFETs, which confirms our earlier observations [17].

Also from Fig 9, it can be seen that the values are higher by more than a decade compared to the ITRS requirement of $200 \mu\text{V}^2/\text{Hz}$, shown by the dotted line. From earlier observations, it has been quite established that n-MOSFETs follow correlated number fluctuations while p-MOSFETs follow the theory on mobility fluctuations. Hence for n-MOSFETs, the values of normalized noise S_{id}/I_d^2 and the input referred noise S_{vg} should be squarely proportional to $t_{high-\kappa}$, while for p-MOSFETs, S_{vg}

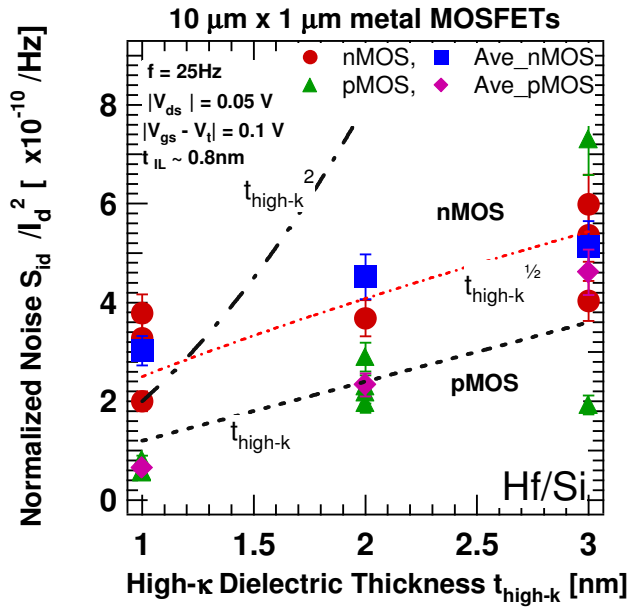


Fig. 8. Normalized drain current spectral density S_{id}/I_d^2 versus Hafnium silicate thickness for n- and p-channel devices.

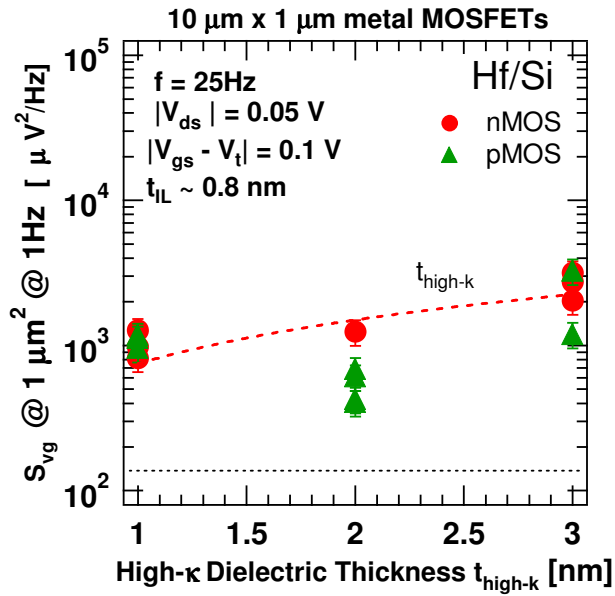


Fig. 9. Normalized S_{vg} values versus Hafnium silicate layer thickness for n- and p-channel devices.

should vary linearly with the high- κ oxide thickness t_{high-k} , according to Table 1.

In our case, for p-MOSFETs, the t_{high-k} dependence of S_{id}/I_d^2 and S_{vg} are clearly visible and seem to follow the theory. But deviations are noticed for n-MOSFETs, where the dependency changes and is found to be between and $t_{high-k}^{1/2}$ and t_{high-k} .

Though it is not possible to isolate the contribution of the interfacial layer t_{IL} on the $1/f$ noise in the studied devices, it is worthwhile to give some considerations on this effect. Simoen *et al.* [18] have investigated the effect of the interfacial layer on $1/f$ noise, and reported a strong dependence on the interfacial layer thickness.

Figure 10 shows the input referred noise values S_{vg} for a gate voltage overdrive $|V_{gs} - V_t| \sim 0.1V$ and $|V_{ds}| \sim 0.05 V$. It is

seen that the devices with the lowest interfacial layer thickness t_{IL} (and in-turn higher EOT), show the highest $1/f$ noise, while a highest IL thickness results in a lower $1/f$ noise. When HfO_2 is used as a high- κ dielectric, the noise values increase almost by an order of magnitude when the 0.8 nm interfacial oxide is replaced by an 0.4 nm oxide layer.

In a similar experiment conducted by Kojima *et al.* [19], a strong EOT dependence was observed and they attribute the increase in $1/f$ noise to both the interfacial layer oxide and the high- κ layer of varying thicknesses. They observed a higher increase in S_{vg} values for an increase in high- κ layer thickness than for an increase in the interfacial layer thickness. Min *et al.* [20] have reported similar observations on interfacial layer dependences in other Hf-based gate stacks.

Though this factor needs to be taken into account for high- κ devices too, it is equally important that the factors related to additional trapping in high- κ oxide layers are also considered. The relaxation-induced noise (RIN), which is strongly related to transient charge trapping in the high- κ layer, is an additional factor. Horikawa *et al.* [21] have shown that in-addition to the high- κ layers supporting the theory on number fluctuations; the contribution of RIN is also present.

Another observation is the proximity effect of the gate-dielectric interface on the $1/f$ noise. It has been reported that the gate-dielectric interface has an additional impact on the $1/f$ performance of the devices [22]. Though the effect is much more pronounced for a poly/high- κ interfacial layer, we have in our metal/high- κ not observed $1/f^{1.7}$ noise due to this proximity effect.

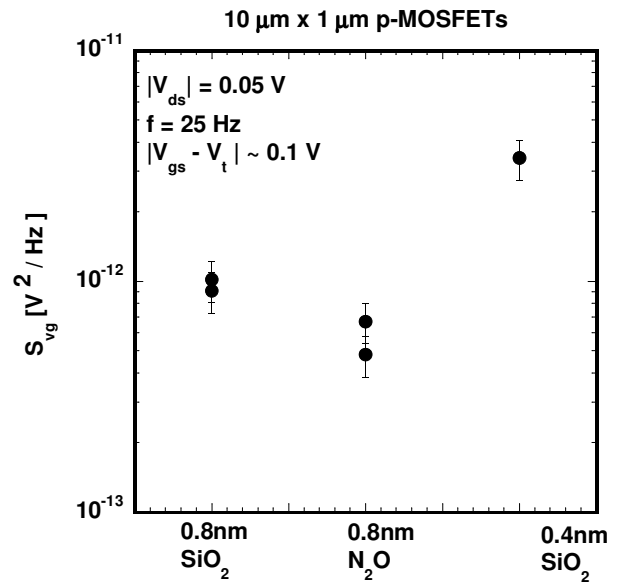


Fig. 10. Input referred noise S_{vg} Vs Different SiO_2 interfacial layer thicknesses for p-MOSFET.

Recently, it has been observed that $1/f$ noise is a strong function of temperature than expected and the existing models do not adequately explain this behavior. In the study made by Kojima *et al.* [19], they were unable to fit their data to the standard noise model based on number and mobility fluctuations and [23]. An anomalous behavior is observed,

whereby the input-referred noise lowers as the temperature increases. For SiO₂ dielectrics, Lee *et al.* [24] proposed a model including thermal activation energies of the traps in the dielectric. However, before adapting this model for high- κ layers one needs to carefully look into the origin of the higher 1/f noise observed for a high- κ dielectric.

VI. CONCLUSION

In conclusion, the need for high- κ based gate stacks has an impact on the low-frequency (1/f) noise behavior. For practical analog applications, this is a very important factor that needs to be taken into account, as both the n- and p-devices exceed the ITRS specs by about an order of magnitude. The gate length and the oxide thickness dependences of 1/f noise were investigated. For both n- and p-MOSFETs, a stronger gate length dependence of the noise was observed for lower L values. While high- κ p-MOSFETs more or less follow the classical theory for the thickness dependence of the 1/f noise, deviations are observed for n-MOSFETs. In addition, other differences related to the interfacial layer, the gate-dielectric interfacial layer and the temperature dependence were observed, though not discussed in detail. There are no existing 1/f noise models enabling to fully explain these effects. The observed differences in 1/f noise behavior in high- κ based gate stacks with respect to SiO₂ should be taken into account for a better and accurate modeling of these devices in future.

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