CMP-based Gate-Last High-K Integration

Ralf Endres, *Student Member IEEE*, Frank Wessely, *Student Member IEEE* and Udo Schwalke, *Member, IEEE*

***Abstract*— This paper presents the first successful attempt to integrate crystalline high-K gate dielectrics into a virtually damage-free damascene metal gate process by means of front-end chemical mechanical planarization. Process details as well as initial electrical characterization results on fully functional gate Gd_2O_3 dielectric MOSFETs with equivalent oxide thickness (EOT) down to 1nm are discussed.**

***Index Terms*— chemical mechanical planarization, CMP, damascene metal gate technology, e-beam lithography, high-K gate dielectrics, metal gate MOSFET, process integration**

I. Introduction

Ever increasing gate leakages through ultra-scaled SiO_2 gate dielectrics have led to extensive investigation of alternative materials with higher dielectric permittivity (high-K) in order to extend the unprecedented growth of IC complexity of the last four decades into the future.

Recently, very promising properties of epitaxially grown, crystalline rare-earth metal-oxides have been reported [1] and the integration of Pr_2O_3 dielectric in a conventional polysilicon CMOS process was successfully demonstrated [2]. However, high temperature annealing [3] and aggressive reactive ion etching (RIE) was found to degrade the initial quality of the sensitive high-K gate stack [2]. In order to minimize process induced oxide damage (PIOD), we have integrated crystalline and amorphous high-K dielectrics into a virtually damage-free replacement gate process [4, 5]. For the first time, fully functional metal gate MOSFETs with crystalline Gd_2O_3 and amorphous HfO_2 dielectric have been fabricated by means of front-end chemical mechanical planarization (CMP) in a “gentle” damascene metal gate technology.

II. Device Fabrication

The basic process concept of the damascene metal gate technology is shown in Fig. 1. Processing is performed on 4 inch p-type Si (100) wafers. Initially, dummy gate stacks are formed by consecutive deposition of silicon nitride and polysilicon, lithography and reactive ion etching (RIE) (Fig. 2a), followed by self-aligned S/D ion implantation. Next, the CVD alignment-oxide is deposited and RTA anneals at 1000°C are performed to activate S/D implants.

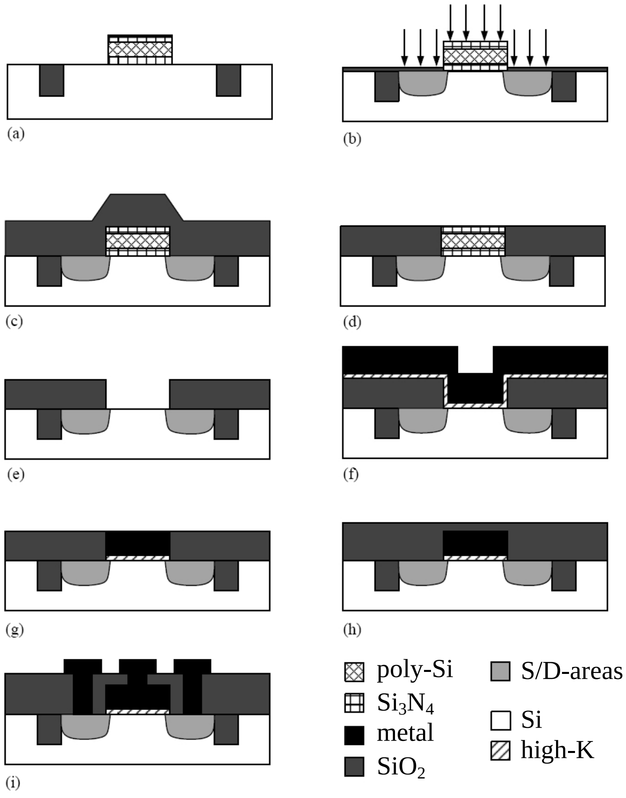

Fig. 1. Basic concept of the damascene metal gate process: A so-called ‘‘dummy gate’’ acts as a placeholder for the final gate stack. After having performed all aggressive process steps as RIE and high temperature anneals (a, b), the position of the dummy gate must be fixed for the later process steps (c, d) and the dummy gate can be removed by leaving a self-aligned imprint of the gate stack in the oxide (e) Subsequently, the high-K gate dielectric and metal gate are deposited (f), followed by a second CMP step (g) and standard back-end-processing (h, i).
The initial materials quality of the crystalline high-K gate dielectric is largely preserved by damascene metal gate processing.

The oxide is planarized by CMP down to the gate level using a atomic force microscope-based ex-situ endpoint detection. The dummy gates are removed completely by wet chemical etching, leaving a self-aligned imprint of the gate stack on the oxide layer (Fig.2b).

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Ralf Endres, Frank Wessely and Udo Schwalke are with the Institute for Semiconductor Technology and Nanoelectronics, Darmstadt University of Technology, Schlossgartenstraße 8, D-64289 Darmstadt, Germany (corresponding author to provide phone: +49 6151 16-3933; fax: +49 6151 16-5233; e-mail: endres@iht.tu-darmstadt.de)

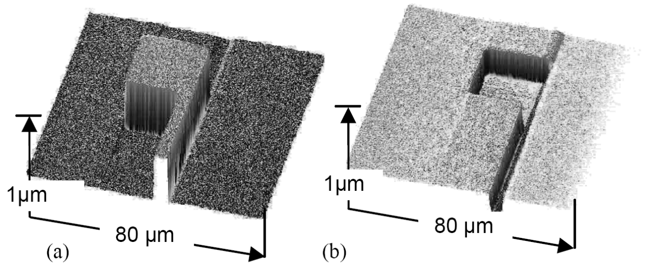


Figure 2. Atomic force microscopy (AFM) image of a dummy gate structure (a) and a self-aligned imprint of the gate stack in the alignment oxide (b).

Subsequently, the high-K gate dielectric is grown by molecular beam epitaxy (crystalline Gd_2O_3 layers of 5.3 nm and 13.5 nm physical thickness with smooth surface topography and good leakage currents as evident from AFM and Conductive-AFM measurements (Fig. 3)) or evaporated (HfO_2 layers with 3.0 nm physical thickness and 0.8 nm SiO_2 interfacial layer) . In addition, wafers with conventional SiO_2 are fabricated as a reference. Tungsten is deposited on top of the gate dielectrics and CMP is used to pattern the damascene metal gates. Standard back-end processing completes the fabrication.

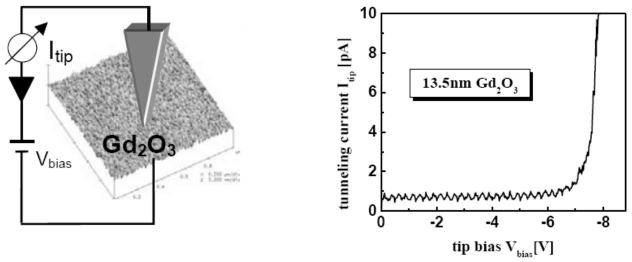


Fig 3. Atomic force microscopy (AFM) image of the Gd_2O_3 surface (left) and nanoscale I-V sweep by conductive atomic force microscopy (C-AFM) measurement (right).

III. RESULTS AND DISCUSSION

Both fabricated long channel devices (L > 4µm) with Gd_2O_3/ HfO_2 gate dielectric and tungsten gate electrode are fully functional. CV measurements on Gd_2O_3 capacitors give a dielectric constant of 10.4, corresponding to EOTs of 1.9 nm and 5.1 nm respectively. Leakages are below $1{\cdot}10^{-3}$ A/cm^2 for the 5.1 nm (Fig. 4), consistent with leakage requirements set by the ITRS [6)].

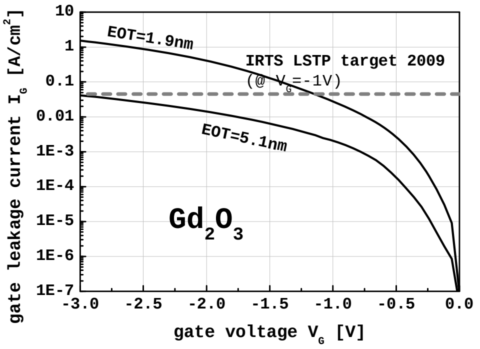


Fig 4. Gate leakage currents of 1.9 nm and 5.1 nm metal gate Gd_2O_3 pMOS capacitors (gate injection, substrate in accumulation).

The Gd_2O_3 gate dielectric nMOSFETs show proper transistor behavior (Fig. 5 and 6).

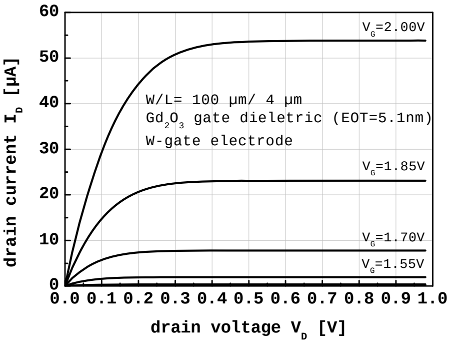


Fig 5. Output characteristics of a metal gate Gd_2O_3 nMOSFET.

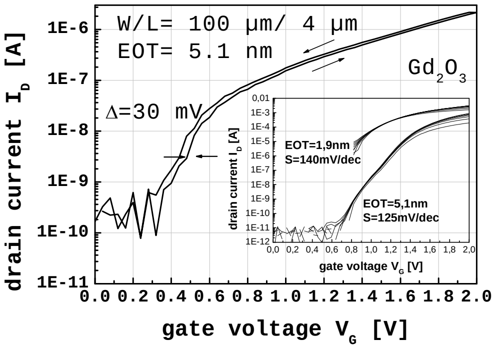


Fig. 6. Subthreshold characteristics of a Gd_2O_3 nMOSFET.

Note that extremely low hysteresis of less than 30 mV is observed in the subVt characteristics (Fig. 6), which is a substantial improvement when compared to conventionally integrated high-K oxides [7]. In the case of process-damaged high-K oxides, large hysteresis effects with Vt-shifts of more than 300 mV have been observed which could be related to a large susceptibility to build-up charge trapping sites [7]. The subVt swing of approximately 130 mV/dec indicates high interface state densities. Charge pumping (CP) measurements revealed trap densities of $2.3{\cdot}10^{12}$ eV^{-1}cm^{-2}, consistent with the degraded subVt swing. However, only slightly reduced values of $1.8 \cdot 10^{12}$ $eV^{-1}cm^{-2}$ are obtained for the SiO_2 reference devices which puts in question the effectiveness of the forming gas anneal when using tungsten gates. Energy resolved CP measurements on Gd_2O_3 nMOS devices showed that most of the interface traps are located in the upper half of the band gap (Fig. 7).

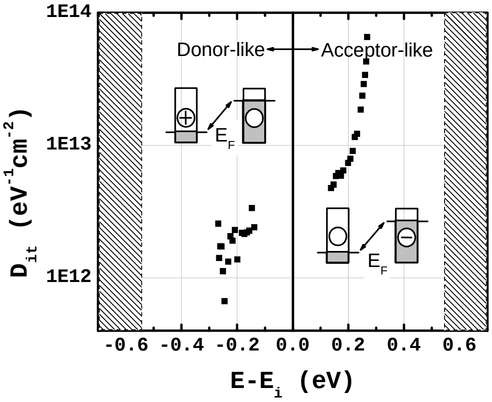


Fig. 7. Energy resolved CP measurements on Gd_2O_3 nMOS devices (EOT=5.1 nm).

Effective mobilities of 130 cm^2/Vs have been measured for the Gd_2O_3 MOSFETs as shown in Fig. 8.

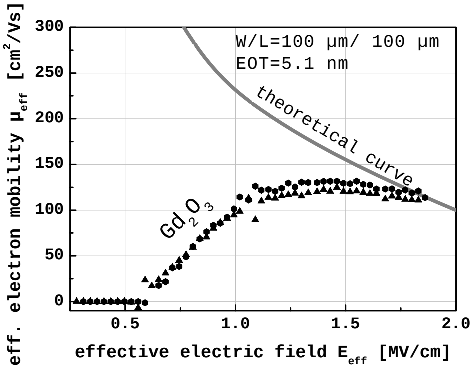


Fig. 8. Measured effective electron mobilities of damascene metal gate Gd_2O_3 nMOSFETs (EOT=5.1 nm).

Compared to SiO_2 references this corresponds to a reduction of approx. 40% at the same effective electric field. We suspect that the acceptor-type interface states significantly degrade mobility due to Coulomb-scattering.

Even the HfO_2 gate dielectric nMOSFETs show proper transistor behavior (Fig. 9).

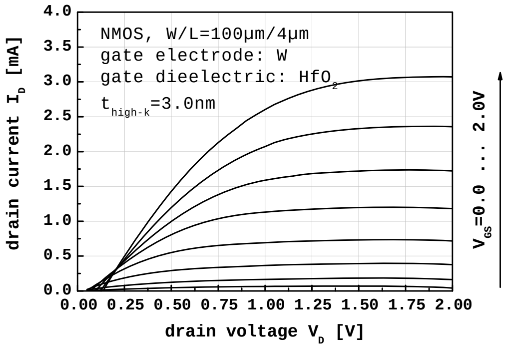
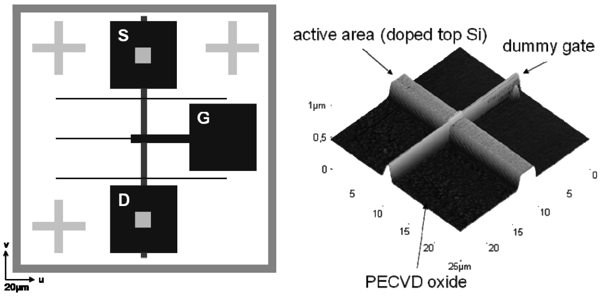


Fig 9. Output characteristics of a metal gate HfO_2 nMOSFET.

The electrical characterization of the devices is not completed yet.

IV. OUTLOOK

Current work includes scaling down the damascene metal gate process to the 100nm regime. We have successfully structured dummy gates on SOI-substrates by means of e-beam lithography (Fig. 10) and we expect functional devices with high-K metal gate stack soon.



(a) (b)

Fig. 10. Layout of an e-beam damascene metal gate MOSFET (a) and atomic force microscope image of a dummy gate structure produced with electron beam lithography (b).

V. CONCLUSION

We have successfully integrated crystalline Gd_2O_3 and amorphous HfO_2 in a damascene metal gate process by means of chemical mechanical planarization. Since the harsh processing is done prior to high-K deposition, PIOD-effects are minimized and the initial material quality of the crystalline high-K gate dielectric is largely preserved, so that the progress in high-K material engineering can be monitored directly at the device level.

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AUTHORS

Ralf Endres received his diploma degree in electrical engineering from Darmstadt University of Technology in 2005 and is currently doing his Ph.D. study at the Institute for Semiconductor Technology, Darmstadt, Germany. His research interests include new materials in CMOS technology as alternative high-K gate dielectrics and metal gates with focus on their gentle process integration and electrical characterization.

Frank Wessely received his diploma degree in electrical engineering from Darmstadt University of Technology in 2005. Currently, he is working towards the Ph.D. degree at the Institute for Semiconductor Technology and Nanoelectronics at the same University. His dissertation focuses on the integration and characterization of novel devices and integration concepts for the beyond-CMOS-era.

Udo Schwalke was awarded a Research Fellowship from the Alexander-von-Humboldt-Foundation for his Ph.D. thesis in 1984. During 1984 - 1986, he was appointed Caltech Research Fellow at the California Institute of Technology, USA. In 1987, he joined the Siemens AG, R&D Microelectronics in Munich, Germany. From 1990-1992 he was responsible for the 64Mb DRAM device design at IBM/Siemens, USA. Subsequently, at Infineon Technologies AG (the former Siemens Semiconductor Group) he worked on novel process architectures and device reliability issues. Since August 2001, Dr. Schwalke is Professor in Electrical Engineering and the Managing Director of the Institute for Semiconductor Technology at Darmstadt University of Technology. Prof. Schwalke has served as expert evaluator and reviewer for the European Commission and is a member of the IEE, IEEE and ECS. He has authored or co-authored more than 80 technical papers and holds several patents. Currently his research interests are focused on nanoscale CMOS technologies and molecular nanoelectronics.