Receiver Planning for a Multi-Standard Front-End

Maja Vidojkovic, Johan van der Tang, Peter Baltus* and Arthur van Roermund
Eindhoven University of Technology, Mixed-signal Microelectronics Group, EH 5.05
P.O.Box 513, 5600 MB, Eindhoven, The Netherlands
Phone: +31 (0)40 247 5131, Fax: +31 (0)40 245 5674
E-mail: m.vidojkovic@tue.nl
*Philips, Eindhoven, The Netherlands

Abstract — **One of the most recent and interesting challenges in the wireless communications area is the trend towards integration of multiple radio links. The integration of multiple radio links might be required either for different purposes (e.g. Bluetooth in a WLAN application) or for compatibility with different systems at various locations (e.g. different types of cellular phone networks in different countries). A multifunctional radio link is valuable only in case if it is less expensive and/or smaller than simply putting multiple radio components next to each other, while still having acceptable performance and a low power dissipation. One way to reduce the cost is to achieve a high level of integration and to eliminate the external components as much as possible. Another way to reduce the cost of the multiple function systems is to reuse building blocks among different radio links in order to limit chip area to a minimum. A number of critical issues at RF design level need to be solved when a flexible, multi-standard receiver is designed. These include: defining a common architecture, defining a multi-standard architecture and designing adjustable and configurable building blocks. The common architecture needs to support all the standards within the multi-standard receiver with acceptable cost, size and performance. The multi-standard, multi-band architecture has to be developed by using the common architecture and the configurable building blocks. In this paper a detail planning for a multi-standard receiver is presented. The GSM, Bluetooth and wireless LANs standards are considered to be main specifications that need to be covered for the multi-standard receiver section. Several options on the architectural level for a non-concurrent multi-standard receiver are investigated.**

Keywords— **RF front-end, multi-standard front-end, adjustability, configurability.**

I. INTRODUCTION

The number of systems that use radio links is increasing quickly. In parallel, the number of standards for such radio links is increasing quickly as well. For example Bluetooth and the ultra-wideband (UWB) standard support Wireless Personal Area Network (WPAN) applications Wireless Local Area Network (WLAN) systems are based on IEEE 802.11a, 802.11b, 802.11g standards. IEEE 802.16a, IEEE 802.16d and IEEE 802.16e standards support Wireless Metropolitan Area Network systems. Among the cellular standards (Wide Area Network) are GSM in 450 MHz, 480 MHz, 850 MHz, 900 MHz (in standard, extended and railway variations) bands, DCS 1800, PCS 1900, with or without GPRS and EDGE extensions, AMPS, IS-95, IS-98, IS-136, UMTS, PDC in high and low bands, CDMA2000 and TD-SCDMA. The mentioned standards are just a subset of the most popular and relatively recent standards.

Such a fast growth in wireless communications standards creates new challenges for the RF system and circuit designers. The most obvious challenge is the development of systems and components for each of these different standards in time and with limited resources. To complicate matters, many applications required multiple radio links, either for different purposes (e.g. Bluetooth in a cellular phone) or for compatibility with different systems at various locations (e.g. different types of cellular phone networks in different countries)-[1].

In this paper two multi-standard architectures are presented. Two approaches are combined to propose a solution to the previously addressed issue related to fast time-to-market and saving chip area in multi-standard architectures. One approach is to reduce the development effort and time of transceivers by reusing parts of previous transceiver development. The other approach is to reuse building blocks among different radio links.

The organization of this paper is as follows. In section 2, in line on the previously mentioned approaches, two multi-standard architectures are proposed. They are a front-end architecture without inductors in the LNA and a front-end architecture with a multi-band LNA. In section 3, the front-end specifications as a noise figure, a voltage gain, linearity (*IIP3* and *IIP2*) and selectivity are determined. In section 4, the distribution of the building block specifications is considered.

II. FRONT-END ARCHITECTURES

In this section two multi-standard architectures are proposed. They are a front-end architecture without inductors in the LNA and a front-end architecture with a multi-band LNA. Both architecture are based on a zero/low IF architecture. The zero-IF and low-IF architectures can be considered as identical if the I and Q paths in the low-IF architecture are combined in the digital section to perform the image suppression.

A. A front-end architecture without inductors in the LNA

A block diagram of the multi-standard front-end architecture without inductors in the LNA is proposed in fig. 1.

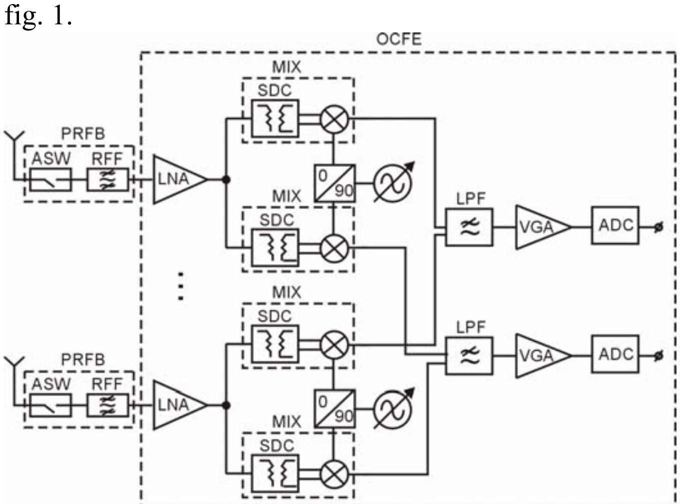

Figure 1: The multi-standard architecture without inductors in the LNA

The Passive RF Block (PRFB) for each standard consists of an antenna switch (ASW) and an RF filter (RFF). It is assumed that the insertion loss of the PRFB (L_{PRFB}) is 3 dB. The input impedance of the On-Chip Front-End (OCFE) is $Z_{in,OCFE}=Z_{LNA,in}$ =50 Ω.

The OCFE consists of separate LNA+mixer for each standard. It is assumed that the LNAs have the same configuration for each receive chain and this LNA is a wideband LNA without inductors. Hence, the chip area occupied by simply putting multiple LNA+MIX will not be too big. A signal-to-differential converter (SDC) converts a single-ended signal to differential signal. After the down conversion, a low pass filter (LPF) selects the wanted channel, and a variable gain amplifier (VGA) accommodates the level of the down-converted RF signals to fit a dynamic range of an analog-to-digital converter (ADC). It is assumed that the employed ADC is not adjustable.

A critical point for this architecture is the wide-band LNA. The LNA has to be a wideband topology that can receive a frequency range from 800 MHz up to 6 GHz, WLANa/b/g, Bluetooth and GSM/EDGE/GPRS, see fig. 3. There are not yet reported wideband LNAs without coils for such a huge frequency range. At high frequencies capacitance of transistors will deteriorate the performance of the circuit and it will decrease the range in which the LNA behaves as a wideband LNA.

B. A front-end architecture with a multi-band LNA

A block diagram of the multi-standard front-end architecture with a multi-band LNA is proposed in fig. 2.

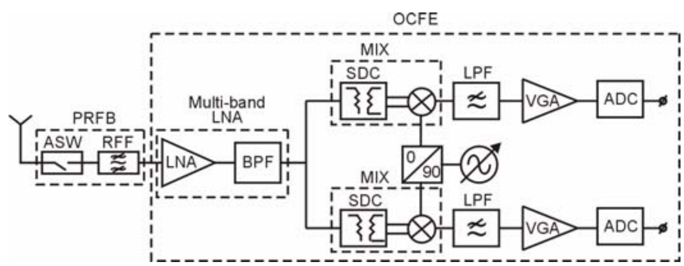

Figure 2: The multi-standard architecture with a multi-band LNA

The Passive RF Block (PRFB) consists of an antenna switch (ASW) and a RF filter (RFF). The RFF has to pass all of WLANa/b/g, Bluetooth and GSM/EDGE/GPRS, see fig. 3. It is assumed that the insertion loss of the PRFB (L_{PRFB}) is 3 dB. The input impedance of the On-Chip Front-End (OCFE) is 50 Ω.

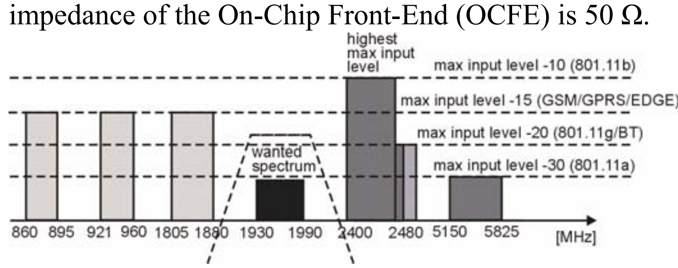

Figure 3: The main standards that has to be handled by the multi-standard architectures

The first block in the OCFE is a multi-band LNA. The signal at the input of the multi-band LNA is shown in fig. 3. At the output the multi-band LNA one of the frequency spectrums depicted in fig. 3 has to be selected. The selectivity is performed in a band pass filter (BPF).

The BPF is an LC tank at the output of the LNA. The capacitance of the LC tank should be adjustable such that the LNA can select one of the bands.

Two critical points are important to discuss for the proposed architecture. The first critical point is the selectivity at the output of the LNA. The bandwidth of an LC tank can be determined as:

$$BW = \frac{f_c}{Q} \tag{1}$$

where Q is the quality factor of the LC tank and f_c is the center frequency. The quality factor of the LC tank has to range from 23 to 65 in order to select a different spectrum at a different center frequency in the previously given frequency range.

The second critical point is that the proposed multi-standard architecture sets very strict linearity requirements. The cross-band 1-dB compression point will occur $20\log\left(\sqrt{2(n-1)}\right)$dB earlier than in-band 1-dB compression point. This suggests that, for the same amount of the nonlinearity, a multi-band system needs to be $20\log\left(\sqrt{2(n-1)}\right)$dB more linear than its single-band counterpart, [2]. n is the number of bands that are processed by the LNA. Therefore, considering 6 bands, see fig. 7, the system has to be 10 dB more linear than for the strongest interferer when compared to a single-band LNA.

C. Front-end architectures –conclusions

Two multi-standard architectures are considered. In the multi-standard architecture without inductors in the LNA, the LNA+mixer components are simply put next to each other. The reduced costs in this case arise from the fact that chip area is saved since LNAs without coils are used. The design time of the system is shorter since the same LNA is copied for more than one receiver path. However, it will be challenging to design a wideband LNA that can satisfied the requirements in a huge frequency range, especially at the high frequencies. Because of this problem this architecture seems to be most suitable for the GSM_GPRS_EDGE standards that operate below 2 GHz.

The multi-standard architecture with a multi-band LNA building block reuses this block among different radio links, in order to limit chip area to a minimum. Moreover this architecture has an LC tank at the output of the LNA, which is convenient to compensate the impact of transistor capacitances at the high frequencies. However, the linearity requirements are very high as the number of processed bands increasing. Is seems that this architecture is suitable solution for the WLANa/b/g and Bluetooth standards.

III. FRONT-END SPECIFICATIONS

In this section the procedure to derive the front-end specifications, such as a noise figure, a voltage gain, linearity (*IIP3* and *IIP2*) and the selectivity, is discussed.

A. Voltage gain

For the voltage gain there are two scenarios. The first scenario is when the input signal amplified by the voltage gain provided by the OCFE does not exceed the maximum full-scale voltage of the ADC.

The mapping of the signals that corresponds to the sensitivity level, the maximum input level and interfere into the ADC dynamic range is shown in fig. 4.

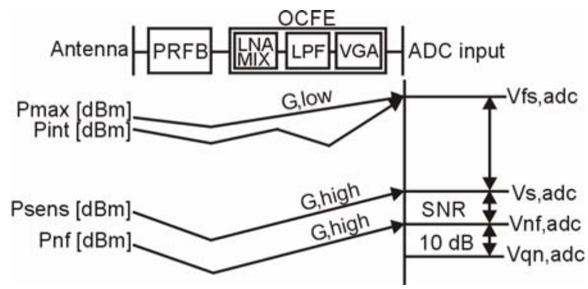

Figure 4: Mapping of the signal levels into the ADC dynamic range

P_{nf} is the noise floor, P_{sens} is the sensitivity level, P_{max} is the maximum input level and P_{int} is an interferer. $V_{fs,ADC}$ is a full-scale differential voltage of ADC, $V_{qn,ADC}$ is the quantization noise of ADC, $V_{s,ADC}$ is a voltage that corresponds to the sensitivity level at the input of ADC and $V_{nf,ADC}$ is a voltage that corresponds to the noise floor at the input of ADC.

The ADC should not be the dominant noise source. It is reported in the literature that the quantization noise of the ADC has to be 8 to 10 dB below the noise floor of the analog front-end. We assume that the quantization noise is 10 dB lower than the noise floor of the analog front-end. The dynamic range of the ADC can be expressed as:

$$DR_{ADC}[dB] = 20\log\left(\frac{V_{fs,ADC}}{V_{qn,ADC}}\right) \tag{2}$$

where DR_{ADC} is the dynamic range of the ADC. Based on (2) $V_{qn,ADC}$ can be calculated as:

$$V_{qn,ADC} = \frac{V_{fs,ADC}}{10^{DR_{ADC}/20}} \tag{3}$$

According to fig. 4 the following equation can be written:

$$V_{s,ADC}[dB] - V_{qn,ADC}[dB] = SNR + 10[dB] = 20\log\left(\frac{V_{s,ADC}}{V_{qn,ADC}}\right) \tag{4}$$

where *SNR* is the minimal signal-to-noise ratio that is necessary to provide at the input of the demodulator in order to provide required reception quality. Based on (4)

$V_{s,ADC}$ can be calculated. The overall voltage gain of the OCFE can be calculated as:

$$G_{OCFE} = 20\log\left(\frac{V_{s,ADC}}{V_{s,OCFE}}\right) \quad (5)$$

where $V_{s,OCFE}$ is a voltage that corresponds to the sensitivity level at the input of OCFE and it is equal to

$$V_{s,OCFE} = \sqrt{10^{((P_{sens} - L_{PRFB})/10)} \cdot Z_{in,OCFE} \cdot 1mW} \quad (6)$$

The second scenario is when the input signal amplified by the voltage gain provided by the OCFE (G_{OCFE}) exceeds the maximum full-scale voltage of the ADC. Such a strong wanted signal has to be amplified by a lower voltage gain. The required voltage gain for the maximum input signal can be calculated by:

$$G_{OCFE,low} = 20\log\left(\frac{V_{fs,ADC}}{V_{\max,OCFE}}\right) \quad (7)$$

where $V_{max,OCFE}$ is a voltage that correspond to the maximum input level at the input of the OCFE and it is equal to:

$$V_{\max,OCFE} = \sqrt{10^{((P_{\max} + L_{PRFB})/10)} \cdot Z_{in,OCFE} \cdot 1mW} \quad (8)$$

B. Noise figure

The overall noise figure (NF_o) of a front-end can be calculated by using equation (1).

$$NF_o = P_{sens} + 174dBm/Hz - SNR - 10\log B \quad (9)$$

B is the effective channel bandwidth. NF_o can be expressed as:

$$NF_O = NF_{PRFB} + NF_{OCFE} \quad (10)$$

NF_{PRFB} is the noise figure of the PRFB and it is equal to the insertion loss of PRFB (NF_{PRFB}=L_{PRFB}=3 dB). The noise floor can be expressed as:

$$P_{nf} = P_{sens} - SNR \quad (11)$$

C. Selectivity

The selectivity in the proposed front-end is determined by the filtering in the PRFB and in the OCFE. In the multi-band architecture with a multi-band LNA, the selectivity in the OCFE is determined by the BPF and the LPF. In the multi-band architecture without inductors in the LNA, the selectivity in the OCFE is determined by the LPF. In this section the filtering provided by the LPF is considered.

The filtering (the attenuation) provided by the LPF has to be enough in order to enable ADC to handle the down-converted RF signal with its dynamic range. When interferer P_{int} (V_{int}), see fig. 4, which is present in the adjacent channel, accompanies the wanted signal, then it will be amplified with the same gain as the wanted signal (G_{OCFE}). In this case, the interferer signal will exceed the full-scale voltage of the ADC. In order to prevent this, the LPF has to provide enough attenuation for the adjacent channel. The required attenuation can be calculated as:

$$A_{LPF} = 20\log\left(\frac{V_{\text{int},ADC}}{V_{fs,ADC}}\right) \quad (12)$$

$V_{int,ADC}$ is the level of the interferer at the input of the ADC without filtering. It can be calculated as:

$$V_{\text{int},ADC} = \sqrt{10^{((P_{\text{int}} + L_{PRFB} + G_{OCFE})/10)} \cdot Z_{in,OCFE} \cdot 1mW} \quad (13)$$

D. Linearity

The front-end specifications related to the linearity are expressed by *IIP3* and *IIP2.*

The overall *IIP3* of the front-end ($IIP3_o$) can be calculated by using (14):

$$P_{IIP3_o} = P_{\text{int}} + \frac{P_{\text{int}} - P_{im3}}{2} \quad (14)$$

The level of the IM3 components P_{im3} is equal to the noise floor of the wanted band. P_{int} is the interferer causing inter-modulation. The *IIP3* that corresponds to the OCFE can be calculated as:

$$P_{IIP3_{OCFE}} = P_{IIP3_o} + L_{PRFB} \quad (15)$$

The overall *IIP2* of the front-end ($IIP2_o$) can be calculated by using (16):

$$P_{IIP2_0} = 2P_{\text{int}} - P_{im2} \quad (16)$$

The level of the interferer is the same as in the case of *IIP3*. The level of IM2 components should be taken to be 10 dB below the noise floor.

The *IIP2* that corresponds to the OCFE can be calculated as:

$$P_{IIP2_{OCFE}} = P_{IIP2_o} + L_{PRFB} \quad (17)$$

IV. Distribution of Building Block Specifications

In this section we determine distribution of the voltage gain, *NF* and *IIP3* of each building block in the front-end. The distribution of the building block specifications is done by using the analytical expressions for overall voltage gain, *NF* and *IIP3* of the front-end.

A. Distribution of the voltage gain

The voltage gain of the OCFE for both multi-standard architectures can be expressed as:

$$G_{OCFE} = G_{LNA}\frac{Z_{MIX,in}}{Z_{MIX,in} + 2Z_{LNA,in}}G_{MIX}G_{LPF}G_{VGA} \quad (18)$$

where $G_{LNA} = G_{lna} \cdot G_{BPF}$, G_{MIX}, G_{LPF}, G_{VGA} are the voltage gain of the LNA, the MIX, the LPF and the VGA, respectively. It is assume that G_{BPF} = 1 (= 0dB) (G_{LNA} = G_{lna}). $Z_{MIX,in}$ is the input impedances of the MIX. $Z_{LNA,out}$ is the output impedances of the LNA. The input impedance of the LPF and the VGA are neglected because they are considered very high in the base-band. It is assumed that G_{LPF} = 1 (= 0dB). Since, in the multi-standard architecture with a multi-band LNA the LC tank is at the output of the LNA, $Z_{MIX,in}$ is much higher than $Z_{LNA,out}$. Hence, the expression for the voltage gain is simplified as:

$$G_{OCFE} = G_{LNA} G_{MIX} G_{LPF} G_{VGA} \tag{19}$$

B. Distribution of the noise figure

The noise figure of the OCFE (N_{OCFE}) for both architectures can be expressed as:

$$\begin{aligned} NF = 10\log[F_{LNA} + \\ &+ \frac{1}{2}\frac{F_{MIX}-2}{\left|\frac{Z_{LNA,in}}{Z_{LNA,in}+R_S}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{LNA}\right|^2} + \\ &+ \frac{1}{2}\frac{F_{LPF}-1}{\left|\frac{Z_{LNA,in}}{Z_{LNA,in}+R_S}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{LNA}\right|^2} + \\ &+ \frac{1}{2}\frac{F_{VGA}-1}{\left|\frac{Z_{LNA,in}}{Z_{LNA,in}+R_S}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{LNA}G_{MIX}\right|^2}] \end{aligned} \tag{20}$$

where F_{LNA} is the noise factor of the LNA. F_{MIX} is the single-side-band noise factor of the MIX. F_{LPF} and F_{VGA} are the noise factor of the LPF and VGA, respectively. Rs=50Ω is the source impedance that drives OCFE. Due to the impedance match at the LNA input, $Z_{LNA,in}$ = Rs =50 Ω. Factor ½ in (2) is consequence of the recombination of I and Q paths in the digital domain.

The *NF* of the LNA and MIX is calculated with respect to an impedance of 50Ω, while the *NF* of the LPF and VGA is calculated with respect to an impedance of 100Ω. The same assumption for $Z_{MIX,in}$ and $Z_{LNA,out}$ are valid, hence, similar simplification of the equation (2) can be done for the multi-standard architecture with the a multi-band LNA.

C. Distribution of IIP3

The *IIP3* of the OCFE for the architecture with a multi-band LNA can be expressed as:

$$\begin{aligned} \frac{1}{A_{IIP3}^2} &= \frac{1}{IIP3_{LNA}^2} + \frac{G_{LNA}^2}{IIP3_{BPF}^2} + \frac{G_{LNA}^2 G_{MIX}^2}{A_{BPF}^3\, IIP3_{LPF}^2} + \\ &+ \frac{G_{LNA}^2 G_{MIX}^2 A_{LPF}^3}{A_{BPF}^3\, IIP3_{VGA}^2} + \frac{G_{LNA}^2 G_{MIX}^2 A_{LPF}^3 G_{VGA}^2}{A_{BPF}^3\, IIP3_{ADC}^2} \end{aligned} \tag{21}$$

$IIP3_{LNA}$, $IIP3_{MIX}$, $IIP3_{LPF}$, $IIP3_{VGA}$ and $IIP3_{ADC}$ are signal levels that correspond to IIP3 of the LNA, mixer, LPF, VGA and ADC. A_{BPF} is the attenuation of the BPF (the LC tank) and A_{LPF} is the attenuation for adjacent channel provided by LPF.

The *IIP3* of the OCFE for the architecture without inductors in the LNA can be expressed as:

$$\begin{aligned} \frac{1}{A_{IIP3}^2} &= \frac{1}{IIP3_{LNA}^2} + \frac{\left|G_{LNA}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}\right|^2}{IIP3_{MIX}^2} + \\ &+ \frac{\left|G_{LNA}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{MIX}\right|^2}{IIP3_{LPF}^2} + \\ &+ \frac{\left|G_{LNA}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{MIX}\right|^2}{A_{LPF}^3\, IIP3_{VGA}^2} + \\ &+ \frac{\left|G_{LNA}\frac{Z_{MIX,in}}{Z_{MIX,in}+2Z_{LNA,in}}G_{MIX}G_{VGA}\right|^2}{A_{LPF}^3\, IIP3_{ADC}^2} \end{aligned} \tag{22}$$

V. CONCLUSIONS

In this paper two multi-standard architectures were introduced. They are multi-standard architecture without inductors in the LNA and the multi-standard architecture with the multi-band LNA. The multi-standard architecture without inductors in the LNA was proposed as a suitable solution for the GSM/GPRS/EDGE standards. The multi-standard architecture with the multi-band LNA building blocks was chosen as a suitable solution for the WLANa/b/g and Bluetooth standards. The complete receiver planning, calculations of the front end specifications and distribution of building block specification, for both architectures was presented.

REFERENCES

[1] M.Brandolini, "Toward Multistandard Mobile terminals-Fully Integrated Receivers Requirements and Architectures", IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 3, March 2005.

[2] H.Hashemi, et al., "Concurrent Multiband Low-Noise Amplifiers-Theory, Design, and Applications", IEEE Transaction on Microwave Theory and Techniques, vol. 50, no. 1, January 2002.