

# Charge Plasma Diode - A Novel Device Concept

B. Rajasekharan, R.J.E. Hueting, C. Salm, T. Hoang and J. Schmitz

**Abstract**— We propose a new device concept called charge plasma (CP) diode [1]. The diodes are with metal/silicided contacts of different workfunctions and thin intrinsic region in between. The workfunctions and layer thicknesses are chosen such that an electron plasma is formed on one side of the silicon body and a hole plasma on the other, i.e. a CP p-n diode is formed. The main advantages of these devices are low temperature budget and no dopant implantation is necessary in thin silicon layers [2,3,4]. We begin by discussing some important results from our silicon p-i-n diodes before moving on to the novel device concept of CP diodes.

**Index Terms**— diode, p-i-n diode, charge plasma (CP) diode, silicon-on-insulator (SOI), buried oxide (BOX), quantum confinement, band gap widening.

## I. INTRODUCTION

Silicon p-i-n devices have been investigated by many groups extensively for power applications and as light emitting devices [5]. In most of the applications the diodes are made using SOI wafers and a long intrinsic region is used which helps to provide unique properties like low and constant capacitance, high breakdown voltage in reverse bias and better controllability over device resistance [6]. For our studies we used p-i-n diodes with thin intrinsic region and uniform field to investigate avalanche behavior. For scaled down devices, the intrinsic region becomes thinner and less wide. This results in improvement of mobility, power consumption, etc [6]. However one misses to understand the importance of scaling other device parameters which would affect the overall behavior of the diode. One of the important parameter is the effect of the thick BOX layer and the gate beneath the substrate on device characteristics in forward and reverse mode. We try to investigate this effect and hint at possible solutions for the same. The other interesting effect is that of band gap widening in very thin silicon layers [7,8]. In this work we show that the breakdown voltage decreases with decrease in silicon layer thickness. However, we find that the

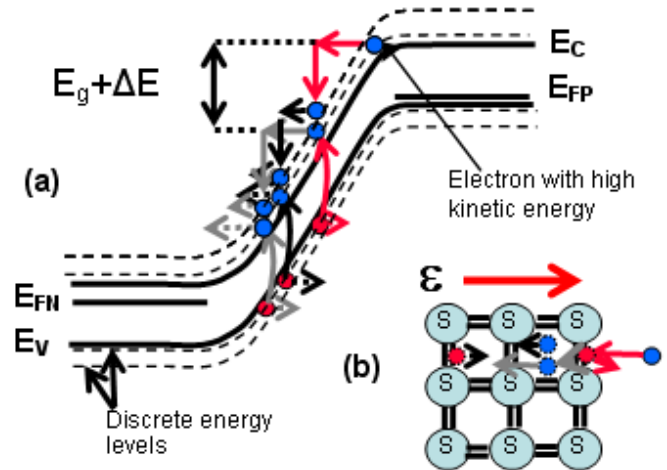


Fig. 1(a) shows the schematic band diagram of a 1D p-i-n diode at reverse breakdown. Due to structural quantum-confinement discrete energy levels rise which induce an effective bandgap widening effect ( $\Delta E$ ). Consequently, more energy and hence applied voltage is required to form the same amount of electron-hole pairs by impact ionization and avalanche. Fig. 1 (b) shows a simplified representation of the electron-hole pair generation. The parameters indicated in the figure are:  $E_g$  is the bandgap,  $E_c$  and  $E_v$  are the conduction resp. and valence band,  $E_{FP}$  and  $E_{FH}$  are the quasi-Fermi levels of holes and electrons respectively and  $\epsilon$  is the electric field.

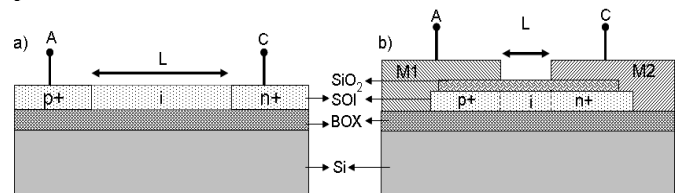


Fig. 2(a) shows the schematic of p-i-n device with doped anode and cathode regions on an SOI wafer. The anode “A” has p-type doping and cathode “C” has n-type doping. The intrinsic region in between is lowly doped p-type. Fig. 2(b) shows the schematic of our novel “charge plasma” (CP) diode. Metal M1 has a workfunction higher than silicon and metal M2 has a lower workfunction. This workfunction difference helps to induce p+ or n+ regions in the intrinsic silicon layer. The silicon dioxide layer on top of silicon is optional.

breakdown voltage begins to increase for layer thicknesses of around 10-nm. This we think is due to quantum confinement in very thin layers. The basic idea is that a decrease in thickness of the silicon layer causes an increase in separation of energy levels. This further increases the voltage at which electron-hole (e-h) pairs can be formed due to impact ionization in the allowed conduction states and hence an increase in breakdown of the intrinsic silicon region (fig. 1). We make use of two types of p-i-n diodes in order to study

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these interesting effects. Fig. 2a shows the schematic of p-i-n diode with doped anode and cathode regions and thinned down SOI region and fig. 2b shows p-i-n diode with metal/silicided contacts of different workfunctions and thin intrinsic region in between. The workfunctions and layer thicknesses are chosen such that an electron plasma is formed on one side of the silicon body and a hole plasma on the other, i.e. a CP p-n diode is formed. The metal gates are optionally isolated from the top of the body with a dielectric layer and each form a contact at both sides of the silicon body. The paper is divided into two parts. The first part discusses results obtained from p-i-n diodes with doped anode and cathode regions and thinned SOI region. In the second part we discuss results of our novel CP diode.

## II. P-I-N DIODE

### 2.1. Experimental

The fabrication of p-i-n diodes are carried out at our in house research lab. A field emission scanning electron microscope (LEO 1550 HRSEM) was used to characterize the obtained features in every step of the process. The detailed process flow for fabricating p-i-n diodes with doped source and drain contacts had been described elsewhere [9].

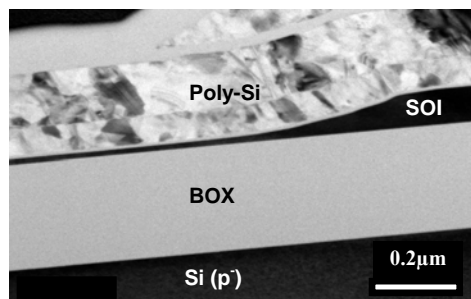


Fig. 3 shows TEM image of a p-i-n device on an SOI wafer.

### 2.2. Characterization and discussion

We began by investigating experimentally obtained p-i-n diodes with doped anode and cathode regions and intrinsic region thicknesses 150-nm, 27-nm and 19-nm. The intrinsic region has an area of 5x60 microns. The transmission electron microscopy (TEM) image of a p-i-n device of 27-nm-thick intrinsic region is shown in fig. 3. The layout of 150-nm device is the same except that there is no thinning in the intrinsic region. In the following lines we will discuss the close agreement observed between simulations and measurement data of these devices. In all the measurements the substrate is grounded. In the forward bias mode the anode/p<sup>+</sup> is biased from 0 to 2-V and cathode/n<sup>+</sup> is at 0-V. Fig. 4 shows the forward bias characteristics of diodes with different intrinsic region thicknesses. As expected the ratio of currents in the diffusion region (~0.7-V) is proportional to the ratio of thicknesses of the intrinsic regions and the slope of the I-V curve is around 110-mV/dec. Fig. 5 shows the reverse breakdown characteristics wherein the cathode/n<sup>+</sup> region is swept from 0 to 30-V and the anode/p<sup>+</sup> is at 0-V. It can be

seen that the breakdown voltage of the 150-nm thick device is around 30-V and this voltage decreases as the thickness of the intrinsic region decreases. It is expected however that the breakdown voltage for a 5-μm long intrinsic silicon region is around 100-V [10]. This can be explained as follows. The critical field at the breakdown ( $E_c$ ) in silicon is around  $2 \times 10^5$  V/cm. Since the electric field in a p-i-n diode is uniformly distributed the breakdown voltage (BV) equals  $E_c \cdot L$ . The breakdown voltages are lowered in our devices due to the fact that the vertical field across the buried oxide (BOX) becomes higher than the lateral field across the intrinsic region thereby causing the breakdown near the BOX – n<sup>+</sup>. Further, the breakdown voltage reduces with decrease in silicon layer thickness.

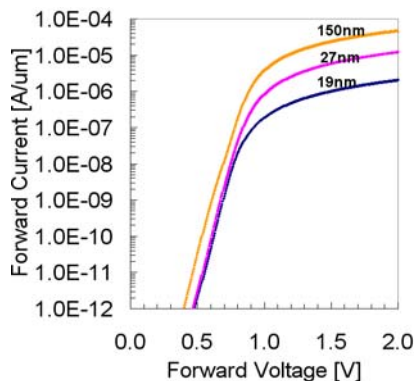


Fig. 4 shows the forward bias characteristics of p-i-n diodes for various silicon thicknesses.

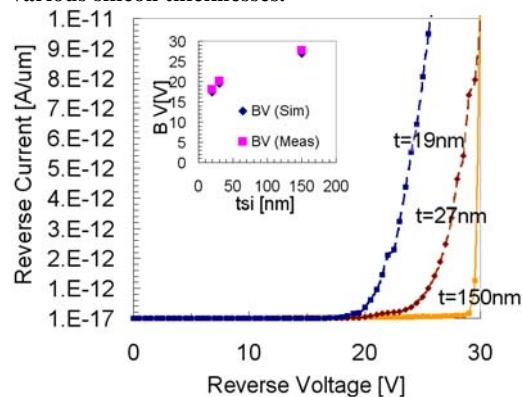


Fig. 5 shows the reverse bias characteristics of p-i-n diodes for various silicon thicknesses. The inset shows that the simulated breakdown voltages are in close agreement with measurements.

This can be understood by applying Gauss's law:

$$\text{div}E = \frac{\rho}{\epsilon_{si}}$$

On integrating over the length of the intrinsic region

$$E_{\text{max},x} = \int_0^L \frac{\rho dx}{\epsilon_{si}} \approx \frac{C_{si} V}{\epsilon_{si}} \quad \text{and,}$$

integrating over the depth,

$$E_{\text{max},y} = \int_0^\infty \frac{\rho dy}{\epsilon_{si}} \approx \frac{C_{ox} V}{\epsilon_{si}}$$

Hence, there is a trade-off between the capacitance from the BOX layer and that of the p-i-n diode.

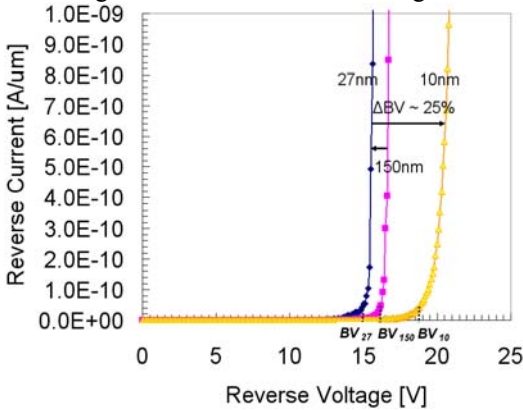
$$\frac{E_{\max,x}}{E_{\max,y}} \propto \frac{C_{Si}}{C_{ox}} \cdot \frac{A_{Si}}{A_{ox}} \propto \frac{t_{ox}}{L} \cdot t_{Si}$$

where,

- $E_{\max,x}$  = maximum field in lateral direction
- $E_{\max,y}$  = maximum field in vertical direction
- $C_{Si}$  = Capacitance of Silicon p-i-n diode per unit area
- $C_{ox}$  = Capacitance of BOX layer per unit area
- $\epsilon_{Si}, \epsilon_{ox}$  = permittivity of silicon and oxide
- $t_{ox}, t_{Si}$  = thickness of silicon and oxide layer
- $L$  = length of intrinsic silicon layer
- $A_{Si}$  = area of p-i-n diode
- $A_{ox}$  = effective area oxide capacitance

Hence the influence of the vertical field can be reduced only by increasing the BOX layer thickness or decreasing the length of the intrinsic region or probably by using silicon fin or nanowire structures with high aspect ratios.

Now, from our characterization experiments it is clear that in order to visualize quantum confinement or band gap widening effect it is imperative to move to smaller thicknesses of the intrinsic region. We fabricated and characterized gated p-i-n diodes with intrinsic region thicknesses of around 10-nm. It must be noted that our ultra-thin silicon devices ( $\leq 10$ -nm) were gated due to the processing techniques employed in achieving such thin intrinsic silicon regions.



**Fig. 6 shows the reverse bias characteristics of gated p-i-n diodes for various silicon thicknesses. The breakdown voltages (BV) are extrapolated to x-axis.**

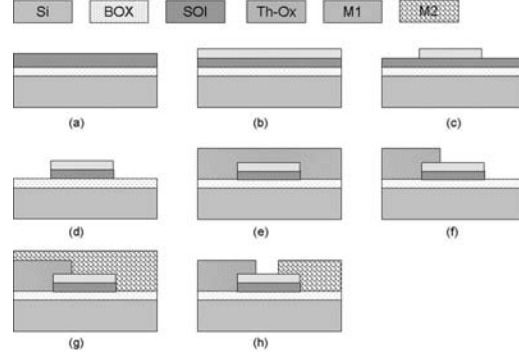
Fig 6 shows the reverse breakdown characteristics of these devices with the gate terminal biased at 0-V and biases to the anode and cathode applied as in previous experiments (fig. 5). From the characteristics we observe an increase in the breakdown voltage w.r.t. 10-nm devices and this voltage is found to be higher than in 150-nm p-i-n devices. This interesting behavior we assume could be due to quantum confinement induced band gap widening effect in thin silicon layers. The decrease in silicon layer thickness to 10-nm resulted in separation of energy bands and this in turn makes it difficult for an electron to jump to one of the allowed states. This means that very high energy is needed to knock out electrons from the lattice to form e-h pairs resulting in higher breakdown voltages (fig. 1). Quantum confinement had been

observed in intrinsic silicon layers of  $\leq 10$ -nm earlier [11]. However, to our knowledge this is the first time an observation of increase in breakdown voltage in ultra-thin silicon p-i-n diodes has been made. We hope to investigate this effect more thoroughly in our future studies. The same set of experiments performed using silicon p-i-n diodes with doped anode and cathode regions can be done with CP diodes.

### III. CHARGE PLASMA (CP) DIODE

#### 3.1 Experimental

The CP diode was briefly introduced in section 1 of this paper. The schematic of such a diode is as depicted in fig. 2b. The processing steps for the CP diode with metal anode and cathode contacts are presented in fig. 7.



**Fig. 7 shows the process flow to fabricate CP diodes. Metals M1 and M2 are chosen in such a way that one metal has a workfunction higher than silicon and the other has lower.**

	Metal 1		Metal 2	
	$\phi_{m,A}$		$\phi_{m,C}$	
Au	5.1	Gd	3.1	
Pt	5.65	TiW	4.3	
Pd	5.12	Zr	4.05	
Ni	5.15	Al	4.28	
Co	5	Ta	4.25	

**Table 1.1 shows the list of available metals that we find interesting as contact metals for our CP device along with their corresponding work functions.**

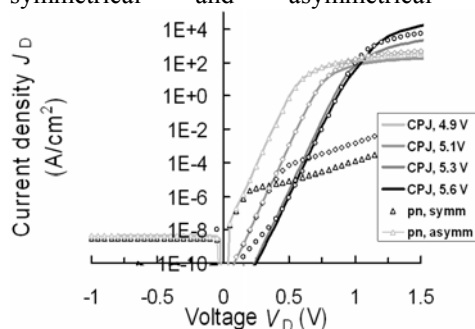
Table 1.1 summarizes the list of available metals that we find interesting to be used as contact metal 1/metal 2. The metals on the left have work function higher than Si and those on right have lower work function. The main advantages of these devices are low temperature budget and no dopant implantation is necessary in thin silicon layers.

#### 3.2 Characterization and discussion

Fig. 2b shows the schematic of a CP diode. The specifications of such a system are as follows. Firstly the workfunctions ( $\phi_{m,A}, \phi_{m,C}$ ) of the metal gates should be different from that of silicon, in which  $\phi_{m,C} < \chi_{Si} + \frac{E_G}{2q}$  and  $\phi_{m,A} > \chi_{Si} + \frac{E_G}{2q}$  are the workfunctions of the cathode and

the anode, respectively. Other parameters are the elementary charge ( $q$ ), the electron affinity of bulk silicon ( $\chi_{\text{Si}} = 4.17\text{V}$ ) and the bandgap of bulk silicon ( $E_G$ ). Secondly, the thickness of the silicon body should be chosen to be less than the Debye length, i.e.  $L_D \propto \sqrt{\frac{\epsilon_{\text{Si}} \cdot u_T}{q \cdot (n+p)}}$

( $\epsilon_{\text{Si}}$  is the dielectric constant of silicon,  $u_T$  the thermal voltage and  $n, p$  are the electron and hole concentrations respectively in the body). For this situation the charge underneath both gates in the silicon is primarily determined by charge carriers, and the depletion charge can be neglected irrespective of the doping concentration in the silicon layer. Consequently, at thermal equilibrium due to the low value of  $\phi_{m,C}$  an electron plasma is formed at the cathode. Likewise, at the anode a hole plasma is formed due to the high  $\phi_{m,A}$  and hence a CP p-n junction is formed. The current is strongly controlled by the gates. When the charge carrier concentration is low, the Schottky barrier height of the metal gate effectively determines the current. On the other hand when the charge carrier concentration is high, the charge carrier concentration determines the current. In order to determine the current densities that one could expect from such a device, we simulated a simple p-n diode contacted by metals of different work functions and also compared it with conventional symmetrical and asymmetrical p-n junctions.



**Fig. 8 shows simulated current density data  $J_D$  of the CP p-n diode (drawn lines) ( $L=0.25\mu\text{m}$ , total device length= $1\mu\text{m}$ ), the conventional uniformly doped p-n diodes having the same device geometry (symbols) versus the diode voltage  $V_D$  ( $T = 300\text{K}$ ).**

The simulation results are shown in fig. 8. The work function of the anode in the CP p-n junction was varied between 4.9 V and 5.6 V and the doping concentration in the conventional symmetrical p-n junction has been simulated for  $10^{14}$ ,  $10^{17}$  and  $2.5 \cdot 10^{19}\text{cm}^{-3}$ . In the asymmetrical p-n junction on one side of the doping has been varied and at the other side of the junction a doping concentration of  $10^{19}\text{cm}^{-3}$  has been taken. So, from the simulations we find that current densities of very high magnitude can be achieved by simply varying the work functions and distance between the metal contacts. We fabricated few test devices using poly-Si on top of grown oxide instead of SOI and contacted them with high work function metal (Pd) on one side and low work function metal (TiW) on the other. Fig. 9 shows microscope image of a

fabricated device. A thorough investigation of our devices is yet to be made and is an ongoing work.



**Fig.9 shows the microscope image of a fabricated CP device.**

#### IV. CONCLUSION

We propose two types of p-i-n diodes, one of which is novel, to study the size dependencies on electronic transport properties. We have shown the relation between thinning of the intrinsic region of a silicon p-i-n diode on the forward currents and on the reverse breakdown voltages. Further, from our experiments it is clear that using a thick BOX layer or an intrinsic region with smaller length is required for obtaining a uniform electric field. Despite this fact, we have experimentally shown increase in breakdown due to quantum confinement in ultra-thin silicon layers of around 10-nm. In our future studies a more in-depth analysis into these effects in layers thinned in both 1 and 2-dimension (fins) for both type of diodes will be made.

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