

A 60GHz Low-Noise High-Linearity Receiver Front-End Design

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Abstract—The rapid growth of wireless communications for broadband wireless personal area networks has sparked interest in the exploitation of unlicensed 60GHz bands. This paper describes a low-noise and high-linearity design approach for integrated low noise amplifier (LNA) and mixer design at 60GHz bands. The LNA power gain may be reduced along with optimum noise source termination for the mixer while maintaining a required receiver noise figure (NF), which leads to a better linearity for the receiver without any tradeoff with noise and power consumption. A 60GHz low-IF receiver front-end consisting of a single-stage cascode LNA and a singly-balanced mixer simulated in a 90nm CMOS technology is designed to verify the idea. The receiver front-end achieves a SSB noise figure of 9.6dB and an input IP3 of -14dBm while consuming 5.4mA from a 1.2V supply.

Index Terms—Low-IF receivers, CMOS receivers, mixer noise match, 60GHz circuits, 60GHz receivers.

I. INTRODUCTION

The rapid growth of wireless communications for broadband wireless personal area networks (WPANs) has sparked interest in the exploitation of millimeter-wave (mm-wave) bands using CMOS RF integrated circuits [1]–[6]. Realizing Gbits/s data throughput with a relaxed requirement on spectral efficiency may require much greater channel bandwidth. The 3GHz of bandwidth available worldwide between 59 and 62GHz could be exploited for this purpose [7].

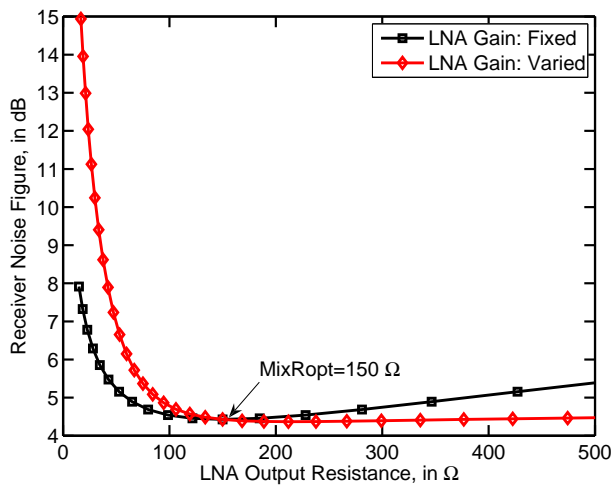
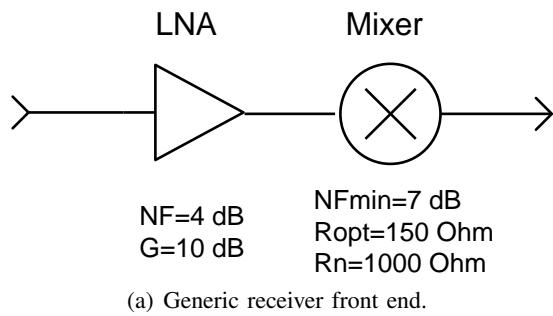
According to the classic Friis formula [8], high power gain from the LNA is crucial to suppress the noise contribution of the mixer and other receiver stages. To obtain a high power gain (e.g., 15-20dB) at 60GHz bands, a multi-stage design is essential due to low maximum available gain (MAG) from active devices (e.g., 8dB

per transistor in a 90nm bulk CMOS technology) and high insertion loss of passive components (e.g., about 1dB/mm loss for a typical coplanar waveguide implementation [9]). In other words, a high power gain implies a high power consumption and probably large chip area. Furthermore, the high gain from the LNA may impair the mixer and overall receiver linearity performance.

Alternatively, this paper describes a low-noise and high-linearity design approach for integrated LNA and mixer design at 60GHz bands. The LNA power gain may be reduced along with optimum noise source termination for the mixer while maintaining a target receiver noise figure (NF), which leads to a better linearity for the receiver without any tradeoff with noise and power consumption. Section II of this paper presents a system-level receiver front end noise simulation, and a 60GHz low-IF receiver front-end consisting of a single-stage cascode LNA and a singly-balanced mixer simulated in a 90nm CMOS technology is described in Section III.

II. SYSTEM-LEVEL RECEIVER FRONT-END NOISE SIMULATION

Fig.1(a) shows a generic receiver front-end diagram which consists of a low-noise amplifier (LNA) and a mixer with nominal design parameters. For simplicity, assume purely resistive for LNA output impedance and mixer optimum source impedance for minimum noise figure (i.e., ‘MixRopt’ in Fig.1(b)). In the system-level simulation, for the LNA, the nominal power gain is 10dB and the noise figure is 4dB; for the mixer, the minimum DSB noise figure of 7dB is achieved at an optimum source resistance of 150Ω or an optimum source reflection coefficient (i.e., S_{OPT}) of 0.5 when R_n is 1000Ω. Two scenarios are simulated using behavioral



(b) Noise figure versus LNA output resistance.

Fig. 1. System-level receiver noise figure simulation.

models in Agilent ADS: one is for an LNA with a fixed power gain (i.e., independent of the variation of LNA output resistance), and the other scenario is for an LNA with power gain proportional to the output resistance.

Simulated receiver noise figure versus LNA output resistance is shown in Fig.1(b). For the scenario with fixed LNA power gain while varying the LNA output resistance, the overall minimum noise figure for the receiver is achieved exactly when the LNA output resistance equals the mixer optimum source resistance (i.e., 150Ω). The maximum noise figure degradation at lower output resistance regime can be as large as 3.5dB even though the LNA power gain is kept constant. If LNA power gain changes proportional to its output resistance, the optimum LNA output resistance for minimum receiver noise figure is about 200Ω, i.e., slightly different with the nominal 150Ω, but with only 0.05dB noise figure deviation. As expected, further increasing LNA power gain to 20dB and output resistance to 500Ω does not help improve the receiver noise figure.

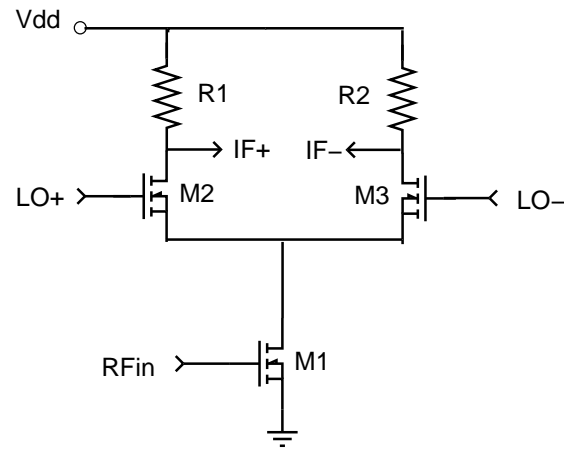


Fig. 2. Singly-balanced mixer schematic.

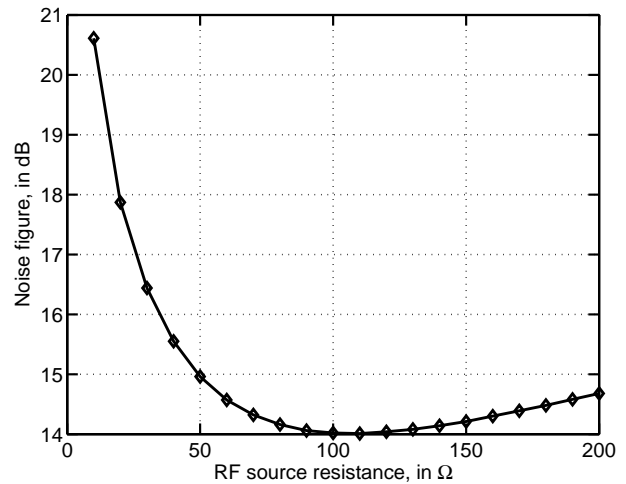


Fig. 3. Simulated mixer noise figure versus source resistance.

III. LOW-NOISE AND HIGH LINEARITY DESIGN OF 60GHZ RECEIVER FRONT-END

In this section, a 60GHz receiver front end is designed for low noise and high linearity in a 90nm CMOS technology. The receiver design starts with the mixer to firstly find out the optimum source impedance for the mixer and the required LNA power gain to achieve a certain overall noise figure for the receiver front end.

Fig.2 shows a simplified schematic for the singly-balanced mixer. In the simulation, a 60GHz RF signal is downconverted to 1GHz IF by a LO at 61GHz. Minimum mixer noise figure (i.e., 14dB) is obtained at an optimum source resistance of 100 Ω (see Fig.3).

Before diving into detailed LNA design, a behavioral model based LNA (similar as in Section II) is integrated with the mixer (see Fig.2) and simulated to find out

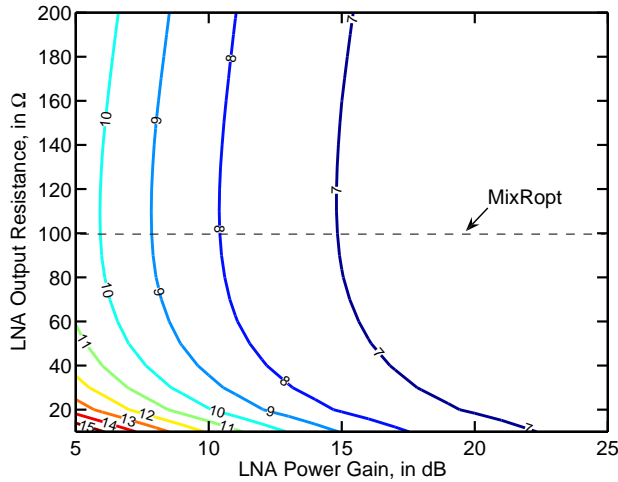


Fig. 4. Simulated receiver noise figure contour (with an ideal LNA: NF=6.3dB).

required LNA power gain to achieve a certain overall receiver noise figure. Fig.4 shows simulated (idealized) receiver noise figure versus both LNA power gain and output resistance. The optimum LNA output resistance is indeed $100\ \Omega$, as predicted in Fig.3. To obtain a receiver noise figure of 10dB, either (8dB, $100\ \Omega$) or (15dB, $10\ \Omega$) for the LNA power gain and output resistance combination is possible candidate. Nevertheless, with only 8dB LNA power gain, the receiver linearity can be improved significantly (i.e., roughly 7dB IIP3 improvement compared to the LNA with 15dB power gain).

For a power gain of 8dB, one cascode stage may be sufficient for the LNA. Fig.5 shows the cascode LNA schematic with resonant loads. Series inductors are placed at the interstage node of cascode stages to resonate with the parasitic capacitance to enhance power gain and reduce noise contribution from cascode transistor when operating at 60GHz bands. All inductors are lossy with a typical Q-factor of 10, which may be realized by microstrip lines or coplanar waveguides. The transistors are biased at a current density of $0.15\text{mA}/\mu\text{m}$ for minimum noise figure and the simulated unit current gain frequency (i.e., f_T) is above 120GHz. The output impedance of the LNA is tuned to $(101 + j51.4)\ \Omega$, to equalize the output resistance with the mixer optimum source resistance (as indicated in Fig.3). The amplifier achieves a noise figure of 6.4dB, a voltage gain of 8.4dB while loaded with the input capacitance of the mixer, or a power gain of 6dB (with a $50\ \Omega$ termination). The LNA consumes 3mA from a 1.2V supply. When

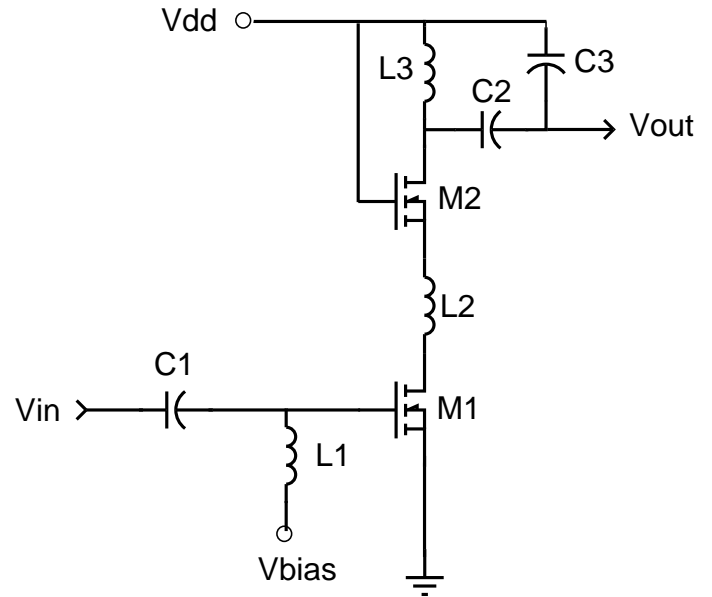


Fig. 5. Simplified LNA schematic.

the cascode LNA integrated with the singly-balanced mixer, the overall noise figure is 9.6dB, which is close to the prediction in Fig.4. The IIP3 at the LNA input is -14dBm .

IV. CONCLUSIONS

A low-noise and high-linearity design approach is described in this paper for CMOS integrated receiver front end at mm-wave bands. The system-level noise simulation of integrated LNA and mixer stages indicates the LNA power gain may be reduced along with optimum noise source termination for the mixer while maintaining a required receiver NF. Therefore, a better receiver linearity may be achieved without any tradeoff with noise and power consumption. A 60GHz low-IF receiver front-end consisting of a single-stage cascode LNA and a singly-balanced mixer is designed and simulated in a 90nm CMOS technology to verify the idea.

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