The Effect of the Contact Window Edges on the Perimeter Currents of Shallow Junction Diodes

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***Abstract*—Ultra shallow junction diodes are fabricated by low energy implantation into contact windows and activation by excimer laser annealing. The diode characteristics are measured on devices with various sizes and the area and perimeter currents are identified. It is found that the perimeter current is dominant at the applied voltage level, and this current is related to the contact window opening method.**

***Index Terms*—Excimer laser annealing, Ultra-shallow junctions**

I. Introduction

LASER annealed junctions and contacts are attractive for integrated circuit technologies where ultra-shallow junction depth or low thermal budget is required. Such technologies are ultra-large-scale integrated circuits, where further lateral downscaling requires shallow S/D extensions. Another application is high frequency silicon-on-anything technology, where dopant activation in a furnace is not applicable due to thermal limitations. By laser annealing, the diffusion of the dopants only happens locally in the laser melted region with a very low thermal budget affecting only the irradiated surface.

Fabrication of near ideal shallow junction diodes was demonstrated by implanting low energy dopants into contact windows and activating them by excimer laser annealing [1] just before the metallization. This straightforward process flow was tuned in order to have low surface roughness in the contact windows [2] so that the uniformity of the implanted region is maintained for the laser melt/recrystallisation process. Nevertheless non-idealities of the diodes are observed. At this stage they are attributed to edge effects and non-annealed defects caused by ion-implantation [3].

In this study the edge effects of the diodes are investigated. Both p^+n and n^+p diodes are fabricated by 5 keV BF_2^+ and As^+ implants under tilted implant angles. A XeCl laser (308 nm, 66 ns, single pulse) is used with energy densities of 700 – 1100 mJ/cm^2. The electrical characteristics are studied through measured I–V curves. Perimeter and area currents are separated by measuring on devices with various sizes and shapes. The perimeter current content was found to be high even in cases where the reverse leakage of the diodes was low.

In general the results presented here can be associated to the quality of the contact window edges and the surface roughness. By controlled removal of the reflective Al mask and the oxide isolation during wet etch steps, near-ideal diodes can be produced with good uniformity and reproducibility.

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II. Experimental

The basic process flow for the fabrication of laser annealed diodes is shown in Fig.1 for p^+n diodes. The starting material is 4 in (100) p-type silicon wafers that are patterned with both n- and p-type regions with a surface doping of 10^{17} cm^{-3}. The p^+ and n^+ regions to be laser annealed are formed by a 5 keV, 2 x 10^{15} cm^{-2} BF_2^+ and As^+ implantations, respectively. Buried layers and deep implants are employed in some structures to allow contacting via the surface rather than from the back of the wafer and to achieve low diode series resistance.

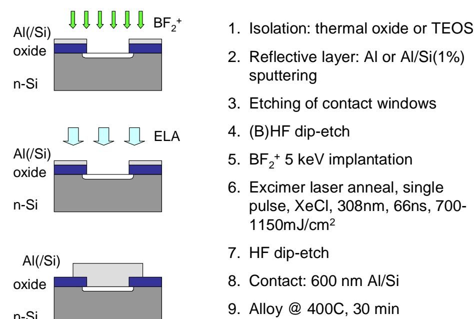

Fig. 1. Schematic of basic process flow for fabrication of p^+n laser annealed diodes.

The ELA junction implants are performed directly in the contact windows, which has the advantage that no high temperature thermal processing is necessary after the laser anneal to complete the devices and the characteristics achieved by pure laser activation can be studied.

The process conditions and parameters are as follows: the 330 nm thick surface isolation layer is a stack of 30 nm thermal oxide covered with 300 nm LPCVD TEOS. The ELA reflecting masking layer is 100 nm Al/Si(1%) deposited by

PVD at 50 °C. The contact windows are defined by different combinations of plasma and wet etching through the Al and oxide to the silicon. The actual landing on the silicon is performed with most of the oxide is etched with the high power plasma, and the landing to the silicon surface is a wet landing using 1:7 BHF. The implantation was performed with a 30° tilt with 8 equal rotations.

The laser annealing after the implantation was performed in a vacuum, using a commercial XMR5121 XeCl excimer laser system with a wavelength of 308 nm, pulse duration of 66 ns (full width at half maximum), single pulsed. On each wafer the laser energy densities are varied from 700 to 1150 mJ/cm^2 in columns.

The devices are completed by a standard metallization process. A 4 min HF dip-etch step is performed to remove the native oxide before the metallization. In this step most of the Al/Si mask is also removed. A new layer of 600 nm Al/Si(1%) is sputtered, patterned and alloyed at 400 °C for 30 min in forming gas.

The diode I–V characteristics were measured on rectangular and ring shaped diodes (Fig. 2) with various sizes (Table I-II) using a HP4156B parameter analyzer and a Cascade probe station.

TABLE I. GEOMETRY OF THE RING STRUCTURES

Ring width w [µm]	Perimeter, P [µm]	Area, A [µm^2]	P/A [µm^{-1}]
1	863.565	430.75	2.0048
2	865.565	861.50	1.0047
4	869.562	1723.15	0.5046
6	873.565	2584.80	0.3380
10	881.565	4307.80	0.2046

TABLE II. GEOMETRY OF THE RECTANGULAR STRUCTURES

Length l [µm]	Width w [µm]	Perimeter P [µm]	Area A [µm^2]	P/A [µm^{-1}]
1	1	4.0	1	4.00
1	2	6.0	2	3.00
0.5	40	81.0	20	4.05
0.8	40	81.6	32	2.55
1	40	82.0	40	2.05
1.2	40	82.4	48	1.72
2	40	84.0	80	1.05
4	40	88.0	160	0.55
6	40	92.0	240	0.38
10	40	100.0	400	0.25
40	40	160.0	1600	0.10
1	20	42.0	20	2.10
4	20	48.0	80	0.60
10	20	60.0	200	0.30
40	20	120.0	800	0.15

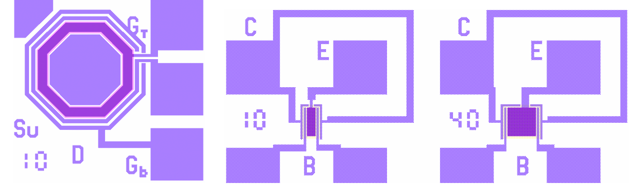

Fig. 2. Example of ring and rectangular devices used here to test diodes.

III. RESULTS AND DISCUSSIONS

The diode I-V characteristics were measured all over the wafer on several devices in the -1–1 V interval, and any further data processing were done in this window. The slope of the forward characteristics are measured, the on current at 0.4 V forward bias, the off current at 1 V reverse bias.

The measured current is considered as a sum of two components (1), namely the area and perimeter currents. The bulk current can be characterized by the current density, *J*, while the current at the edges of the diodes by the perimeter current density, *K*. The geometry is introduced by the area, *A* and the perimeter, *P* parameters.

$$I = I_A + I_P = A \cdot J + P \cdot K \tag{1}$$

The current components can be distinguished by measuring on devices with different aspect ratios.

A. Ring shaped diodes

The perimeters of the ring shaped diodes used here are practically constant with an average value of 870 µm, while the area varies with the ring width. For this reason the perimeter current is constant while the bulk current varies. Current components can be separated by fitting the data on I–A graphs with a line. The slope of the line is the current density, and the intersection of the line with the vertical axis is the perimeter current. We used the I–w graphs for the analysis, where the ring width, *w*, is proportional to the area by the mid ring perimeter (431 µm).

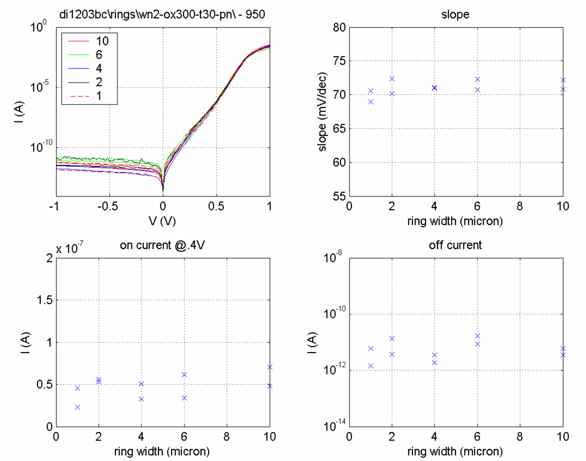

Fig. 3. Characteristics of ring shaped diodes with different ring width, annealed at 950 mJ/cm^2; I–V graph (top left), slope at forward bias (top left), on current at 0.4 V (bottom left), off current at -1V (bottom right).

Fig. 3 is an example for p^+n diodes annealed at 950 mJ/cm^2 and it shows the necessary data for the analysis. The I–V curves are plotted for all the devices and the slopes of the forward characteristics are calculated. An ideal diode has a forward slope of 60 mV/dec, which is related to the diode ideality factor of 1. Any larger values than that means that non-idealities are present. I–V curves with large deviations from the average ideality factor are excluded from the analysis.

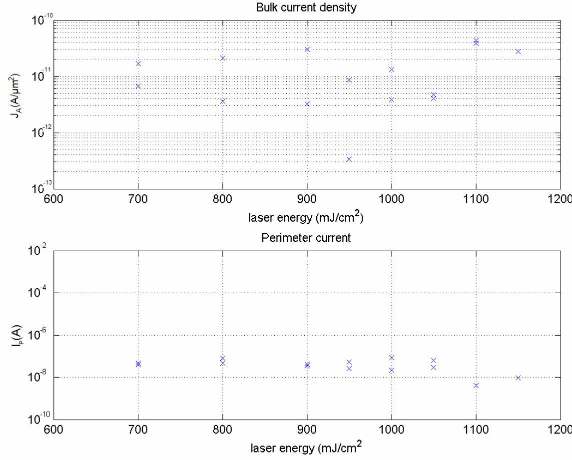

Fig. 4. Bulk current density and perimeter current versus laser energy for p^+n diodes.

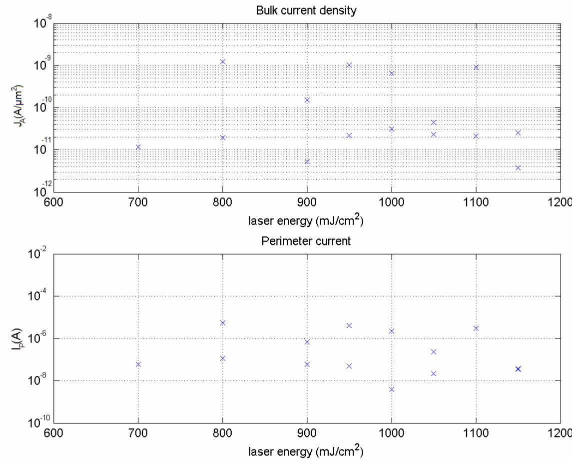

Fig. 5. Bulk current density and perimeter current versus laser energy for n^+p diodes.

The analysis results – the bulk current density, J and the perimeter current I_P – are shown for all the used laser energy density range in Fig. 4 and 5 for p^+n and n^+p diodes, respectively. Current levels are higher for the n^+p than the p^+n diodes, the As^+ implanted diodes are slightly more leaky, but the perimeter leakage is rather high for both types. A large scatter of the data is also a result of the leakage of the diodes, as the goodness of fit on I–w graphs like in Fig. 3. is low.

The analysis was also applied on previously processed diodes, where the implantation windows were opened through Al/Si and thermal oxide masking layers by using a high power plasma down to the silicon surface (hard landing), and an HF dip etching was performed before the implantation. Table IV summerizes the results with the average values of the parameters for the various runs and types of diodes. The perimeter current as well as the reverse curent is reduced by the wet landing process.

TABLE IV. COMPARISON OF PROCESSES FOR RING SHAPED DIODES

	Wet landing		Hard landing
	p^+n	n^+p	n^+p
J [A/μm^2]	2x10^{-11}	3x10^{-10}	2x10^{-9}
K [A/μm]	1x10^{-9}	3x10^{-9}	2x10^{-8}
slope [mV/dec]	68	73	67
I_{off} [A]	3x10^{-12}	4x10^{-12}	1x10^{-11}

B. Rectangular diodes

The rectangular diodes are smaller in size but cover a larger perimeter-to-area interval. However neither the area nor the perimeter is constant, thus the separation of the current components can be more complex. Assuming that the perimeter current is dominant (or the bulk current is small), a simple approach can be applied: dividing eq. (1) by A, would suggest that a linear fit can be applied on the plot of the bulk current density versus the P/A ratio. The slope of the line is then the perimeter current density. The bulk current density than can be tuned in order to have a good fit of the measured and recalculated currents on the I–A graph.

Fig. 6 shows the results for n^+p and p^+n diodes, respectively. At the applied voltage level, the n^+p diode conducts a larger current, and therefore the data is less noisy and the goodness of the fit is better. The I–A graphs show reasonably good fit with the simple approach. The recalculated currents reflect the dual parameter dependence when the perimeter leakage is present and has a strong effect. Nevertheless a deviation to the fitted trend is observed in many cases at the largest structures as they conduct less current than expected. This might be explained with a non-linear dependence of the perimeter current density on the perimeter. The results for the rectangular diodes are summarized in Table V. The parameters agree with the ones extracted from the ring diodes.

TABLE V. COMPARISON FOR RECTANGULAR SHAPED DIODES

	Wet landing	
	p^+n	n^+p
J [A/μm^2]	2x10^{-11}	3x10^{-10}
K [A/μm]	1x10^{-9}	3x10^{-9}
slope [mV/dec]	68	70
I_{off} [A]	1x10^{-13}	1x10^{-12}

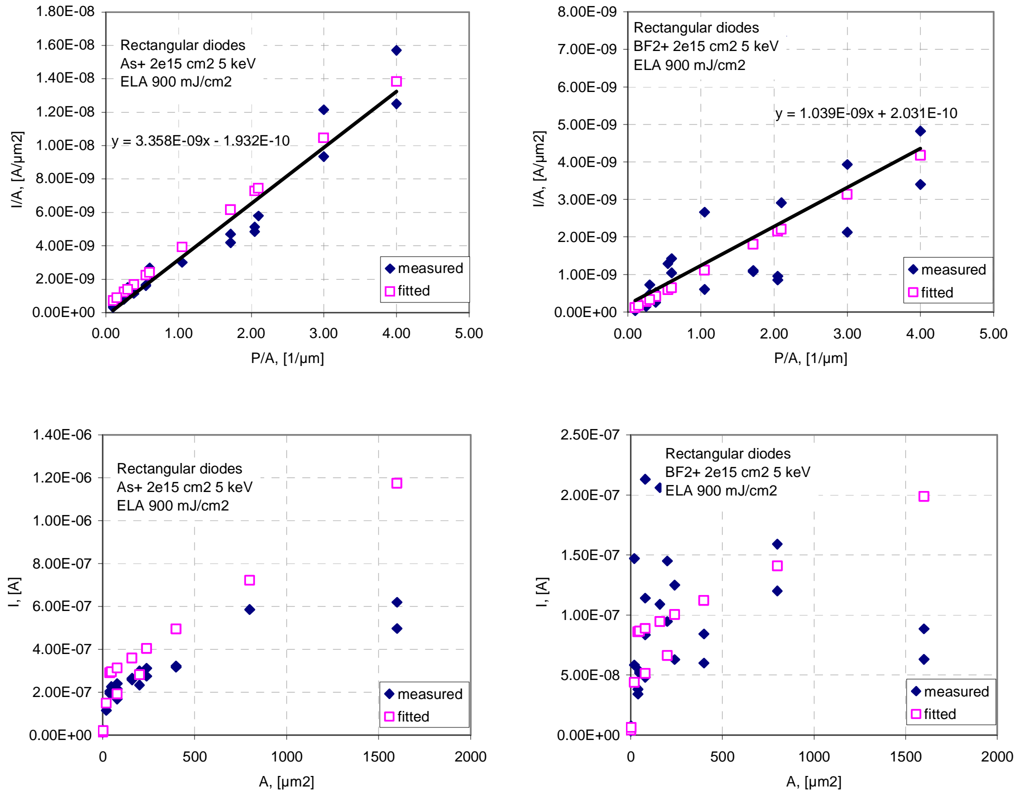

Fig. 6. Extracting the perimeter current for the rectangular n^+p (left) and p^+n (right) diodes (top), I–A graph (bottom).

TABLE VI. PERIMETER CURRENT CONTENT AT DIFFERENT P/A RATIOS AT 0.4 V

P/A $[\mu m^{-1}]$	I_p/I [%] p^+n	n^+p
4.00	97.12	99.51
3.00	96.19	99.35
2.05	94.53	99.05
1.05	89.86	98.17
0.55	82.27	96.56
0.38	76.38	95.14
0.25	67.83	92.74
0.10	45.76	83.64

The perimeter current content defined as I_P/I is calculated from the extracted *J* and *K* values are shown in Table VI for various *P*/*A* ratios. The perimeter current is dominant at the smallest devices, and its significance reduces with the increasing area, but it is still large at the applied voltage level.

IV. CONCLUSION

In order to evaluate the perimeter and bulk current components on laser annealed ultra shallow junction diodes, we measured and analyzed the electrical characteristics of diodes with various shapes and aspect ratios. The results show that the perimeter current is large. Further experiments are to be carried out to reduce the perimeter leakage of the devices.

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