

Self aligned fabrication process for carbon nanotube based field-effect devices: transistors, memory cells and bio-sensors.

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Abstract—We present in this work our new fabrication process for single-walled carbon nanotube (SWNTs) based devices. The process is based on chemical vapor deposition growth of the nanotubes using a sacrificial catalyst. SWNTs are grown directly on their final place avoiding any manipulations. Furthermore, only one-step lithography is necessary, not only in order to contact the devices but also to passivated them simultaneously. Polymethyl methacrylate (PMMA) is used as a passivation layer to protect the SWNTs from ambient air and increase the life time. Thanks to this suitable process, we have already fabricated around 15,000 passivated devices. Moreover, we show that our CNTFETs are suitable for memory applications. They can be used as non-volatile memory cells operating at room temperature. The memory function is obtained by the threshold voltage shift due to the highly reproducible hysteresis in the transfer characteristics. The ratio of the current levels between a logical “1” and a “0” is about 10^6 . Lastly, CNTFETs are ideally suitable for biomedical sensor applications due to their excellent inherent properties such as ultra small size, high specific surface area, extremely high sensitivity and the above mentioned hysteresis effect. For example, the detection and identification of single viral particles may be possible using functionalized CNTFETs as sensors: The binding of a virus to a suitably functionalized semiconducting SWNT will measurably affect the gate-dependent electrical current-voltage characteristics of the transistor via charge transfer between the SWNT and the virus.

I. INTRODUCTION

Carbon nanotube field-effect transistors (CNTFETs) are currently fabricated and investigated by many research groups since they are one of the most promising candidates for future nanoelectronics. For single-walled carbon nanotube (SWNT) growth, two main methods are used: separate growth of SWNTs usually by laser ablation and dispersion from a solvent by spinning onto the silicon wafer [1], or in-situ growth of the SWNTs directly on the wafer with chemical vapor deposition (CVD). Concerning the integration process, multi-step lithography is often required implying a misalignment risk [2]. The purpose of this work is the development of a very simple self-aligned fabrication-process, where SWNTs are grown homogeneously on unstructured Si-wafers used as back gate electrode. It is based on in-situ CVD growth of SWNTs using a sacrificial aluminum/nickel catalyst. We choose the in-situ growth method because it looks most practical for future use in microelectronics where millions of transistors need to be

fabricated at the same time. It avoids complicated and hazardous manipulations of the SWNTs at the nanoscale. Furthermore, the process does not contain multi-step lithography because palladium electrodes are patterned at the end of the process on the bare wafer surface covered with SWNTs, avoiding the risk of misalignment.

II. CNTFET FABRICATION PROCESS

Highly doped p-type silicon wafers have been chosen to fabricate the CNTFETs because the substrate is used directly as a back gate electrode and should then have a good conductivity. The wafers are first oxidized (40 nm SiO_2) in order to isolate the SWNTs from the gate electrode, i.e., the silicon substrate. Subsequently, a metal stack of 0.5 to 1 nm Ni on 5 to 10 nm Al is deposited on the whole wafer surface with electron beam evaporation. These are well-known combinations for catalyzing SWNT growth selectively (i.e., avoiding multiwalled nanotube growth). Subsequently, the wafers are annealed to about 870°C in a CVD reactor in N_2 at atmospheric pressure for 5 min to form Ni nanoclusters, which act as catalyst particles for SWNT growth. Subsequently, SWNT growth occurs for 10 min in a CH_4/H_2 mixture at the same temperature in the same furnace uniformly across the wafer surface. During this high-temperature step and because of reaction with SiO_2 , the thin metal catalyst converts into an Al_xO_y film (high-k dielectric) covered with discontinuous Ni nanoclusters. The 5 to 10 nm Al converts into Al_xO_y because of reaction with SiO_2 during the high-temperature step (i.e., oxidation of the lower part of the Al layer at the SiO_2 interface). In addition, the continuous 0.5 to 1 nm Ni film turns into nanoclusters during CVD. The discontinued Ni layer allows ambient air contact from the top, resulting in the oxidation of any residual metallic fraction in the top part of the Al layer. The metallic catalyst converts into a high-k dielectric (i.e., Al_xO_y), which is not conductive. The catalyst can indeed be called “sacrificial”: it will not short-circuit future devices laterally and will allow the vertical gate field to penetrate and control the current flow within the SWNTs as it is a dielectric. For contacting the nanotubes and passivating the transistors, only one-step lithography is required. Such a self-aligned process is time-saving, cheap and reliable (i.e., no risk of misalignment). First, the wafers are heated for 2 h in a dry chamber to remove humidity and then an adhesion promoter (A1100) is applied under vacuum. For the photolithography, a

two-layer-system from All Resist is used. Polymethyl methacrylate (PMMA), a copolymer based on methyl methacrylate and methacrylic acid, is spin-coated and dried. The photoresist (novolac-naphthoquinondiazide combination) is brought on top of this tempered copolymer layer. Only the photoresist is photosensitive (positive resist): the exposed parts are removed in the developer. The PMMA layer does not react with light but is etched by the developer at a defined rate. This etching is isotropic and undercuts are formed. After lithography, the wafer is evaporated with palladium as its high work function is known to provide Schottky-barrier-free contact to SWNTs [3]. During evaporation, the wafer support rotates so that the undercut is also coated with palladium until the PMMA layer is reached. Subsequently, the photoresist covered by Pd can be lifted off with an acetone-based remover that does not etch PMMA when the handling time is sufficiently short. A handling time of 15 to 30 s is used with subsequent 5 s ultrasonics. To even more protect PMMA from being etched, the wafer can also be measured without liftoff at all. The 700 nm thick PMMA layer and the 3 μm thick photoresist isolate the Pd source/drain contacts from the Pd layer on the photoresist so that there are no short circuits between the electrodes. The last step is the SiO_2 etching of the back side of the wafer with a drop of HF because the silicon substrate, which is used as the back gate electrode, must have electrical contact to the wafer prober chuck. The wafer is then rinsed with water and dried. Fig.1 gives a schematic of the fabricated CNTFETs.

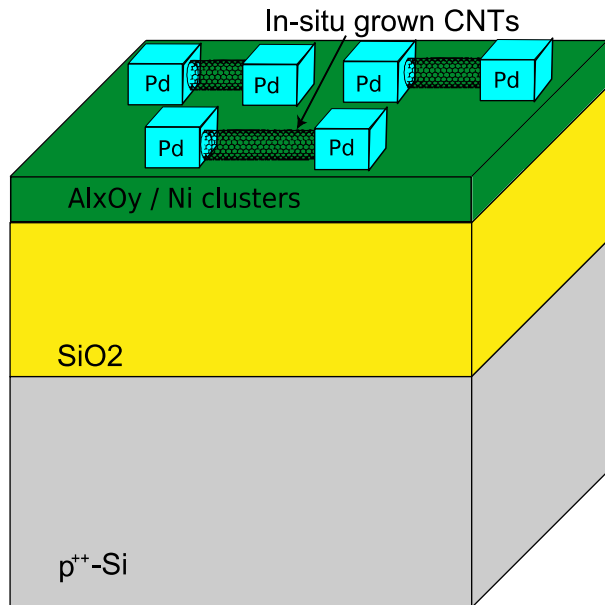


Figure 1. Schematic of CNTFET

III. CNTFET MEASUREMENTS

A. Transistors

To show the effect of passivation, passivated and nonpassivated devices have been fabricated and measured. The only difference in the process is the remover for liftoff. For the fabrication of passivated devices, the remover is acetone-based and does not attack PMMA when the handling time is short. As a result, the channel is covered with a

copolymer layer of about 700 nm (see Fig. 2 left for AFM topographical measurement of a passivated transistor). For the fabrication of nonpassivated devices, the remover is NMP-based and dissolves the photoresist and PMMA simultaneously. The channel area has direct contact to ambient air between the 80 nm Pd electrodes (see Fig. 3 left).

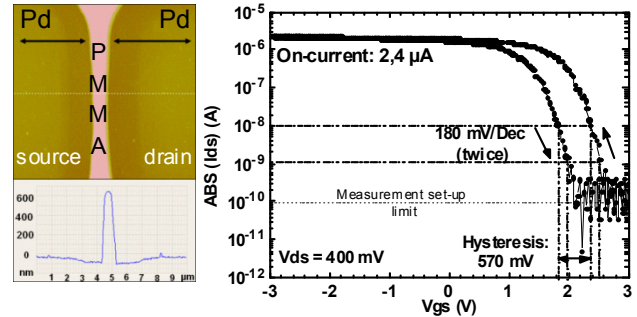


Figure 2. AFM topographical scan (left) and transfer characteristics (right) of passivated CNTFET with semiconducting SWNT as channel.

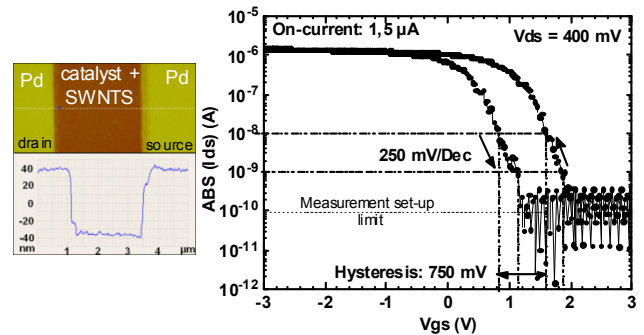


Figure 3. AFM topographical scan (left) and transfer characteristics (right) of nonpassivated CNTFETs with semiconducting SWNT as channel.

Figures 2 (right) and 3 (right) show two typical examples of transfer characteristics measured on passivated and nonpassivated devices, respectively, where the SWNT linking the source and drain is semiconducting. Both devices have an on-current of about 2 μA (i.e., 2 $\text{mA}/\mu\text{m}$) at a V_{ds} of 400 mV and an on/off ratio of about 10^4 (note that the off-current sensitivity is limited by the measurement setup). However, passivated CNTFETs show improved characteristics in comparison with nonpassivated ones: the slope and the hysteresis are smaller (respectively 180 mV/dec for passivated CNTFETs instead of 250 mV/dec for nonpassivated ones and 570 mV instead of 750 mV). This is not exactly the expected result: though the hysteresis decreases, it is still present. Injected charges or charge traps in SiO_2 could be the reason for the hysteresis in the transfer characteristics of CNTFETs. The shift in threshold voltage could come from a reconfiguration of the carriers near the CNTs when applying a gate voltage [4]. The reconfiguration could be based on different traps or carriers that change their state depending on the applied gate voltage [5]. From the MOS technology, it is known that the oxide has fixed charges and traps in its body and also traps at the oxide/silicon interface. This could be an explanation why PMMA passivation does not completely remove the hysteresis.

One important observation is that after two weeks, more than half of the nonpassivated transistors do not function anymore, whereas more than three-quarters of the passivated devices are still fully functional. The PMMA passivation layer is then an appropriate protection layer for nanotube devices. Lastly, the remeasurement of the transistors with a new setup (Keithley 4200) recently obtained at our institute yields improved results: the noise in the off-current that could be observed in the measurement with the old setup (oscillation between -100 and 100 pA, see Figs. 2 and 3) is eliminated because the preamplifiers for the current are placed very near to the probe under the measurement box of the wafer prober. As a result, the off-current decreases to 0.2 pA and is very regular (see Fig. 7). The on/off ratio improves then to 2×10^6 .

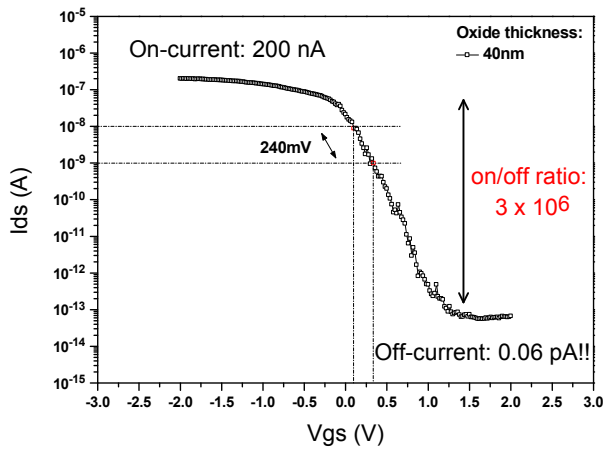


Figure 4. Remeasurement of device with semiconducting SWNT as channel (new measurement setup, Keithley 4200).

As our novel fabrication method allows growing of individual SWNTs directly within the desired device area and no tedious manual manipulation and alignment of the SWNTs is necessary, the self-aligned fabrication process allows mass-production of SWNT memory devices with high yield (Fig. 5).

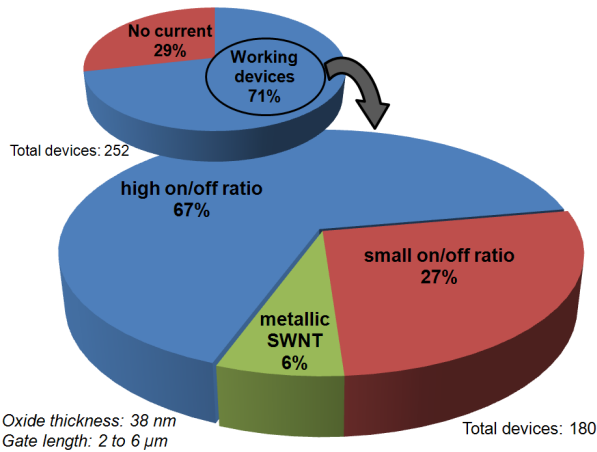


Figure 5. 15,000 CNTFET structures have been fabricated. Statistics on hundreds of electrical measurements revealed a yield of about 50% ($71 \times 67\%$) for fully functional semiconducting devices, suitable for use as CNTFET memory devices.

Statistical analysis on hundreds of electrical measurements reveals that 71% of the devices are working (i.e. there is current between source and drain) and 67% of them show excellent semiconducting behavior (on/off ratio $\geq 10^6$, see Fig. 6). 27% of the working devices have also a s-SWNT as the channel but with a small band-gap and only 6% of the working devices show a purely metallic behavior (i.e. no field-effect notable).

B. Memory

The storage of binary data in memory units is a fundamental prerequisite in information technology. Molecular memory devices with semiconducting single-walled carbon nanotubes (s-SWNTs) are promising candidates to realize ultra-dense non-volatile memory cells [6]. However, present state-of-the-art fabrication methods of CNTFETs are very time-consuming and are not suitable for fabrication of memory chips with millions of transistors.

The memory function is obtained by the threshold voltage shift (memory window) due to the hysteresis in the transfer characteristics (Fig. 6). The ratio of the current levels between a logical "1" and a logical "0" is about 10^6 .

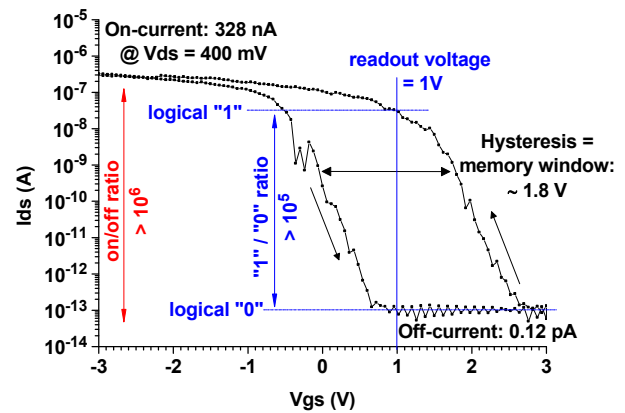


Figure 6. Example of measured transfer characteristics of fabricated CNTFET device structures with only one s-SWNT as the channel.

The "0" and "1" current levels are seen to be temporally stable and stay within the same decade for several minutes (Fig. 7). Long term data retention for more than 12 hours was also observed even at power off. More detailed measurements on data retention are in progress. Also, excellent endurance properties have been obtained after performing multiple read/write cycles. The reading current remains at the same level and depends only on the programming gate voltage applied before. Since the current levels do not depend on the previous history of read/write cycles and due to the long retention time, voltage-programmable CNTFETs have the characteristics of non-volatile memory cells.

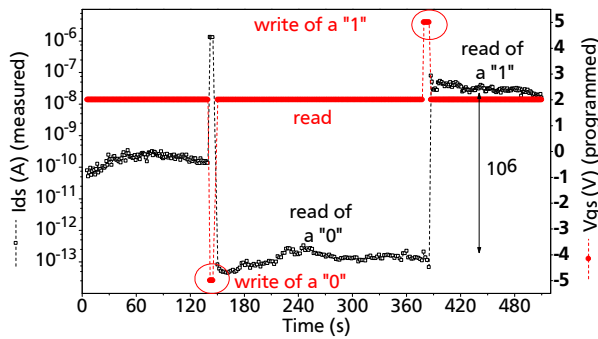


Figure 7. Cycling of CNTFET memory cell. Black triangles: applied gate voltages versus time. Red dots: measured drain current versus time.

C. Proposal: Biomedical CNT-Field-Effect Sensors

Taking advantage of the above mentioned hysteresis effect which we observe in our CNTFET devices, extremely sensitive nanosensors (i.e. CNTFES) well suitable for biomedical applications can be realized. For example, the detection and identification of single viral particles may be possible using functionalized CNTFETs as sensors as illustrated in Fig. 8: The binding of a virus to a suitably functionalized s-SWNT will measurably affect the gate-dependent electrical current-voltage characteristics of the s-SWNT via charge transfer between the CNT and the virus.

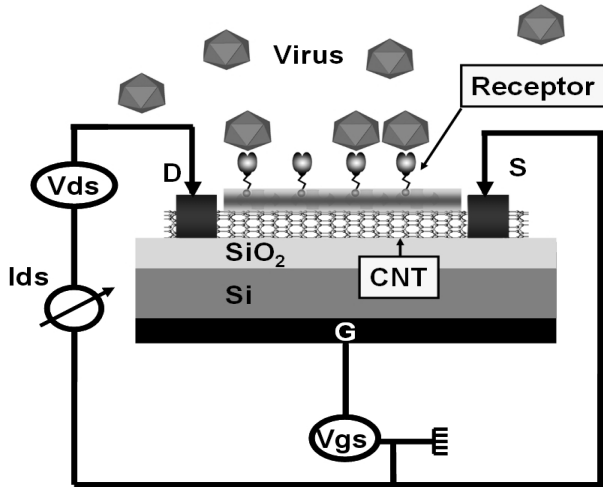


Figure 8. Illustration of proposed CNTFES for virus detection. The s-SWNT is functionalized with a suitable receptor to allow selective bonding via its protein. Extremely sensitive sensors for virus detection are feasible, since any change in the charging state introduced by the virus will alter the device characteristics via the field-effect.

The virus detection is thus performed electronically via the CNTFET (cf. Fig. 6) which will alter its electrical device characteristics in presence of a virus. The sensitivity can be enhanced further by using CNT-networks or array structures with multiple SWNTs. Furthermore, complete electronic integrated sensor circuits based on hybrid CNT-CMOS technology are envisioned which will perform data analysis on-chip (smart biosensors).

However, the main challenge for the realization of this biomedical sensor will be the proper functionalization of the CNT in order to be highly selective to the desired type of virus. This knowledge is outside of the scope of our own expertise (nanoelectronics). For a successful realization of these biomedical nanosensors, additional expertise from the biochemical and biomedical area is needed through collaborations with experts from the respective fields via research projects.

IV. CONCLUSION

In conclusion, the fabrication process reported in this work is suitable to fabricate functional CNTFETs, Pd-contacted and PMMA-passivated and that are working like P-MOSFET. The easiness of the process has to be noticed because no manipulation of the CNTs as well as no alignment of multiple lithography steps are needed. The process is silicon CMOS compatible and opens the possibility to fabricate circuits, either by structuring a top gate on the in-situ grown SWNTs or by using buried isolated bottom-gate on SOI wafers. Moreover, we have presented results on measurements of the CNTFETs as memory cells. Lastly, we have shown that the novel method for the fabrication of carbon nanotube field-effect transistors is applicable for bio-sensors due to their excellent inherent properties such as ultra small size, high specific surface area and extremely high sensitivity.

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