An Approach for an Efficient Transition from System-on-Chip to System-in-Package

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Abstract—**An approach for an efficient transition from System-on-Chip (SoC) to System-in-Package (SiP) for biomedical signal acquisition is presented. An effective work flow has been developed for the SoC-to-SiP transition and functional block separation. Block redesign for reduced interconnects has been realized. Finally, by an optimized floorplanning and die stacking for the SiP blocks an overall area reduction by a factor of 2 compared to the SoC has been achieved.**

Index Terms—**SiP, Multi-Chip-Modules, Die Stacking, Reduced Interconnects**

I. INTRODUCTION

An emergence and rapid growth of SiP applications have been seen since the mid-1990s. The development of SiP technology has benefited from the SoC technology by reusing existing integrated circuits and Intellectual-Property (IP) cores, which decreases the design effort [1]. However, it presents many challenges [2]:

1) Assembling the SiP dice: The current assembly technologies offer different choices for 3-D integration like *Die Stacking*, and *non-/Through-Silicon Vias* (TSV). These varieties make the assembly process rather complicated compared to the basic 2-D integration of Multi-Chip-Modules (MCM).

2) The substrate design: The correct choice of the substrate material and design technology to match the target application offers great opportunities for design optimization, which can be realized by transferring the large components off-the-chip. This enables 3-D design and integration of substrate-embedded passive components, which results in an overall area reduction.

3) The wiring effort: A large number of interconnects between the SiP dice can affect the application performance due to long routing and increased parasitics. Hence, adjusting the design for reduced interconnects is essential. In addition, a suitable contact methodology —Wire bonding or Flip-Chip— has to be chosen for the different dice.

The presented work addresses an efficient approach for the transition from an existing SoC to a SiP for biomedical signal acquisition. The reference SoC is described in [3]. It consists of 3 channels and combines the acquisition of multiple biomedical signals (ECG, EEG, EMG and EP) with on-chip signal processing. The first transition approach targets the low-frequency operation, while a future work package shall consider the integration of an RF module for wireless communication. SiP implementations for wireless biomedical systems have been reported in [4], where an eight-channel wireless EEG system is implemented in a 3-D SiP.

The aim of the presented SiP approach is, firstly, to add more flexibility while achieving the same reference-chip functionality, and secondly, to investigate efficient strategies to deal with the previously defined challenges in the SoC-to-SiP transition process.

In this work, as a first step, a structured work flow has been developed in order to separate the reference SoC into functional blocks taking into consideration the technology choice, the interconnects minimization, and the area reduction and optimal usage. As a second step, the separated blocks have been redesigned to reduce the number of interconnects and, hence, the wiring effort. The design optimization for off-chip passives integration is also considered in the designed work flow, however, it has not been realized in this work and is considered as a future work package.

The outline of this paper is as follows. In section II, the developed work flow for the SoC-to-SiP transition is thoroughly explained. In section III, the redesign of the different separated SiP blocks is discussed. Section IV illustrates the selected floorplanning of the SiP blocks and highlights the benefits achieved from the SoC-to-SiP transition, in addition to a comparison of the alternative assembly options for these blocks, and section V concludes the paper.

II. WORK FLOW

One goal of our work is to find decision rules which help to decide which kind of integrated circuit, SoC or SiP, is more suitable for a specified application. Since design flows are well defined for designing a system on chip, we developed a flow for converting an existing SoC design into a SiP as shown in Fig. 1.

The first step is to identify functional modules. In the best case the SoC can be divided into modules which could be used as stand alone parts. Using the floorplan of the SoC, one can

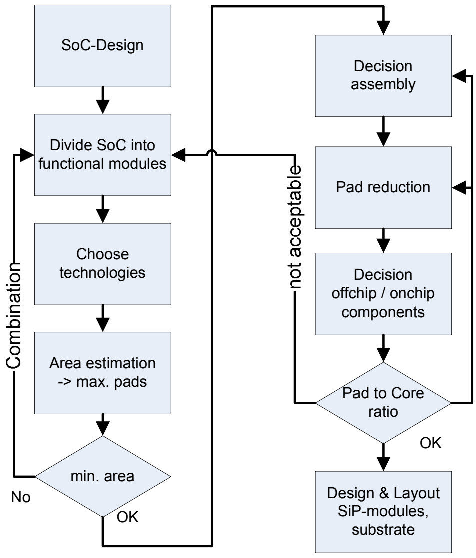

Fig. 1: Work flow to convert SoC to SiP

see which parts of the system form a functional unit, giving a good hint for the lines separation of the modules. The number of interconnects should be already considered when defining the modules, as every wire will likely result in a pad.

When the separation is done, the optimal technology for each module is chosen. The freedom to choose different technologies for a specific module enables the designer to save lots of silicon area, especially for mixed signal systems with large digital parts.

The layout of the SoC gives a good estimation regarding the area of the modules. It is important to consider the minimal dimensions of a die to facilitate assembly. For fabrication, there are often minimal sizes of a die which result in a waste of silicon area if the module is much smaller than that. If a module does not match one of these criteria, two or more modules have to be combined.

The decision about the assembly technology determines the design of the following steps. Using flip chip, the pads can be spread over the whole die area, whereas when using bond wires the pads have to be placed as a ring around the die. With new technologies like TSVs, this decision will become more and more important.

In deep submicron technologies, the pads do not scale like the rest of the design does. Hence, it is likely that the design will be dominated by the area the pads need to contact the die. To improve the utilization of the silicon area, the designer should consider ways of serializing certain data lines like busses, or adding registers with a serial interface for configuration.

The next two steps are ruled by economical concerns. From the silicon area needed for a certain device, its price can be calculated with the fabrication cost of the technology and can be compared to discrete components. The ability to exchange off-chip components has to be evaluated too and is specific to the application. The drawback of moving components off the chip is that the number of pads will increase by at least one. Furthermore, most discrete components cannot match the precision of integrated components. If there is no chance to use the silicon area efficiently, the separation of modules needs to be redone.

In Fig. 2, the resulting structure is shown. The three programmable channels are separated and each will be located on its own die. The Decimator is a pure digital circuit, hence it is manufactured in a smaller technology.

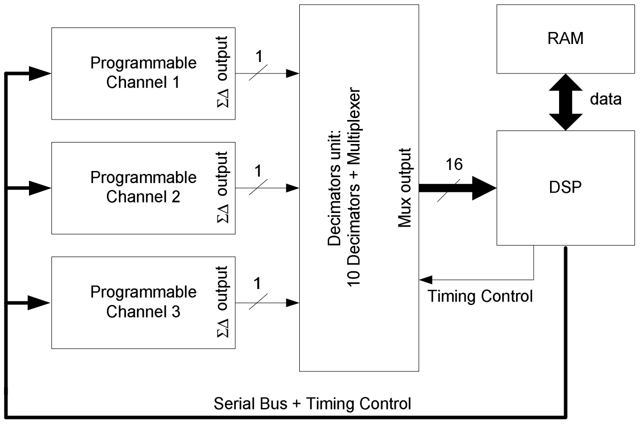

Fig. 2: Block diagram of SiP modules

III. BLOCK IMPLEMENTATION

This section explains the implementation of the different SiP blocks after being separated using the presented work flow. A redesign of the programmable analog channel and the decimator blocks for reduced number of interconnects and improved system flexibility has been achieved. The technologies selected for the implementation are the 0.35 µm and 0.13 µm technologies for the analog channel and the decimator, respectively, whereas the DSP and the RAM blocks have been chosen as off-the-shelf dice.

A. *Programmable Analog Channel*

The programmable analog channel block integrates an Analog Front End (AFE), a Sigma-Delta ADC and an R/2R DAC as shown in Fig. 3. These modules have been designed in

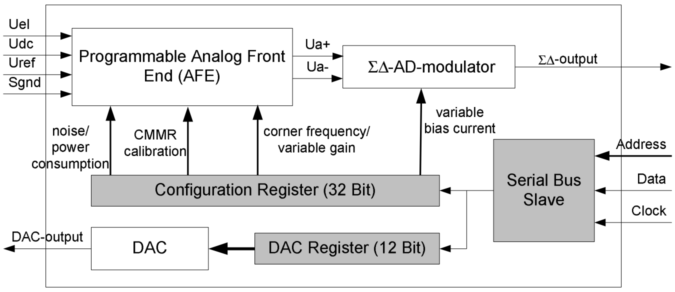

Fig. 3: Analog channel block diagram

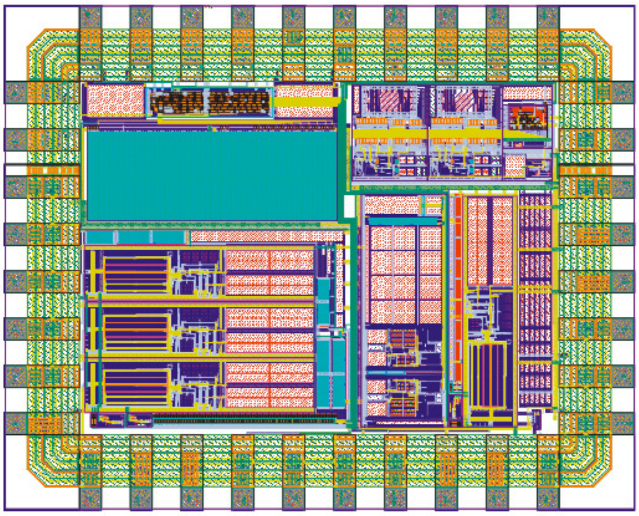

Fig. 4: Analog channel layout

[3] and updated, in an extended work [5], for an optimized performance. In this work, the updated design version of these modules is used to acquire the benefits achieved from the enhanced performance, however without affecting the structure of the reference SoC. The AFE is programmable as low-power or low-noise by external bias current and can be calibrated in terms of common mode rejection ratio (CMRR), gain and bandwidth. The resolution of the ΣΔ-ADC is specified to be at least 16-bit for EEG and EP signals, and hence designed as 20-bit. The DAC has a 12-bit resolution and is used for DC-offset compensation [5].

The structure of the reference analog channel has been modified by redesigning it for reduced interconnects. This has been realized by including an additional digital part to support the channel programmability with a serial bus and 2 shift registers as illustrated by the grey blocks in Fig. 3. Accordingly, a remarkable reduction by 30 pads, hence interconnects, has been achieved, resulting in a total of 36 pads. The layout-area of the digital part is 0.075 mm^2 which is very small compared to the analog channel core area (about 2.5%). Thus, it barely influences the overall area.

Fig. 4 shows the layout of the analog channel implemented in 0.35 μm technology. The total area of the channel is about 6.5 mm^2. The different channel blocks were arranged to obtain an optimum top-layout to enable a very small area and a relatively square architecture. This arrangement results in a pad-limited design and a core-to-pad area ratio of about 1.15. In addition, the efficient use of the pad area and the pad reduction achieved by the serial bus control, made it possible to add pads for testing the intermediate outputs of the different channel modules.

The post-layout of the redesigned analog channel has been evaluated to verify its functionality for an equivalent performance compared to the design in [5]. Simulation results show that a maximum value of 96 dB for CMRR can be achieved with the 6-bit calibration circuit. In addition, power consumptions of 1.7 mW and 21.8 mW for both the low-power and low-noise modes, respectively, have been achieved, without the ADC and the DAC modules. Other simulations involving the referred input noise measurements are done. All the achieved results are quite consistent with the ones obtained in [5].

TABLE I
FLOORPLANNING POSSIBILITIES

Assembly of Analog Channels	**Wiring**	**Area Impact**	**Effect on Parasitics**
2-D, no stacking	Flip-chip	No area reduction	Reduced parasitics
2 channels stacked in 3-D, one in 2-D	2 flip-chips, 1 wire bonding for the stacked die	Area reduction to 2/3	Increase in parasitics due to the long wires of the stacked die
3 channels stacked in 3-D	1 flip-chip, 2 wire bonding for the stacked dice	Area reduction to 1/3	Very long wires specially for the top die leading to a high increase in parasitics

B. Decimators Unit

To obtain the 20 bit data from the sigma-delta modulator, the 1-Bit-stream is decimated by three IIR and FIR filters. Since this is a digital process, a 130 nm process was chosen to fabricate this module.

The area of the filters for one channel is very small, so the decision was made to integrate filters for up to 10 channels and multiplex the data output. This adds some scalability to the system.

Nevertheless, we were not able to fully use the die area and the core utilization is only about 30%. The pad to core ratio is not good either, so it has to be investigated, if serializing the multiplexed data is feasible here. On the other hand, the decimation stage could be implemented in software on a DSP. If this is possible, the decimator unit could be omitted and the system becomes less complicated in terms of supply chain and assembly steps.

C. DSP & RAM

Depending on the application, a DSP and RAM could be added. This enables the system to acquire, digitize, process and store the data. A wide range of components, e.g. wireless, flash, UARTs, could be added easily to extend the functionality of the system. It is intended to use off-the-shelf dice, whenever possible, so the increased functionality has almost no design effort.

IV. SIP FLOORPLANNING

In this work, the non-TSV technology has been chosen for assembling the SiP blocks. This technology offers the 3-D integration of the dice with the possibility of connecting them to the substrate using either the flip-chip or wire bonding methodologies [2]. The floorplanning selected in this work for the SiP blocks aims at stacking two analog channels for area reduction, where one channel is assembled as a flip-chip and the second is stacked on its top, while the third channel is

TABLE II
SIP MODULES COMPARED TO SOC

Functional Block	SoC	SiP	Remark	Area Impact
Analog front end	350 nm, embedded	350 nm, single die	• 3.3V Vdd-technology allows greater offset voltage compensation. • Redesign of parallel to serial ports to reduce number of pads	by stacking 2 dice area reduction to about 2/3
Decimators unit	350 nm, embedded	130 nm, single die	• 1.2V Vdd for digital core to reduce power consumption • Multiplexed 16 bits data	Smaller area due to smaller technology
DSP, RAM	350 nm, embedded	off-the-shelf dice	• No design effort • Tested functionality	

directly connected to the substrate. In addition, the remaining blocks —Decimator, DSP and RAM— are assembled as 2-D directly on the substrate. The chosen floorplanning is not the optimal choice from the area point of view, as depicted in Table I, which lists the different floorplanning options together with the area benefits achieved. However, it offers a compromise between complexity and area reduction. In addition, it avoids a high increase in parasitics through the long wire bonds, which results if all the three analog channels were vertically stacked.

The estimated overall area gained from using two technologies and from stacking two analog channel dice is about 50% for the whole SiP compared to the SoC approach. Table II compares the SiP approach relative to the reference SoC chip. The table highlights the benefits achieved on the system level, which are reflected in the reduced area and the increased system flexibility. Furthermore, it illustrates the benefits gained on the circuit level illustrated in the smaller design effort and the lower power consumption compared to the SoC.

Although the SiP approach has several benefits and advantages compared to the SoC, it has also its disadvantages and challenges as previously introduced in section I. An increase of parasitics is inherent to the SiP architecture. Though the amount of parasitics will increase in any case, it is heavily dependent on the assembly technology. Using flip-chip, the amount of resistive parasitics will be kept very small, but would not allow the stacking of the dice. Hence, it can be used only with the lower die, while the upper one is connected using bond wires. Therefore, the validity of the selected floorplanning as an optimum solution has to be verified by further simulations and measurements, which is considered as a future part for this work.

V. CONCLUSION

In this work, we presented the development and use of a work flow which helps turning a SoC into a SiP and helps finding the solution which is best suited for the application. From our example, it can be shown that a SiP for a mixed signal system has certain advantages compared to a SoC. By modern assembly technologies a great area reduction can be gained, but designing a substrate is not an easy task for an IC-designer, at first. In a SiP, Frontend- and Backend-designers have to work very close together to achieve the optimal result.

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