

# Dynamic Power Management for the Xetal SIMD Processor

Vishal S. Choudhary, Anteneh A. Abbo, Leo Sevat, Richard P. Kleihorst  
Philips Research Laboratories  
Prof. Holstlaan 4, 5656 AA, Eindhoven, The Netherlands.  
EMail: {vishal.choudhary,anteneh.a.abbo}@philips.com

**Abstract**—In this paper, we investigate the benefits of dynamic power management using voltage scaling in SIMD architectures. We base our investigation on the Xetal SIMD processor targeted for pixel processing. We analyze the power consumption of the Xetal architecture and show how dynamic voltage and frequency scaling can improve the power efficiency by means of measurement results. We propose implementation techniques for dynamic voltage scaling on Xetal.

Our measurement results show more than 50% of power can be saved by supply voltage scaling of the Xetal chip. This power gain can be further improved by frequency scaling if the application does not demand full performance.

**Keywords**—SIMD, Dynamic Power Management, Voltage Scaling, Xetal, Linear Processor Array.

## I. INTRODUCTION

With the advent of deep-submicron technology systems are becoming more and more complex with increasing demand on performance. At the same time, portability, flexibility and longer battery life impose severe constraints on the power consumption of the systems. Because of the increasing cost of mask sets, ICs are designed with reprogrammability and reusability in mind. This implies that ICs are designed to serve a wide area of applications with varying performance requirements and strict power budgets. This varying workload gives an opportunity to tune supply voltage and frequency for reducing the power consumption. By scaling the supply voltage, quadratic energy gains can be achieved at the cost of reduced performance, which is acceptable if the application does not demand full performance.

In this paper, we investigate the benefits of dynamic power management for the Xetal SIMD architecture. Applications for Xetal vary from simple pixel processing tasks to complex algorithms with high computational demand. This is an ideal case for implementing Dynamic Power Management, as the state of the Xetal chip can be changed dynamically depending on the computational demand of the application.

The layout of the paper is as follows: we start with a

brief introduction of dynamic power management using voltage scaling, followed by an overview of the Xetal architecture. Next, we discuss the measurement results of the experiment we did with the Xetal chip manufactured in 0.18  $\mu\text{m}$  CMOS technology. We also give an overview of our future plans to implement voltage scaling on Xetal-II architecture.

## II. DYNAMIC VOLTAGE SCALING

Dynamic Voltage Scaling (DVS) is one of the most promising approaches in power management. The supply voltage is dynamically reduced to the lowest possible extent that ensures proper operation when the required performance of the target system is lower than the maximum performance. DVS is very efficient in situations where the system does not have to deliver its peak performance all the time. Due to the fact that total power is still dominated by active dynamic power, DVS can bring quadratic gains in terms of energy savings. Dynamic power dissipation and operating frequency of CMOS circuits is given by the following equations:

$$P_d = C_{eff} f V_{dd}^2 \quad (1)$$

$$f = k(V_{dd} - V_t)^2 / V_{dd} \quad (2)$$

where  $C_{eff}$  is the effective switching capacitance,  $f$  is the operating frequency,  $V_{dd}$  is the supply voltage and  $V_t$  is the threshold voltage. Reducing the frequency (frequency scaling) will reduce the power consumption linearly, but energy consumption remains the same for a given task. However, reducing the supply voltage  $V_{dd}$  can reduce the total energy consumption quadratically.

One of the most cited processors that supports dynamic voltage and frequency scaling is Transmeta's Crusoe TM5800. Figure 1 shows power profile of TM5800 [1]. Transmeta's power management uses a number of core frequency/voltage operating points, allowing Crusoe TM5800 processors to optimize for the lowest power and maximum performance along its operating curve, as shown in figure 1. This ensures the processor delivers high

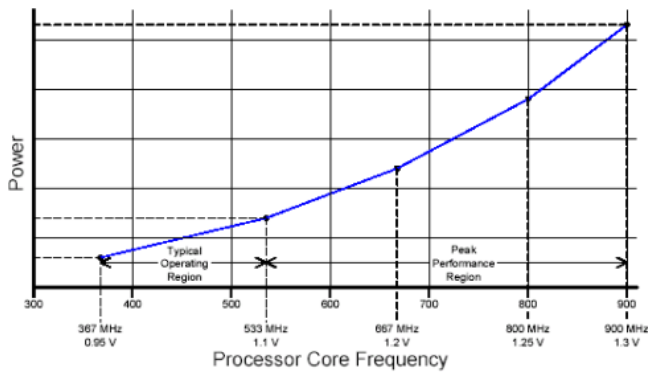


Fig. 1. Transmeta Crusoe TM5800 Power Profile.

performance when necessary and conserves power when demand on the processor is low. DVS is often coupled with frequency scaling in order to maximize the benefits.

### III. XETAL ARCHITECTURE

Due to the growing features and quality improvements, multimedia applications require more and more computational performance at low power consumption. Processing architectures based on Single Instruction Multiple Data (SIMD) paradigm have proven to be efficient in combining high performance at low power while maintaining ease of programmability [3]. For example, the Xetal SIMD processor [4][5] designed in  $0.18\mu\text{m}$  CMOS technology provides up to 8 GOPS performance while dissipating less than 2.0 watts when running at 25 MHz. Since SIMD architectures exploit data parallelism, they are suitable for handling most multimedia applications efficiently. Media processors such as TriMedia and accelerators as in Intel MMX also employ some degree of SIMD processing.

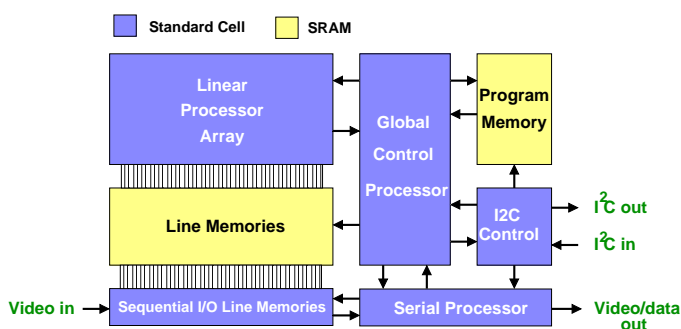


Fig. 2. Xetal Architecture

Xetal is a massively parallel SIMD processor targeted at computationally intensive low-level pixel processing tasks. Xetal is targeted for applications ranging from early vision processing on the sensor side to rendering images on the display side. The architecture is also well suited for smart

vision applications in advanced surveillance systems, machine vision, intelligent home robots, etc. The Xetal architecture is depicted in figure 2. The linear processor array consists of 320 processing elements (PEs) and is the workhorse of the chip. It performs all DSP operations on the incoming video data or data stored in the line memories. Tasks such as conditional execution, iteration and synchronisation are mapped on to the global control processor. The serial processor performs image formatting and statistical computations. The control processor uses the statistical estimates to dynamically update filter coefficients or set sensor control parameters. Xetal has a single channel video input port and a three channel output port for video or data. Please refer to [4] and [5] for detailed discussion on the hardware architecture and the software framework of Xetal.

### IV. EXPERIMENTAL SETUP

Because of the massive parallel architecture of Xetal, low clock frequency (e.g. 25 MHz) was enough to carry out most of the pixel processing algorithms. For our experiment, we have selected three different pixel processing tasks with different computational demands. Since the clock of Xetal is tied to its environment (image sensor and display), frequency scaling was not possible i.e., the chip runs at the pixel clock of the image sensor. However, the Xetal test board does offer control over the supply voltage of the Xetal chip. For all our applications, we scaled the supply voltage from 1.8 volts down to 1.3 volts and measured the current consumption of the chip. These measurements are then used to calculate the power consumed by Xetal at each setting.

The image sensor on the test board runs at a clock frequency of 12.5 MHz, which means it supplies pixel data at the rate of 12.5 MHz. The sensor has a VGA dimension (640 pixels by 480 lines) and a frame rate of 30 frames per second. For our second set of measurement, the image sensor runs at a pixel clock of 6.25 MHz with a frame rate of 15 frames per second.

### V. APPLICATION DESCRIPTION

Xetal applications range from moderate computational complexity (mobile multimedia processing) to more complex and compute intensive applications like industrial machine vision and medical imaging. We choose the following three applications for our experiments.

#### A. Camera Signal Processing

This application has almost all the algorithms that are needed in most digital camera applications and requires around 220 operations per pixel. At 30 frames per second

of VGA-sized images, the total computational requirement is about 1 GOPS. The camera signal processing algorithm includes:

1. Defective Pixel Correction: a majority selection filter, which masks pixels whose values differ from the neighbour by a large value due to manufacturing or radiation defect of the image sensor.

2. Colour Reconstruction: an interpolation filter, which estimates missing colours due to colour sub-sampling in image sensors.

3. Auto-White Balance: an adaptive filter, which reconstructs natural looking colours through colour transformation.

### B. Edge Detection

This application is typical of machine vision tasks, which extracts edges of the objects in the scene for further analysis. Depending on the desired quality, different kinds of edge detection algorithm can be used. In our experiment a simple gradient edge detection filter is used to extract horizontal and vertical edges. The algorithmic complexity is about 124 operations per pixel, equivalent to 570 MOPS at 30 VGA frames per second.

### C. Game of Life

This application simulates the growth of bacterial colonies (a pixel representing a bacteria) under a set of rules that dictates how the colony grows or shrinks. The implementation on Xetal allocates 4 pixels per bacteria for good visibility on the display and simulates a colony of 240 x 320 bacteria. The computational requirement for simulating a single bacterium is about 485 operations. This translates to a total computational load of 1.1 GOPS for 30 simulations per second.

## VI. MEASUREMENT RESULTS

Since our applications are running at a lower frequency (equal to sensor pixel frequency of 12.5 MHz), there is room for scaling the supply voltage. We scaled down the supply voltage with a step of 0.1 V and measured the power consumption at each operating point. 1.3 V is the lowest voltage for running the chip at 12.5 MHz. The nominal voltage of 1.8 V is used as a reference for calculating the power gain.

From the measurement results shown in table I and table II, we observe that by scaling the supply voltage down to 1.3 V we can reduce the power consumption of Xetal in the order of 50% in all the cases. Since the clock frequency is fixed in our case, this translates directly to the

Voltage V	Appl A		Appl B		Appl C	
	Power mW	Gain %	Power mW	Gain %	Power mW	Gain %
1.80	54.90	0.00	43.20	0.00	54.90	0.00
1.70	47.60	13.30	37.40	13.43	48.96	10.82
1.60	41.60	24.23	33.60	22.22	42.56	22.48
1.50	35.70	34.97	30.00	30.56	36.90	32.79
1.40	30.38	44.66	24.50	43.29	31.50	42.62
1.30	26.00	52.64	20.80	51.85	26.39	51.93

TABLE I

MEASUREMENT RESULTS WITH CLOCK OF 12.5 MHz AND FRAME RATE OF 30 FRAMES PER SECOND.

Voltage V	Appl A		Appl B		Appl C	
	Power mW	Gain %	Power mW	Gain %	Power mW	Gain %
1.80	31.50	0.00	26.10	0.00	33.48	0.00
1.70	26.86	14.73	22.95	12.07	28.90	13.68
1.60	23.04	26.86	19.52	25.21	24.64	26.40
1.50	19.50	38.10	15.30	41.38	20.70	38.17
1.40	16.52	47.56	12.88	50.65	17.50	47.73
1.30	13.00	58.73	11.05	57.66	14.69	56.12

TABLE II

MEASUREMENT RESULTS WITH CLOCK OF 6.25 MHz AND FRAME RATE OF 15 FRAMES PER SECOND.

equivalent energy gain. If the application would allow frequency scaling, further reduction in power dissipation is possible. For Xetal, if the application demands less performance, significant power and energy gain can be achieved by scaling down the supply voltage.

## VII. POWER ESTIMATES FOR XETAL-II

The first generation Xetal chip in CMOS 0.18  $\mu\text{m}$  technology runs at 25 MHz and consumes around 2.0 watts when running in maximum performance mode. For Xetal-II, the target frequency is 100 MHz in 0.13  $\mu\text{m}$  CMOS technology and with full VGA frame memory on-chip. In this section, we will discuss the estimated power consumption of the proposed Xetal-II architecture. The estimates are based on analytical calculations and the data sheets for memories.

The on-chip VGA frame memory is built from 40 instances of 128 bit wide memory modules each with 2048 words. Xetal-II core logic (LPA with 16 bit processors, Global Control Processor, I/O Processors) is estimated to be around 250K gates. I/O pads consume 30% of the total core power. Power estimates for the above mentioned

On-chip Frame Memory (1 MB)	1136 mW
Xetal Core Logic (250 KGates)	875 mW
IO Pads	300 mW
Total Xetal-II Chip Power	2311 mW

TABLE III  
XETAL-II POWER ESTIMATES FOR CMOS12 TECHNOLOGY.

components are as shown in table III. Power consumed by the Xetal-II core logic is around 40% of the total power, assuming the memory is accessed every clock cycle. Since this is not the case in most practical applications, the percentage of core power dissipation is somewhat higher. Thus, voltage scaling of the core is a promising approach for saving power.

Supply voltage scaling has an impact on the speed of the core logic as shown in table IV. The table is based on CMOS propagation delay model described in [6] and also shows the achievable power savings for combined voltage and frequency scaling. The table is computed using equations 3 and 4, where  $\alpha$  is technology dependent factor. We assume a value of 1.3 for  $\alpha$  in CMOS 0.13  $\mu m$  technology.

$$f/f_{max} = \frac{(V_{dd} - V_t)^\alpha}{(V_{ddmax} - V_t)^\alpha} \quad (3)$$

$$P/P_{max} = \left( \frac{V_{dd}}{V_{ddmax}} \right)^2 \left( \frac{f}{f_{max}} \right) \quad (4)$$

$V_{dd}$	$V_{dd}/V_{ddmax}$	$f/f_{max}$	$P/P_{max}$
1.2	1.00	1.00	1.00
1.1	0.92	0.85	0.71
1.0	0.83	0.71	0.49
0.9	0.75	0.57	0.32
0.8	0.67	0.44	0.19
0.7	0.58	0.32	0.11

TABLE IV  
EFFECT OF VOLTAGE SCALING.

As shown in table IV, by voltage and frequency scaling we can save power ranging from 30% to 90% at the cost of reduced performance. For the Xetal core, this translates to 12% to 40% of the total chip power. This is significant power gain and motivates us to go for voltage and frequency scaling for power management.

### VIII. POWER MANAGEMENT ON XETAL - TEST CHIP

Before implementing power management on Xetal-II, we decided to tapeout a small test-chip with independent

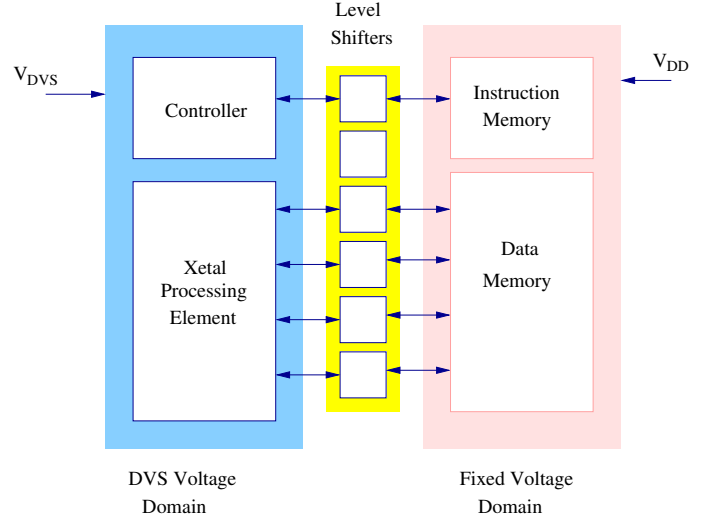


Fig. 3. Test-chip for power management using voltage scaling.

voltage domains and level-shifters cells to communicate between the two voltage domains. The test-chip has one of the Xetal processing elements, a controller and small program and data memory. The block diagram of the test-chip is shown in figure 3. The objective of the test-chip are the following: (i) to verify implementation of voltage domains and the level shifter cells. (ii) to verify the feasibility of implementing DVS for the Xetal core. (iii) to measure power/energy gains of DVS on Xetal core. (iv) to study  $V_{dd} - f$  trade-off for Xetal core.

The layout of the test-chip is shown in figure 4. The test-chip is designed in 0.13  $\mu m$  CMOS technology with a target frequency of 150 MHz. The total chip area is 1.3 sq.mm. The test-chip has two independent voltage domains: (i) a variable voltage domain with Xetal processing element and the controller, (ii) a fixed voltage domain for the program and data memory. The communication between the two voltage domains is done by the level shifter cells. The variable voltage domains is controlled from outside the chip.

### IX. DYNAMIC VOLTAGE SCALING FOR XETAL-II

For our final implementation of Xetal-II, we plan to have two voltage domains on the chip as on the testchip. All the memories (frame memory and program memory) will have a fixed voltage to guarantee the proper functioning of the memory modules. The rest of the digital logic blocks will have a variable voltage. Level shifter cells will be used at the interface between the two voltage domains.

For the Xetal-II compiler to support power management using voltage scaling, we propose to have off-line voltage scheduling scheme. Figure 5 shows the process of compile-time off-line voltage scheduling for power man-

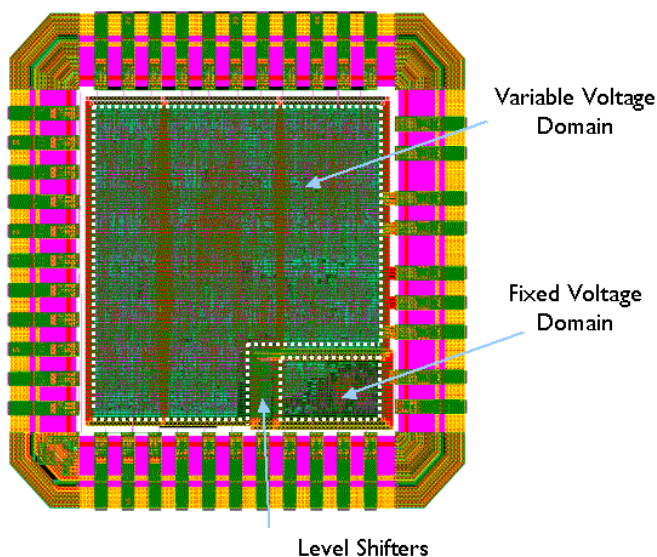


Fig. 4. PMoX - Power Management on Xetal, test-chip layout

agement. Depending on the performance requirement of the task being executed on the Xetal core, the compiler will schedule voltage on its core. Additional instruction will be added to Xetal instruction set. These instructions will enable the controller to set the core operating voltage and frequency.

The original C code is profiled to measure the computational demand of various tasks in the applications. The profiled data is then used to tag the task with its performance requirement, which in turn will be used to assign voltage and frequency for that particular task. This information will then be used for appending the code with instructions, which will set voltage and frequency of the core as per the requirement.

## X. CONCLUSION

SIMD architectures like Xetal exhibit high silicon efficiency (MOPS/Watt) since they exploit the data parallelism available in most video/image processing applications. However, the level of parallelism (hence, inherent performance) is usually high compared to what applications demand in dynamic situations. In this paper, we have shown how dynamically controlling the operating voltage and frequency of the processor according to the performance demands of the application can further improve the power efficiency of the SIMD processor.

Dynamic voltage scaling experiments were conducted to study the power consumption of three video processing applications (VGA resolution at 30 frames/second) running on Xetal. From the measurement results, we observe that scaling the supply voltage from 1.8 V to 1.3 V can re-

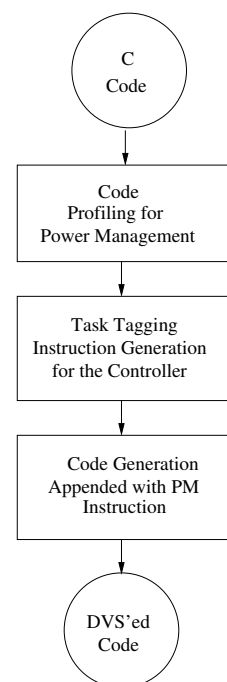


Fig. 5. Off-line compile time voltage scheduling for power management

duce the power consumption of Xetal by more than 50%. Analysis of the Xetal-II architecture for CMOS 13  $\mu m$  technology shows that by voltage scaling of the core, we can save power ranging from 30% to 90% at the cost of reduced performance for Xetal core, which translates to 12% to 40% of the total chip power. Dynamically scaling the frequency and voltage together shows a promising approach for optimizing the power and energy consumption.

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