

An Ultrawideband CMOS Low-Noise Amplifier with Dual-Loop Negative Feedback

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Abstract— A Low-Noise Amplifier for ultrawideband (UWB) applications is presented. Dual-loop negative feedback is favorable, since it can achieve impedance matching and very low noise at the same time, and saves a lot of chip area as no bulky inductors are needed. We employ a nullor and a resistive feedback network and, in order to fulfill the noise-figure and power-gain requirements for an UWB receiver, define the values of the feedback elements involved. The input stage of the nullor is very important for noise, so to optimize the noise performance, we define the width and bias current of its input transistor. For the output stage, we have to make sure that the finite output impedance will not affect our impedance matching. To obtain a large bandwidth, we add an intermediate stage and optimize the width of all the transistors involved. Frequency compensation is necessary to ensure the circuit stability. The design is based on TSMC 0.18 μ m CMOS technology. Post-layout simulations show that the gain of the LNA is 18.8dB and the bandwidth spans from 3GHz to 8GHz, the S_{11} is below -10 dB up to 10GHz and the minimum noise figure is 2.0dB for a 3.3V supply voltage, while consuming 15mA. At the end of this paper, a comparison with previously reported works is given and the advantages and disadvantages of the proposed LNA are discussed.

Index Terms— dual-loop negative feedback, ultrawideband (UWB), low-noise amplifier (LNA), broadband, impedance matching

I. INTRODUCTION

ULTRA WIDEBAND (UWB) is one of the most promising approaches to radio communication due to its inherent ability of transmitting data over a wide frequency spectrum with high speed and low power. With these advantages, UWB can be used for imaging systems, vehicular and ground-penetrating radars and wireless communication systems. Especially for Personal Area Networks, it can provide wireless link connection at home and in the office instead of heavy cables with data rates of a few hundred megabits up to a few gigabits. UWB communication poses big challenges for low noise amplifier (LNA) design. Since the LNA is the first active component close to antenna, it must provide sufficient low noise behavior not only at one frequency but over the whole bandwidth of 7.5GHz. The

targeted noise figure is around 2dB, which is quite a challenging value compared to other reported works. Power gain is another important parameter; S_{21} should be larger than 15dB. Wideband matching is another critical issue: we have to match the LNA to 50Ω , the characteristic impedance of the antenna, so S_{11} should be below -10 dB over the entire frequency band. At the same time, we need to ensure that matching network will not destroy the noise performance and waste chip area. Some LNA designs by other UWB groups in the world employ LC ladder networks. However, an inductor is a costly component since it consumes most of the chip area and also introduces a lot of parasitic resistance that will increase noise. Power consumption is another consideration. Our goal is to limit the current consumption to 15mA. The IC technology we use is TSMC (Taiwan Semiconductor Microelectronics Corp.) 0.18 μ m CMOS.

In Section II, we will discuss the dual-loop feedback topology chosen for the LNA and we will define the feedback network according to our specifications. In Section III a nullor implementation with optimized performance and relevant simulation results will be presented. A comparison between our work and previously reported wide-band amplifiers will be given in Section IV.

II. LNA TOPOLOGY

A. Resistive Feedback

To achieve accurate input impedance matching, we use two feedback loops: a voltage-to-current (V-I) feedback loop and an indirect current-to-current (I-I) feedback loop, as shown in Fig. 1. The reason that this topology is called “indirect feedback” is because the I-I feedback does not sense the output directly, but senses it in an indirect way, by means of a replica of the output current.

For the I-I loop, it holds,

$$\frac{I_o}{I_i} = 1 + \frac{R_2}{R_1} \quad (0.1)$$

For the V-I loop,

$$\frac{I_o}{V_i} = \frac{1}{R_f} \quad (0.2)$$

R_f denotes the V-I feedback resistor and R_1 and R_2 are the current divider resistors. Hence, we can define the input impedance as:

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$$R_i = \frac{V_i}{I_i} = \frac{I_o/I_i}{V_i} = \left(1 + \frac{R_2}{R_1}\right)R_f \quad (0.3)$$

By proper selection of the feedback resistors, appropriate values for the input impedance, power gain and noise figure can be designed.

For the power gain (S_{21}), we can derive

$$S_{21} = \frac{P_o}{P_i} = \frac{I_o I_o}{I_i V_i} Z_l = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{R_f} Z_l \quad (0.4)$$

Z_l being the load impedance, usually equal to 50 ohms. We need S_{21} larger than 15dB in our design.

So from (0.3) and (0.4), we have

$$R_f \leq 8.8\Omega \quad (0.5)$$

$$\frac{R_2}{R_1} = \frac{50}{R_f} - 1 \leq 4.7 \quad (0.6)$$

The resistors in the two feedback loops will contribute noise and have influence on the noise transfer. After shifting and combining all the noise sources, we arrive at the following expression for the total noise voltage power spectral density:

$$S_{v_n,eq} = 4kTR_s + (R_s + R_f)^2 \bar{i}_n^2 + \left(1 + \frac{R_s}{R_2}\right) \bar{v}_n^2 + \frac{R_s^2}{R_2} 4kT + 4kTR_f \quad (0.7)$$

v_n and i_n are the equivalent voltage and current noise sources of the first stage of the nullor. R_s is the source impedance, assumed to be 50 Ω . As we can see from the equations above, R_1 does not appear in the equation while R_2 and R_f do. If we decrease the value of R_f and increase the value of R_2 , the total noise power spectral density will be reduced. So in order to achieve low noise, R_f has to be chosen as small as possible and R_2 as large as possible. However, some practical limitations arise. For example, if R_f is too small, the distortion is getting worse, because for the same input signal, more current needs to flow through it. This is likely to cause clipping distortion. From a technology point of view, R_2 should be between a few hundred and a few kilo ohms. Based on simulation results we choose $R_f=8\Omega$, $R_2=5.25k\Omega$ and $R_1=1k\Omega$, so $S_{21}=15.9\text{dB}$ and $NF=0.71\text{dB}$.

B. Capacitive Feedback

Instead of using resistive feedback by means of R_1 and R_2 , it is possible to use inductors as I-I feedback elements as long as you keep the current division, set by the ratio of both inductances constant; it will not change the impedance matching and power gain. However, for the same reason the excludes the use of LC ladders, we cannot use inductors as they consume a rather large area.

On the other hand, capacitive feedback, thus by means of capacitors, also provides an accurate current division, and does not contribute thermal noise. As a consequence, the noise figure can be made smaller. For capacitive feedback, we have

$$S_{v_n,eq} = 4kTR_s + (R_s + R_f)^2 \bar{i}_n^2 + \left(1 + \frac{R_s}{R_2}\right) \bar{v}_n^2 + 0 \quad (0.8)$$

Z_2 should have same impedance as R_2 at the highest frequency to suppress the noise of the nullor. However, from

calculations and simulations it follows that the difference between the resistive and capacitive feedback networks is equivalent to the noise generated by a 0.5 ohm resistor. As a consequence, capacitive feedback does not help much to improve the noise performance. Moreover, a drawback of capacitive feedback is that it will make the loop gain dependent on the frequency. It will also add an additional pole to system transfer that has to be compensated for in the subsequent receiver block.

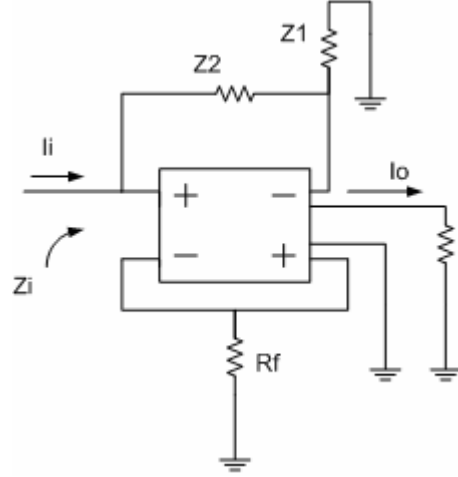


Fig. 1. Dual loop indirect negative-feedback power-to-current amplifier

III. NULLOR DESIGN

The nullor is a very critical part in our design, since the parameters such as bandwidth, noise figure, distortion etc. will all depend on how good the nullor implementation is.

For proper design of the first stage, its noise performance is of prime importance. Further, a high gain is required to suppress noise from other stages. Generally, a nullor at least has two stages, but in order to increase the bandwidth, we can add intermediate stages. Each stage will add gain and a dominant pole, so if more than 3 stages are used, frequency compensation will be very difficult, compromising the stability of the circuit.

A. Input Stage

As we discussed above, for the first stage, noise is the main consideration. Since its noise figure is inversely proportional to the drain bias current, I_d , in order to minimize the noise, I_d should be chosen as large as possible. Trading off noise figure for power consumption, we choose 4mA for the drain current of the first stage.

Since the gain of a transistor is proportional to its g_m , which, in turn, is proportional to its W/L , W being the width of the transistor and L its length, we choose the minimum feature size 0.18 μm for L . In weak inversion, the g_m of the transistor no longer depends on its width and as the parasitic capacitances still do, the gain of the transistor reduces again for increasing widths. As a consequence, the NF increases again. As a compromise, we choose $W=100\mu\text{m}$, yielding a NF as shown in Fig. 2.

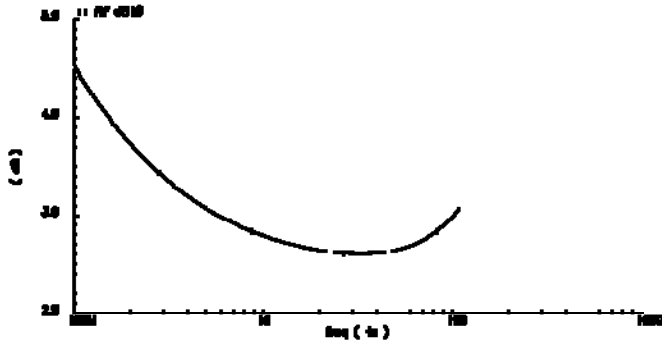


Fig. 2. NF of first stage as a function of frequency for $W=100\mu\text{m}$, $I_d=4\text{mA}$

1) Noise Matching

As we can see in Fig. 2, the minimum NF is about 2.6dB. We can introduce another degree of freedom that leads to lower NF . Inductor noise matching is often applied in narrow band amplifiers, but seldom applied in wide-band negative-feedback amplifier design. Here, we introduce the use of an inductor in series with the input of the first stage transistor. It will resonate with C_{gs} at a particular frequency to keep the NF close to the minimum noise figure, NF_{\min} . The value of the inductor is derived from circuit simulations on the circuit in Fig. 3. The noise figure results are shown in Fig. 4.

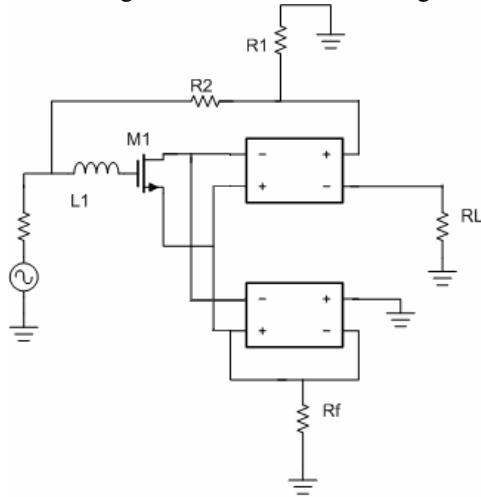


Fig. 3. Circuit diagram used for noise simulation of first stage

The inductor using in the simulation is still considered to be ideal. We will replace it with a realistic model later.

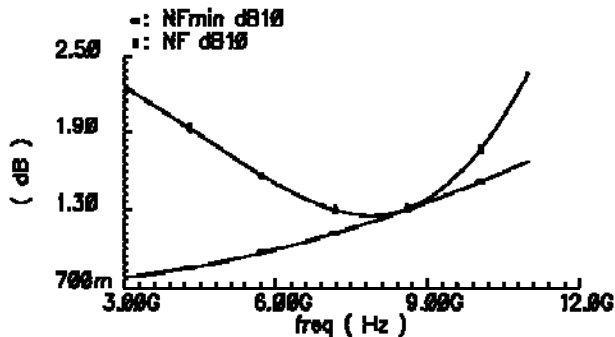


Fig. 3. NF and NF_{\min} after inductive noise matching

Based on the simulation results, we choose $L_1=2\text{nH}$. The minimum value of NF is around 1.3dB and is equal to NF_{\min} at 8GHz. The average value of NF is below 2dB, so this method improves the noise performance a lot.

2) Current Follower

C_{gd} of M1 introduces an extra pole and will reduce the bandwidth. To reduce its effect, we use a CG (common-gate) stage as current follower, as shown in Fig. 5. Now C_{gd} is in parallel with C_{gs} and $1/g_m$ of the CG stage. We choose its width equal to $100\mu\text{m}$ and a 3mA bias current.

As shown in Fig. 5, we even add an extra CG stage, so two CG stages are following the input stage. This additional increase in output impedance means more output current of first stage will flow to the next stage, M4.

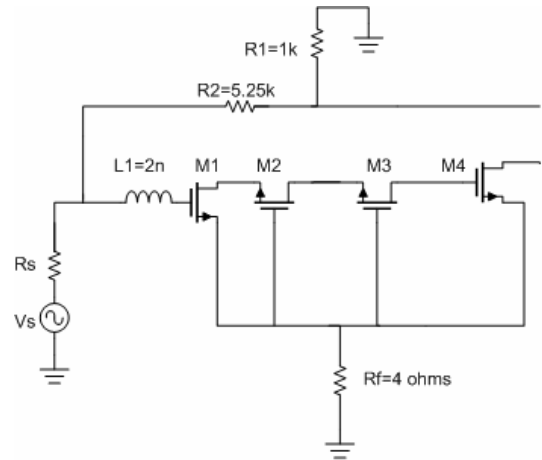


Fig. 5. Current follower after first stage

B. Output Stage

For the two (indirect) output stages, like for the input stage, to have a large gain, we use CS stages. The width of each transistor equals $120\mu\text{m}$. Their bias currents equal 3mA.

Unfortunately, the output impedances of both CS stages is not very large. As a consequence, they will load the feedback network and affect the impedance matching. To achieve a high gain and a large output impedance, we use a cascode structure for both output stages as shown in Fig. 6. To increase the loop gain, we add an intermediate CS stage, its width= $100\mu\text{m}$ and bias current=3mA.

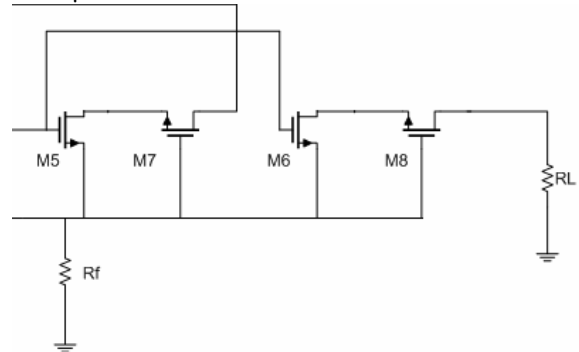


Fig. 6. Cascode structure for output stage

IV. CONCLUSIONS

We have demonstrated an ultrawideband LNA with dual-loop negative feedback in TSMC 0.18 μ m CMOS technology. It has a high gain of 18.8dB over a bandwidth up to 8GHz with a minimum noise figure of 2dB. S_{11} is below -10 dB from very low frequencies up to 10GHz. Since the supply voltage is 3.3 V, and the total current consumption is 15mA, the power consumption equals 50mW. In table 1, below, a comparison with previous UWB LNA designs is made. We can state that our work is one of the most advanced LNA solutions for UWB applications and that it can also be used for other, e.g., multi-band, applications due to its wide-band features. Further there are some advantages and disadvantages over previously published designs.

Advantages: We only use two inductors in total compared to solutions that distributed or LC-ladder networks. This means that our chip will be much smaller and cheaper. We use standard CMOS technology. We achieve very low noise, high gain and wide band matching at reasonable power consumption. Since the design is based on negative feedback, it benefits from technology (fT) advancements, leading to a larger loop gain and hence a larger bandwidth and a lower power consumption.

TABLE 1: COMPARISON WITH THE STATE-OF-THE-ART REPORTED WIDEBAND AMPLIFIERS

	Technology	S11 [dB]	S21 [dB]	B [GHz]	N _{fmin} [dB]	Power [mW]	IIP3 [dBm]
[2]	0.18 μ m CMOS	<-9.9	9.3	2.3-9.2	4.0	9	-6.7 @6GHz
[6]	0.18 μ m CMOS	<-8	8.1	0.6-22	4.3	52	N/A
[7]	0.18 μ m CMOS	<-11	10.6	0.5-14	3.5	52	N/A
[8]	0.5 μ m SiGe	<-8	12	0-15	2.8	24	1.9 @2GHz
[1]	0.18 μ m SiGe	<-9.6	21	3.0-9.6	2.5	30	-5.5 @3.5GHz
Our work	0.18 μ m CMOS	<-10	18.8	3.0-8.0	2.0	50	-8.2 @5GHz

Disadvantages: We use three CS stages in our circuit, rendering frequency compensation more difficult. The voltage-to-current feedback resistor R_f is so small that it is very sensitive to parasitic capacitance and resistance of wires, so integration with other circuits and packaging must be done very carefully.

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